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Design, Fabrication and Characterization of GaN HEMTs for Power Switching Applications

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Abstract

The unique properties of the III-nitride heterostructure, consisting of gallium nitride (GaN), aluminium nitride (AlN) and their ternary compounds (e.g. AlGaN, InAlN), allow for the fabrication of high electron mobility transistors (HEMTs). These devices exhibit high breakdown fields, high electron mobilities and small parasitic capacitances, making them suitable for wireless communication and power electronic applications. In this work, GaN-based power switching HEMTs and low voltage, short-channel HEMTs were designed, fabricated, and characterized.

In the first part of the thesis, AlGaN/GaN-on-SiC high voltage metal-insulator-semiconductor (MIS)HEMTs fabricated on a novel 'buffer-free' heterostructure are presented. This heterostructure effectively suppresses buffer-related trapping effects while maintaining high electron confinement and low leakage currents, making it a viable material for high voltage, power electronic HEMTs. This part of the thesis covers device processing techniques to minimize leakage currents and maximize breakdown voltages in these 'buffer-free' MISHEMTs. Additionally, a recess-etched, Ta-based, ohmic contact process was utilized to form low-resistive ohmic contacts with contact resistances of 0.44-0.47 Ω·mm. High voltage operation can be achieved by employing a temperature-stable nitrogen implantation isolation process, which results in three-terminal breakdown fields of 98-123 V/μm. By contrast, mesa isolation techniques exhibit breakdown fields below 85 V/μm and higher off-state leakage currents. Stoichiometric low-pressure chemical vapor deposition (LPCVD) SiN_x passivation layers suppress gate currents through the AlGaN barrier below 10 nA/mm over 1000 V, which is more than two orders of magnitude lower compared to Si-rich SiN_x passivation layers. A 10% dynamic on-resistance increase at 240 V was measured in HEMTs with stoichiometric SiN_x passivation, which is likely caused by slow traps with time constants over 100 ms. SiN_x gate dielectrics display better electrical isolation at high voltages compared to HfO_2 and Ta_2O_5. However, the two gate oxides exhibit threshold voltages (V_{th}) above -2 V, making them a promising alternative for the fabrication of recess-etched normally-off MISHEMTs.

Reducing the gate length (L_g) to minimize losses and increase the operating frequency in GaN HEMTs also entails more severe short-channel effects (SCEs), limiting gain, output power and the maximum off-state voltage. In the second part of the thesis, SCEs were studied in short-channel GaN HEMTs using a drain-current injection technique (DCIT). The proposed method allows V_{th} to be obtained for a wide range of drain-source voltages (V_{ds}) in one measurement, which then can be used to calculate the drain-induced barrier lowering (DIBL) as a rate-of-change of V_{th} with respect to V_{ds}. The method was validated using HEMTs with a Fe-doped GaN buffer layer and a C-doped AlGaN back-barrier with thin channel layers. Supporting technology computer-aided design (TCAD) simulations indicate that the large increase in DIBL is caused by buffer leakage. This method could be utilized to optimize buffer design and gate lengths to minimize on-state losses and buffer leakage currents in power switching HEMTs.

Keywords: GaN HEMT, 'buffer-free', high voltage, isolation, passivation, gate dielectric, SCE, DIBL, DCIT

List of Publications

Appended Publications

This thesis is based on work contained in the following papers

[A] **B. Hult**, M. Thorsell, J. T. Chen, N. Rorsman, "High Voltage and Low Leakage GaN-on-SiC MISHEMTs on a 'Buffer-Free' Heterostructure", *IEEE Electron Device Letters*, vol. 43, no. 5, pp. 781-784, May 2022

[B] **B. Hult**, M. Thorsell, J. T. Chen, N. Rorsman, "AlGaN/GaN/AlN 'Buffer-Free' High Voltage MISHEMT with Si-rich and Stoichiometric SiN_x First Passivation", accepted for a presentation at *Compound Semiconductor Week*, June 1-3, 2022

[C] **B. Hult**, J. Bergsten, R. Ferrand-Drake Del Castillo, V. Darakchieva, A. Malmros, H. Hjelmgren, M. Thorsell, N. Rorsman, "Investigation of Electron Confinement in GaN HEMTs with a Drain Current Injection Technique", submitted to *IEEE Transaction on Electron Devices*, 2022

Other Publications

The content of the following publication is out of the scope of this thesis

[a] A. Papamichail, A. Kakanakova, E. O. Sveinbjörnsson, A. R. Persson, **B. Hult**, N. Rorsman, V. Stanishev, S. P. Le, P. O. Å, Persson, M. Nawaz, J.-T. Chen, P. Paskov, V. Darakchieva, "Mg-doping and free-hole properties of hot-wall MOCVD GaN", accepted for publication in *Journal of Applied Physics*

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Chapter 1

Introduction

Power electronic converters play a vital role in the electrification of our increasingly energy-demanding society. Consumer electronics, motor drivers, renewable energy, and power grids require power conversion in the form of DC-DC (buck, boost), AC-AC, DC-AC (H-bridge), and AC-DC (three-phase). Two necessary building blocks in any power electronic converter are power electronic diodes and transistors, which act as passive and active switches. An ideal power electronic switch can conduct arbitrarily large currents with zero power dissipation in the on-state, block arbitrarily large voltages in the off-state, and switch between the two states at any frequency without dissipating any power. However, any realizable power electronic switch will exhibit on-state losses, switching losses and limitations to the off-state voltage. These constraints depend on the semiconductor material properties and the device design. Semiconductor materials with a high critical electric field are of primary interest since they allow for lateral and vertical downscaling, which reduces on-resistance (R_{on}) and, therefore, on-state losses [1]. The reduction of parasitic capacitances (C_{oss}, C_{iss}) and gate charge is also highly important, since these quantities affect the transition time between on-state and off-state (and vice versa), which, in turn, impacts switching losses and switching frequency. Devices with higher switching frequencies also allow for downscaling of passive elements (e.g. inductors and capacitors) in power electronic circuits, reducing the overall module size further.

Si has been the most prevalent semiconductor since the onset of solid-state power conversion. However, the interest in wide bandgap semiconductors such as SiC and GaN has rapidly increased due to their high breakdown fields and high electron mobilities [2]. SiC power switching devices, including metal-oxide-semiconductor field-effect transistors (MOSFETs), junction FETs (JFETs), and insulated gate bipolar transistors (IGBTs), exhibit a smaller tradeoff between R_{on} and breakdown voltage (BV) compared to their Si counterparts (Figure 1.1). SiC IGBTs are typically suitable for power switching applications where the blocking voltage requirement is above 10 kV due to the smaller drift region thickness required for IGBTs compared to SiC MOSFETs [3]. These applications include high voltage transmission and

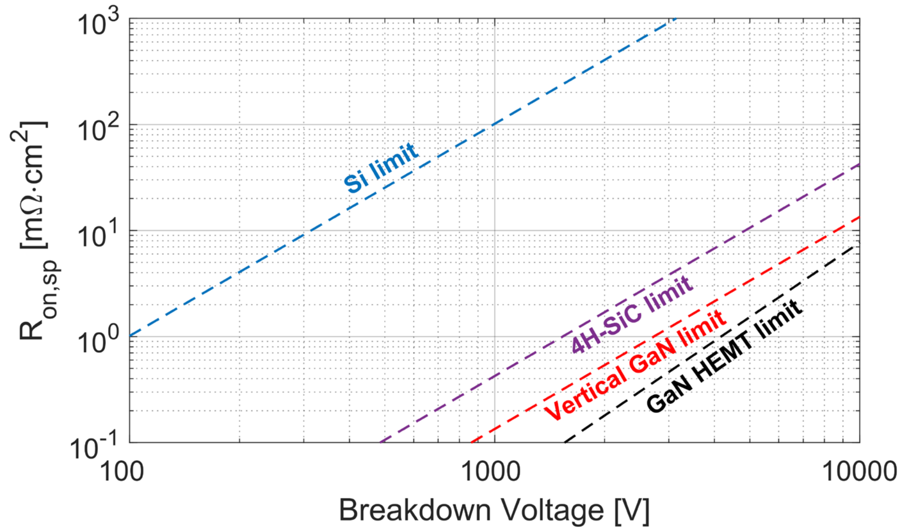

Figure 1.1. Ideal specific on-resistance for Si, 4H-SiC and GaN. The semiconductor properties of the respective materials were taken from [1], [2].

smart grids. On the other hand, MOSFETs tend to have better current handling capabilities at switching frequencies above 5 kHz [3]. Both MOSFETs and JFETs are more suitable for low voltage and medium-to-high frequency applications. In voltage classes up to 1200 V, SiC MOSFETs and JFETs are already commercially available [4]. These devices show lower switching and on-state losses compared to Si IGBTs to at least 100 kHz [5].

GaN-based semiconductors allow for the fabrication of power electronic devices with lower R_{on} for a given breakdown voltage relative to their Si and SiC counterparts (Figure 1.1) [1], [6]. Furthermore, the high spontaneous and piezoelectric polarization in GaN and its alloy AlGaN can be utilized to form a two-dimensional electron gas (2DEG) at the interface of an AlGaN/GaN heterostructure. This, in turn, can be used for fabricating HEMTs, which exhibit high electron saturation velocities, high electron mobilities and high electron carrier concentrations [7]. Additionally, GaN HEMTs display lower parasitic capacitances, gate charge, and reverse recovery charge compared to conventional Si MOSFETs [8]–[11], and SiC MOSFETs [12]–[14] rated at, or below, 1200 V. This enables higher switching frequencies and reduces switching losses. In the first part of this work, power electronic GaN HEMTs operating above 1200 V are primarily studied.

Commercially available GaN-on-Si HEMTs typically operate in the 650 V and 1200 V voltage classes [15], [16]. Moreover, GaN-based HEMTs operating beyond 1200 V have been (and are still being) researched [17]–[20]. However, GaN-on-Si HEMTs are not without their disadvantages. The thermal and lattice mismatch between GaN and Si necessitates thick buffer layers to reduce the concentration of growth defects [2], [21]. Additionally, the buffer layer is typically doped with carbon or iron to suppress vertical leakage current [21]–[23], which is one of the limiting factors in GaN-on-Si high voltage HEMTs. An alternative to Si is semi-insulating (SI) SiC, which offers higher thermal conductivity, higher electrical resistivity, and a

lower lattice mismatch between SiC and GaN [2]. In GaN-on-SiC heterostructures, it is also common to grow highly resistive carbon or iron-doped buffers to reduce lateral leakage currents [24]–[26]. However, growing GaN with high carbon concentration leads to trapping states, which has a negative impact on dynamic on-resistance ($R_{on,dyn}$) and drain lag [24]–[26].

A new type of 'buffer-free' heterostructure deposited on a SI-SiC has been proposed [27], [28], which consists of a thin AlN nucleation layer, a thin unintentionally doped (UID) GaN layer, an AlGaN barrier, and a GaN capping layer. Together, they form a 2DEG with high electron confinement without needing any intentionally doped carbon buffer layer. Furthermore, the highly resistive SiC substrate effectively eliminates vertical leakage currents and breakdown at high voltages. This means that the high voltage capability and $R_{on,dyn}$ are limited by the device processing, the quality of the AlN, GaN or AlGaN layers, or their interfaces. Processing parameters that can affect high voltage operation or $R_{on,dyn}$ include source and gate-integrated field plates, the type of passivation, and the type of electrical isolation [19], [29]–[32]. However, to what extent these parameters impact the breakdown voltage, R_{on} and $R_{on,dyn}$ in 'buffer-free' HEMTs are still relatively unexplored. In Chapter 2, different electrical isolations, SiN_x passivation layers, and gate dielectrics are compared in terms of their impact on off-state leakage currents and breakdown voltages in 'buffer-free' HEMTs. In addition, a novel Ta-based ohmic contact metallization was employed on this type of heterostructure. This part of the work is used as a foundation for [Paper A-B].

GaN HEMTs have also played a major role in high power and high-frequency applications [33], [34]. In order to realize high-frequency operation, it is common to laterally downscale the transistor as much as possible to reduce losses and increase the current gain and power gain cut-off frequencies [35]. This involves gate length (L_g) reduction and minimization of the access regions. However, reducing L_g also entails more severe SCEs, which reduce gain, efficiency, and output power [35]. These effects give rise to DIBL, which is a negative shift of the V_{th} toward more negative values at high V_{ds}. DIBL is traditionally characterized by calculating the relative shift of two transfer curves at different values of V_{ds}. However, with this method it is difficult to track large, sudden changes in V_{th} with respect to V_{ds}.

In Chapter 3, an alternative technique will be presented in which V_{th} is measured for a large range of V_{ds} in a single measurement. From this measurement, it is possible to observe the evolution of DIBL as V_{ds} increases. This becomes useful when assessing a suitable bias range in HEMTs. This technique can also be applied to power switching HEMTs to optimize the gate length in terms of DIBL (at high voltages) and R_{on}. In this part of the thesis, the method is evaluated using HEMTs with short gate lengths and two types of epitaxial heterostructures. This is based on the work presented in [Paper C].

Chapter 2

'Buffer-Free' GaN-on-SiC High Voltage HEMTs

The design goal of any power electronic HEMT is to maximize the off-state breakdown voltage while simultaneously minimizing R_{on}, $R_{on,dyn}$ and parasitic capacitances. One strategy for increasing the breakdown voltage is to scale up the component by increasing the gate-drain distance (L_{gd}). In doing so, the access region increases in size, which leads to a higher R_{on} and, therefore, on-state losses. The lowest specific on-state resistance ($R_{on,sp}$) in HEMTs for any given breakdown voltage follows the relation given by

$$R_{on,sp} = \frac{BV^2}{q\mu_n n_s E_{crit}^2} \tag{2.1}$$

where q, μ_n, n_s, and E_{crit} are the elementary charge, electron mobility, sheet carrier concentration, and critical electric field of GaN, respectively [1]. However, in a real device, there is a multitude of material growth and device processing parameters that can cause the $R_{on,sp}$-BV relation to deviate from the ideal relation in Equation 2.1. For instance, defects in the crystal structure, dopants, surface contaminants, and the quality of the dielectrics (and their interfaces) deposited on the III-nitride surface can negatively affect the device's breakdown voltage and the critical electric field of GaN. This can manifest as an elevated off-state leakage current, a dielectric breakdown, or a sudden current surge due to some unintentionally added leakage path in the III-nitride heterostructure.

In addition, trapping-related effects, which negatively impact the dynamic performance, are highly influenced by the quality of the heterostructure and the dielectrics deposited on it. During off-state stress, electrons can start to occupy acceptor-like states in the vicinity of the 2DEG at the heterostructure interfaces, in the buffer, or at the III-nitride surface. These traps can have a longer de-trapping time than the off-to-on state switching time. As a result, the 2DEG remains

partially depleted during the on-state, which reduces the on-state current. Therefore, optimizing both GaN material growth and device processing parameters is essential to reduce these unwanted effects.

Substrate Alternatives

The type of substrate on which the III-nitride heterostructure is grown strongly impacts the resulting semiconductor properties. Discrepancies in lattice constant and thermal expansion coefficients can give rise to dislocations, which can negatively affect electron mobility and maximum drain current in HEMTs [36], [37]. In addition, the bandgap and doping concentrations of the substrate affect the number of charge carriers, which, in turn, influences vertical leakage currents. Table 2.1 summarizes the properties of common substrates for GaN.

Si substrates are currently the most popular alternative for power electronic GaN HEMTs due to their low cost [38], [39]. However, the small bandgap of Si results in a high intrinsic carrier concentration and, therefore, a low resistivity. This leads to high vertical leakage currents during high voltage operations. Moreover, Si substrates typically require a strain relaxation layer to prevent large wafer bowing and cracks in the GaN epitaxial layers [40].

Sapphire (Al_2O_3) has traditionally been utilized for GaN growth in solid-state lighting applications due to its low cost, high-temperature stability, and high electrical resistivity [41]. However, the poor thermal conductivity and large lattice mismatch with GaN make sapphire less suitable for power switching HEMTs.

SiC and GaN substrates have emerged as two alternatives to Si and sapphire. Both offer a high electrical resistivity due to their large bandgaps, which reduce vertical off-state currents. The advantage of GaN substrates is that they do not require any nucleation layer to promote GaN growth, which removes any additional thermal boundary resistances between the III-nitride epi and the substrate. Additionally, GaN-on-GaN homoepitaxy can suppress dislocation densities below 10^5 [43], making it a preferred choice for lateral GaN devices. However, low growth rates currently limit the large-scale production of SI-GaN wafers, making it the most expensive and least accessible substrate among the four presented in Table 2.1.

Table 2.1. Material properties of substrates used for GaN HEMTs [2], [42].

Parameter	Si	Sapphire	4H-SiC	GaN
Bandgap (eV)	1.12	8.1-8.6	3.26	3.39
Thermal conductivity (W/cm·K)	1.5	0.23	3.8	1.3 / 3
Lattice mismatch (%)	-17	-16	+3.5	None
Thermal mismatch (%)	+116	-25	+33	None

SiC substrates combine a high thermal conductivity with a low lattice mismatch to GaN. This makes SiC an excellent choice for both high power microwave HEMTs and power electronic HEMTs, as it allows for improved epitaxial crystal quality and heat dissipation. Furthermore, the increasing demand for GaN-on-SiC microwave HEMTs and SiC power devices has incentivized research into bulk n-type SiC and SI-SiC growth. Thus, GaN-on-SiC could become an alternative to GaN-on-Si for future power switching applications.

Conventional Buffer Designs

AlGaN/GaN-based heterostructures grown on foreign substrates mainly consist of four layers (Figure 2.1): (1) an AlN nucleation layer, (2) a thick GaN buffer layer, (3) a UID-GaN layer, and (4) an AlGaN barrier layer to form the 2DEG. A strain relief layer is sometimes also grown after the nucleation layer to reduce the stress in the GaN buffer.

The purpose of the nucleation layer is to facilitate the formation of GaN crystals and allow them to promote lateral growth [44]. This layer also reduces the dislocation density significantly compared to GaN grown directly onto a foreign substrate [45]. The thick buffer layer grown on top of the nucleation layer serves two functions: (a) to further reduce the impact of dislocations and other growth defects in the vicinity of the active areas [21], and (b) to reduce vertical leakage currents (mainly applicable for conductive substrates). In addition to being detrimental to the on-state performance of the HEMT, dislocations can serve as vertical leakage paths during high voltage operation [46]. When the III-nitride heterostructure is grown on a conductive substrate, these additional leakage paths can lead to premature breakdown.

When the buffer layer is grown using metalorganic chemical vapor deposition (MOCVD) or hydride vapor phase epitaxy (HVPE), O, Si and N vacancies are unintentionally introduced into the crystal structure. These act as donor states, which increases the electron carrier concentration and reduces the resistivity of the buffer layer [47]–[49]. As a consequence, the drain-source current can be canalized under the depleted channel region during high off-state drain biases. In order to counteract this effect, it is common to intentionally add deep-level acceptor states to compensate the donors in the crystal structure. This leads to a higher resistivity, which improves the electron confinement and reduces vertical leakage currents. The two most commonly used acceptors in GaN HEMT heterostructures are C and Fe.

Iron is typically incorporated into GaN by introducing ferrocene in MOCVD [22]. The Fe atoms predominantly substitute Ga (i.e. Fe_{Ga}) due to its low formation energy [50], which leads to the creation of an acceptor level 0.5-0.7 eV below the conduction band edge (E_c) [51], [52]. Fe-doped GaN provides good insulation with sheet resistances as high as $7 \cdot 10^9$ Ω·cm at a doping concentration of $1.3 \cdot 10^{19}$ cm^{-3} [22]. Furthermore, it has also been shown that GaN can reach lateral breakdown fields up to 2 MV/cm at high Fe-concentrations of $4 \cdot 10^{20}$ cm^{-3} [53]. However, the surface morphology can deteriorate at concentrations above 10^{20} cm^{-3} [22]. Iron-related traps also tend to cause $R_{on,dyn}$ dispersion. Hilt et al. demonstrated that $R_{on,dyn}$ increases more than twice the static value when an off-state drain bias of

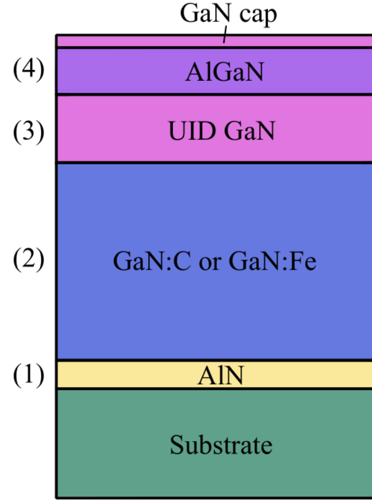

Figure 2.1. A conventional AlGaN/GaN heterostructure with a thick C-doped or Fe-doped buffer layer.

600 V is applied [54], which is an unacceptably high increase of $R_{on,dyn}$. However, Würfl et al. showed that HEMTs with Fe-doped buffers display lower $R_{on,dyn}$ dispersion than HEMTs with purely C-doped buffers [26].

Carbon is usually incorporated into GaN by changing the growth conditions in the MOCVD reactor [55]. However, increasing the C concentration using this approach can lead to poorer crystal quality by introducing more extended defects. A less common technique is to introduce a separate carbon precursor gas, such as propane or methane, together with the Ga and N precursor [56]. The carbon atoms substitute both Ga sites (C_{Ga}) and nitrogen sites (C_N) in the GaN crystal. As a result, C_N forms a deep acceptor level with ionization energy of 0.9 eV above the valance band edge (E_v) [57], and C_{Ga} forms a shallow donor level. At high carbon concentrations, the semiconductor becomes semi-insulating since the C_N acceptors compensate the C_{Ga} donors and other donors in the crystal. Carbon doping is typically preferred over Fe doping in power switching HEMTs due to the high ionization energy of C_N, which leads to a higher resistivity and breakdown fields [26].

Carbon concentrations above 10^{19} cm^{-3} are typically needed to achieve sufficiently good isolation for power electronic devices. This enables vertical breakdown fields up to 2.3 MV/cm [21]. On the other hand, the GaN buffer becomes p-type at high concentrations due to the acceptor-like nature of C_N [58]. The p-n junction formed between the 2DEG and the buffer leads to a greater $R_{on,dyn}$ dispersion at high drain biases [58]. Eldad et al. reported a large drain current lag for HEMTs with a highly C-doped GaN buffer on SI-SiC at a small drain quiescent of 30 V [25]. A high drain lag dispersion has been seen in other GaN-on-SiC HEMTs with a high C doping concentration as well [24]. Hilt et al. and Würlf et al. both demonstrated that C-doped buffers caused $R_{on,dyn}$ to increase more than two times above the static values

[26], [59]. However, introducing an AlGaN back-barrier between the UID-GaN and the C-doped buffer layer can suppress the $R_{on,dyn}$ dispersion caused by the C acceptors, while maintaining a high lateral breakdown strength [26]. It has also been suggested that $R_{on,dyn}$ can be reduced by employing a stepped carbon profile instead of a sharp transition to the highly C-doped buffer [60]. Moreover, Uren et al. showed that the $R_{on,dyn}$ dispersion can be lessened by intentionally forming dislocation-induced leakage paths between the 2DEG and the traps in the buffer [58]. This allows trapped electrons to charge/discharge from the buffer layer, preventing charge build-up underneath the 2DEG.

In conclusion, incorporating high concentrations of Fe or C in the buffer layer to improve isolation is not without its complications. The growth process required to achieve high doping concentrations can impair the crystal quality. Additionally, the dopant atoms introduce trapping effects, necessitating careful control of the doping concentration, doping profile, or the concentration of dislocations to suppress $R_{on,dyn}$ while maintaining good isolation. A heterostructure that can combine high isolation without introducing deep-level traps would be preferable to the conventional heterostructures.

The 'Buffer-Free' Heterostructure

The negative effects caused by C or Fe can be avoided completely using a novel 'buffer-free' GaN-on-SiC growth technique. With this method, an AlN nucleation layer is grown on top of two intermediate atomic layers consisting of (from the SiC substrate surface) $(Al_{1/3}Si_{2/3})_{2/3+x}N$ and $(Al_{2/3}Si_{1/3})_{1-x}N$ [27]. The out-of-plane compositional gradient and in-plane vacancy ordering of these two layers enable a high crystal quality in the AlN layer. A UID-GaN is then grown on top of the AlN with low dislocation density (~10^8 cm^{-2}) and C concentrations at $3 \cdot 10^{16}$ cm^{-3}, without any intermediate resistive buffer layer (Figure 2.2). Removing the thick buffer layer from the heterostructure design also entails a lower thermal resistance between the active region and the SiC substrate, improving the heat dissipation. The thin UID-GaN layer grown on top of the AlN and SiC substrate results in a high electron confinement without additional deep-level traps added to the heterostructure [61]. Furthermore, the confinement can be improved by reducing the thickness of the

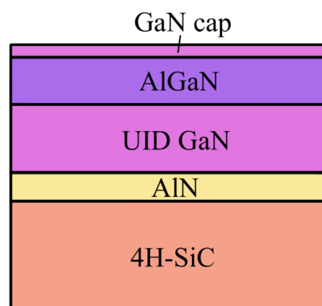

Figure 2.2. A 'buffer-free' heterostructure grown on 4H-SiC. Layer thicknesses are not to scale.

GaN layer. This prevents lateral leakage currents under the depleted channel region during high voltage operations. Moreover, the SiC provides good vertical isolation, suppressing leakage current and preventing vertical breakdown.

Off-State Breakdown Characterization

The breakdown voltage of a semiconductor device is defined as the voltage at which the impact ionization rate of charge carriers approaches infinity (avalanche breakdown), which leads to a rapid increase in current. However, it is more convenient for measurements to set an upper limit to the off-state current(s). The voltage at which this current criterion is exceeded at any terminal is defined as the breakdown voltage. This typically occurs through (a) a hard (or destructive) breakdown, where a sudden current surge exceeds the breakdown current criterion and destroys the device in the process, (b) a soft (or non-destructive) breakdown caused by a current surge through some unintentional current path, and (c) a soft (or non-destructive) breakdown where a raised leakage current exceeds the current criterion. In literature, the two commonly used breakdown criteria are 1 mA/mm, and 1 μA/mm for HEMTs [19], [20], [62]–[65]. In [Paper A], the lower criterion was employed to compare the 'buffer-free' HEMTs with HEMTs found in the literature. However, in this thesis, the 1 mA/mm current criterion is primarily utilized to explore the impact of different processing parameters on the catastrophic breakdown, which requires a higher tolerance for off-state current in some devices.

2.1 Device Fabrication

MISHEMTs were fabricated on a 'buffer-free' III-nitride heterostructure. The general outline of the device fabrication process will be presented in this subsection. However, individual process variations will be presented in subsections where it becomes relevant.

The 'buffer-free' heterostructure was grown using MOCVD by SweGaN AB, utilizing their QuanFINE® concept. The III-nitride stack consists of (from bottom to top layer) a 43 nm AlN nucleation layer, a 265 nm GaN layer, a 18.5 nm $Al_{0.22}Ga_{0.78}N$ layer, and a 2.5 nm GaN capping layer (Figure 2.3a). The substrate is a 500 μm thick high purity SI-SiC. The mobility and carrier concentrations were measured to 2018 cm^2/Vs and $7.1 \cdot 10^{12}$ cm^{-2} using contactless Hall measurement.

A schematic of the fabrication process flow and a top view microscope image of a completed MISHEMT can be seen in Figure 2.3a, and Figure 2.3b, respectively. The general process flow can be divided into six steps and are as follows:

1. The sample is immersed in $(NH_4)_2OH$:H_2O 1:10 (SC1) and HCl:H_2O 1:10 (SC2) to remove organic and metallic contaminants, respectively. Afterwards, a 100-177 nm SiN_x layer is grown using LPCVD. Variations in the SiN_x stoichiometry will be presented in section 2.4 and is a part of [Paper B].
2. A gate recess is defined using photolithography and NF_3-based dry etching to remove SiN_x in the developed gate lithography openings. This step defines the gate length of the HEMT. Gate lengths of 2-4 μm were included in the device design. An additional standard cleaning (SC1 and SC2) process is

implemented, followed by an LPCVD deposition of a ~40 nm stoichiometric SiN_x, which acts as a gate insulator.

3. Recess-etched ohmic contacts is formed. A Ta/Al/Ta metal stack is deposited using a physical vapor deposition (PVD) system with the same resist etch mask preserved (self-aligned process). A more detailed description of the ohmic process will be presented in section 2.2. This step also defines the gate-source distance (L_{gs}) and L_{gd}. In this work, all HEMTs have a L_{gs} of 2 μm and a L_{gd} between 12 μm and 25 μm.
4. The active area is defined. A thick photoresist is spun, baked, exposed and developed. After development, the resist protects the ohmic metal and the source-drain regions. The SiN_x gate dielectric and passivation layer is dry-etched using an NF_3-based plasma, exposing the GaN cap layer. Afterwards, nitrogen implantation is employed. This act to electrically isolate the area surrounding the source, gate and drain contacts. Additional information on nitrogen implantation process will be presented in section 2.3.
5. A metal stack consisting of Ni/Pt/Au/Ti is deposited in the gate recess using a PVD system. In the same lithography step, a gate-integrated field plate is included. The lengths of the field plate (L_{gfp}) were designed to 0.75-5 μm in this work.
6. A 600 nm SiO_x layer is deposited using a plasma-enhanced chemical vapor deposition (PECVD) system. Afterwards, dielectric vias at the drain and source contacts are dry etched using a CHF_3-based plasma. Lastly, a Ti/Au source connected field plate was deposited. Source field plate lengths (L_{sfp}) between 0 μm and 5 μm were designed.

Results for mesa-isolated HEMTs are also presented in this thesis. When this isolation technique is employed, the SiN_x gate dielectric and passivation layers are deposited after the mesa etch to prevent the gate metal from directly contacting the sidewall formed by the etch. The ohmic metal is deposited after the mesa isolation.

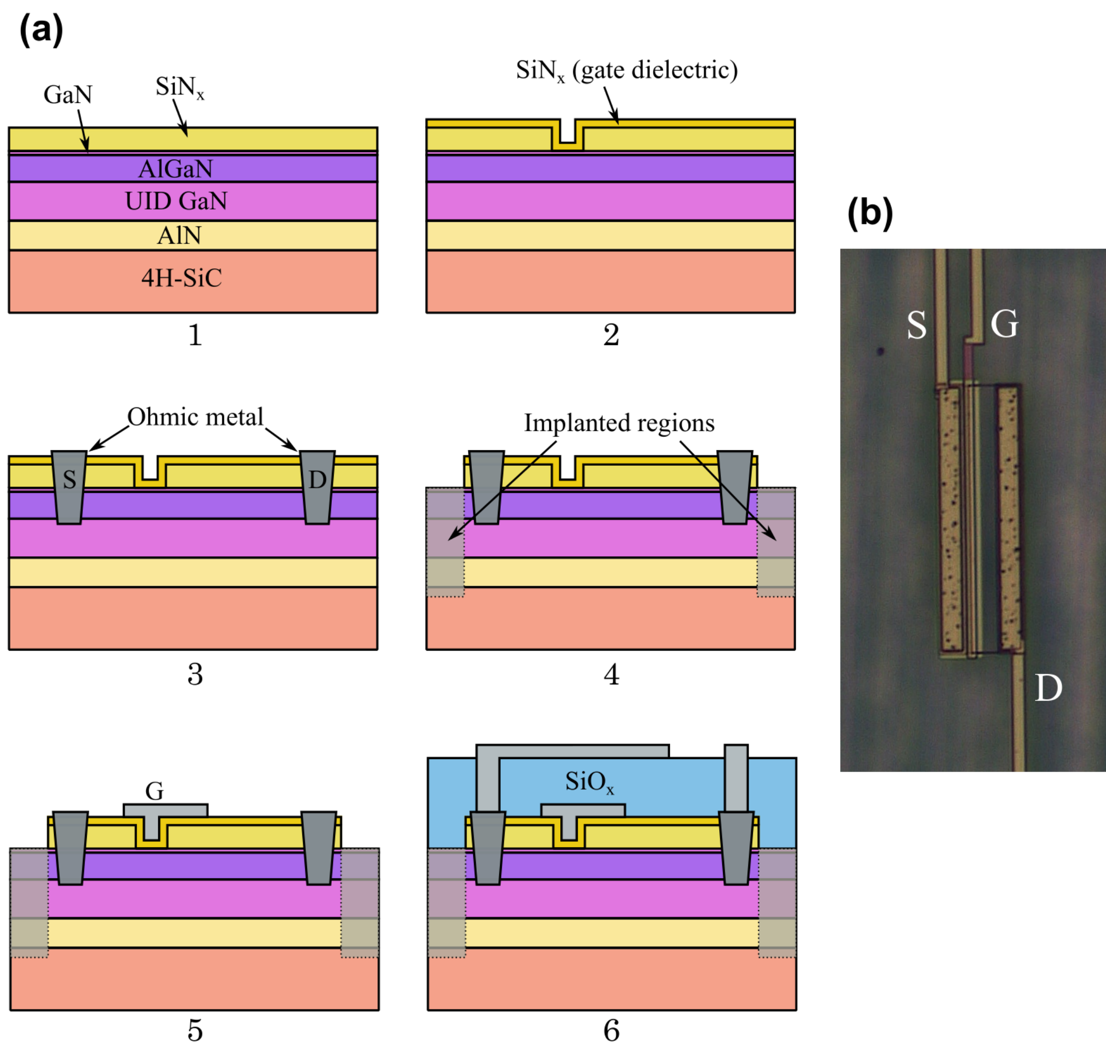

Figure 2.3. (a) Schematic of the fabrication process of MISHEMTs on a 'buffer-free' heterostructure. (b) A top view microscope image of a MISHEMT.

2.2 Ohmic Contacts

A power electronic switch dissipates power when it (a) transitions between its two operating states (switching losses) and (b) when it's conducting current (on-state losses). The on-state losses depend on the series resistances in the channel and between the semiconductor and the metal (Equation 2.2).

$$P_{on} = D \cdot I_{on}^2 \cdot R_{on} = D \cdot I_{on}^2 \cdot (R_{2DEG} + 2R_c) \tag{2.2}$$

where D is the duty cycle, I_{on} is the on-state current, R_{2DEG} is the resistance intrinsic to the 2DEG, and R_c is the contact resistance (Figure 2.4). The on-state resistance is primarily reduced by increasing the electron mobility in the channel, increasing the 2DEG carrier concentration, or by downscaling the component. However, achieving good ohmic contacts is essential for the transistor to function properly. Rectifying contacts can cause R_c to become the dominating term in Equation 2.2, resulting in large on-state power dissipation. This becomes even more crucial in low voltage classes, where 10-15% of the total on-resistance consists of the contact resistances from the source and drain contacts.

In GaN devices, it is more difficult to achieve contact resistances in the same range as Si due to the large bandgap of GaN [66]. Ti/Al-based ohmic contact metallization deposited directly on the barrier (or capping layer) surface is the most common approach for AlGaN/GaN HEMTs [67]–[69]. However, this technique requires post-deposition annealing temperatures of 700-890 °C [69], making it less suitable to use in conjuction with temperature-sensitive processing steps, such as implantation isolation and after deposition of Schottky gate metals.

In the development of the MISHEMTs for [Paper A-B], a Ta/Al/Ta metallization technique was used [70], [71]. Prior to metal deposition, a recess etch is performed to remove the AlGaN barrier (Figure 2.4). This enables low R_c using post-deposition annealing temperatures of 550-575 °C. Ta-based metallization also provides good surface morphology, sharp edge acuity and stability over time [71]. In addition,

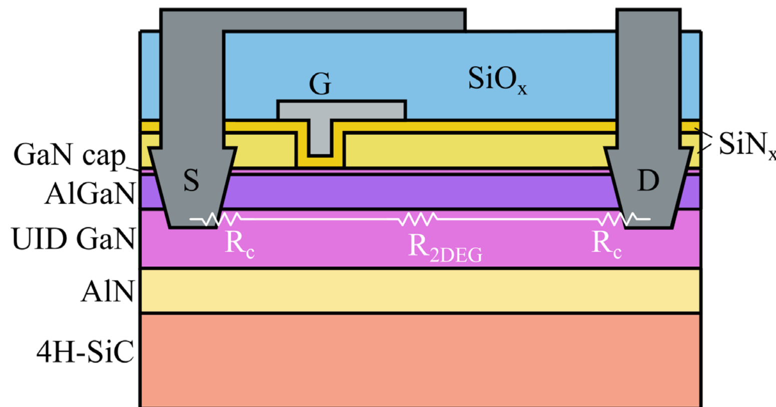

Figure 2.4. A schematic of a MISHEMT with all on-state resistances included. Lengths and layer thicknesses are not to scale.

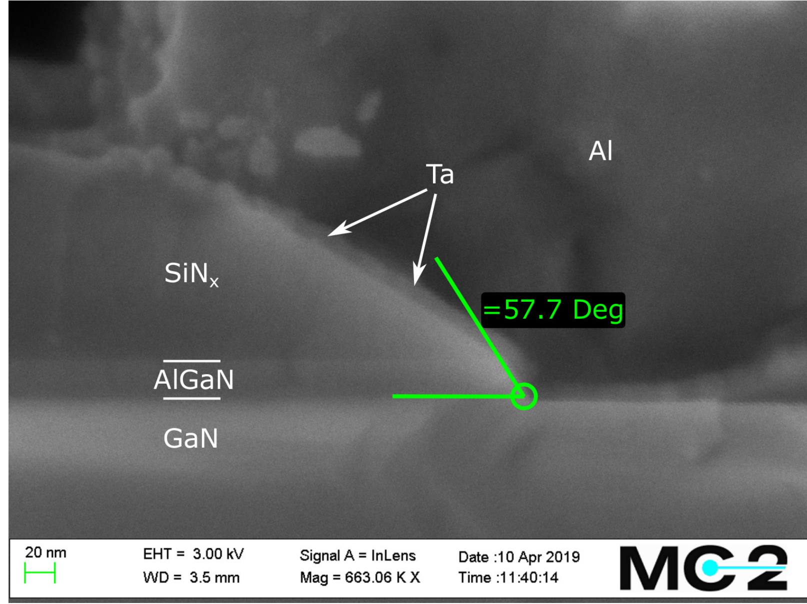

Figure 2.5. A cross-section scanning electron microscope image of a recess-etched Ta-based ohmic contact.

complications related to purple/white plague is avoided by excluding Au from the metal stack.

In this Ta-based metallization method, the photoresist acts as an etching mask and a lift-off resist for the metal (self-aligned process). The recess etch creates an inclined sidewall that facilitates contact between the bottom Ta layer and the 2DEG (Figure 2.5). After metal deposition, a Schottky barrier is naturally formed at the metal-semiconductor interface. This results in highly resistive, rectifying contacts. The rectifying behavior is effectively suppressed by annealing the sample at a sufficiently high temperature. This is thought to cause an out-diffusion of nitrogen atoms in the direct vicinity of the Ta/Al, which then forms TaN and AlN [70], [71]. The nitrogen vacancies left behind as a consequence of the migrating nitrogen atoms act as a thin, highly doped n-type layer. This, in turn, reduces the extent of the depletion region formed by the Schottky contact, which promotes electron tunnelling through the Schottky barrier. The elevated electron tunnelling results in an ohmic behaviour with low contact resistance. The relation between contact resistance and doping concentration in the semiconductor adjacent to the metal is given by

$$R_c \propto e^{\frac{\phi_B}{E_{00}}}, \qquad E_{00} \propto \sqrt{N_d} \tag{2.3}$$

where ϕ_B is the Schottky barrier height, and N_d is the doping concentration close to the metal. Metals with low work functions are therefore preferable since they result in lower barrier heights. Ta and Ti exhibits work functions of 4.25 eV and 3.95 eV, respectively [72]. According to Uryu et al., the ohmic contact formation is not caused by a high donor density at the GaN surface [73]. Instead, the strain induced in the AlGaN barrier caused by the Ta/Al/Ta metal stack results in a change of the

polarization in the barrier, which leads to an effective doping concentration. This polarization-induced doping consequently increases the field emission between the metal and semiconductor, leading to a reduction of the contact resistance.

The fabrication of recess-etched Ta-based ohmic contacts started after the deposition of SiN_x passivation and gate dielectric. Next, an AZ5214 image reversal photoresist was spun, soft-baked, exposed, reversal baked, flood exposed and lastly developed. The resist profile determines the inclination of the sidewall after the dry etch recess [70]. An Oxford Plasmalab 100 ICP/RIE system was used for dry etching the SiN_x passivation in a fluorine-based plasma. The AlGaN barrier and ~10 nm of the UID-GaN layer were etched in a chlorine-based plasma. After the recess etch, the samples were immersed in a buffered oxide etch (BOE:H_2O 1:10) for 4 min, and a hydrochloric acid etch (HCl:H_2O 1:10) for 1 min prior to metal deposition. A metal stack consisting of 20/280/20 nm Ta/Al/Ta was deposited using a Lesker Spectros evaporator. Lastly, the ohmic contacts were annealed in an AccuThermal AW610 RTP system. The temperature of each annealing run was kept at 575 °C, and the annealing time varied between 1-8 min. All annealing steps were performed in a nitrogen ambient.

Contact resistances and sheet resistances were extracted using the transfer length method (TLM). With this method, the total resistance is calculated between two ohmic contacts with varying contact separations. The two components comprising the total resistance can be extracted through a linear extrapolation using the expression

$$R_{tot} = R_s L + 2R_c \qquad [\Omega \cdot mm] \tag{2.4}$$

where R_{tot} is the total resistance, R_s is the sheet resistance, and L is the contact separation. Both R_s and R_c were obtained after each annealing run. The annealing and TLM measurements were repeated for an aggregated time of 50-70 min. The contact resistance decreases and approaches a value of 0.44-0.47 Ω·mm as the total annealing time is increased (Figure 2.6a). The sheet resistance shows a similar trend and reaches a value of 421 Ω/sq (Figure 2.6b), indicating that it is not negatively affected by the long annealing times. The contact resistance presented here is higher than what has been reported for other Ta-based, recess-etched, ohmic contacts (0.21-0.36 Ω·mm) [70], which means further optimization of Ta layer thickness, annealing temperature, recess depth, and recess sidewall angle is needed. Nevertheless, Ta-based contacts display lower contact resistance compared to most other Ti/Al-based contacts used for high voltage AlGaN/GaN HEMTs in literature (Table 2.2).

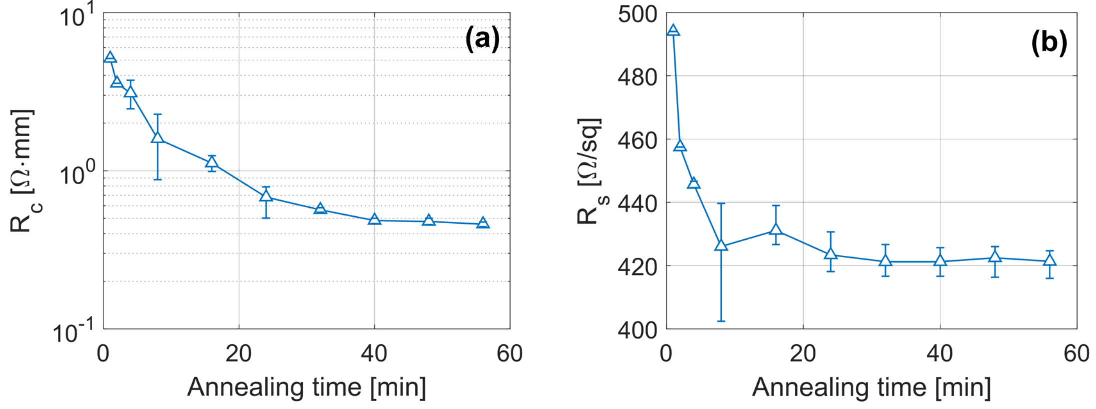

Figure 2.6. (a) Contact resistance, and (b) sheet resistance as functions of total annealing time in the left and right figures, respectively.

Table 2.2. Examples of ohmic contacts for high voltage AlGaN/GaN HEMTs in literature.

Reference	Metal stack	Annealing temperature [°C]	R_c [Ω·mm]
This work	Ta/Al/Ta	575	0.44-0.47
[17]	Ti/Al/Ni/Au	N/A	~1
[65]	Ti/Al/Ni/Au	875	1.4
[74]	Si/Ti/Al/Mo/Au	800	0.5
[75]	Ti/Al/W	N/A	0.93
[76]	Ti/Al/Ni/Au	890	1.12
[77]	Ti/Al/Ni/Au	875	0.35
[78]	Ti/Al/Ni/Au	870	0.6

2.3 Electrical Isolation

It is necessary to electrically isolate the area surrounding the active part of the device so that the gate can maintain control of the off-state current. Moreover, the critical electric field of the isolated regions must be as high as possible to prevent impact ionization and catastrophic failure at the edge of the gate contact. In general, there are two ways to achieve electrical isolation: (a) mesa isolation, or (b) implantation isolation. In this work, both isolation techniques have been studied for 'buffer-free' heterostructures.

The mesa isolation technique lowers the lateral conductivity by physically removing the AlGaN/GaN heterostructure and, therefore, the 2DEG. The resistivity is then determined by the bulk resistivity in the etched layer. In the 'buffer-free' heterostructure, the mesa isolation can be subdivided into two categories: (i) a trench that is etched down into the thin UID-GaN layer, and (ii) a trench that is etched down to the SiC substrate. The purpose of subdividing the two mesa structures is to characterize the electrical isolation of the UID-GaN and SI-SiC separately for this epitaxial design. Both mesa isolation types were tested. The mesa structures were formed with an Oxford Plasmalab 100 ICP/RIE system. A Cl_2/Ar-plasma with a platen forward power of 100 W and an ICP power of 50 W etched the AlGaN, GaN and AlN layers. The depth of the GaN-mesa etch was approximately 180 nm, while the SiC-mesa was above 330 nm.

The main advantage of ion implantation is that a planar surface is maintained, which facilitates device processing and improves repeatability. Both light and heavy elements can provide a high resistivity by introducing point defects as a result of implantation damage, or through chemical reaction with the crystal atoms [79]. These defects and ions act as trapping centers, which compensate any preexisting donors in the crystal. A wide variety of ion species have been reported, such as H^+,

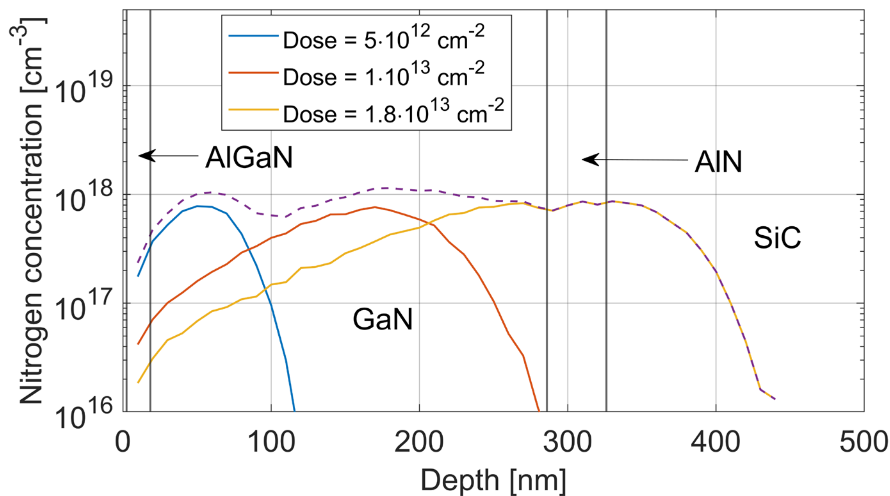

Figure 2.7. SRIM-calculated nitrogen implantation profiles in a buffer-free AlGaN/GaN heterostructure. The dashed purple line is the net concentration of nitrogen ions.

He^+, N^+, Kr^+, Ar^+ and O^+ [80]–[83]. However, N^+-implanted GaN can maintain a stable resistivity at temperatures up to at least 600 °C, making it preferable over other types of ion species [81], [84].

In this study, three N^+ implantation profiles were used. The SiN_x passivation and SiN_x gate dielectric films were deposited prior to implantation due to the high temperatures required ($\geq$ 770 °C) for LPCVD deposition. The N^+ implantation profiles were determined before implantation using the "Stopping and Range of Ions in Matter" (SRIM) software [85]. Three implantations were required to completely cover the depth of the AlGaN barrier and GaN channel with nitrogen atoms. The energy and doses for the three implantations used were 30 keV and $5 \cdot 10^{12}$ cm^{-2}, 100 keV and $1 \cdot 10^{13}$ cm^{-2}, 180 keV and $1.8 \cdot 10^{13}$ cm^{-2}, respectively. Their respective implantation profile can be seen in Figure 2.7 together with the total concentration of nitrogen ions.

2.3.1 Two-Terminal Breakdown

The measurement structures to test the three different isolation techniques consists of two separated ohmic contacts (Figure 2.8), with distances between the contacts varying from 5-25 µm. The area between the contacts is isolated using N^+ implantation or mesa isolation. A voltage is applied between the two contacts and is swept from 0 V up to the maximum voltage of 3 kV with a step of 2 V. In the following results, only the destructive breakdown of the device has been considered.

In Figure 2.9a, the breakdown voltage is displayed for contact separations between 5-25 µm for the three isolation techniques. The SiC trench isolation provides superior isolation compared to the shallow GaN trench isolation. Although GaN has a larger bandgap and a higher breakdown field compared to SiC in theory, it is likely that the lower breakdown voltages seen for the GaN trench isolation is due to the incorporation of donor-like impurities such as O or N-vacancies during the MOCVD growth. This consequently leads to a lower resistivity, which also explains why the leakage current is higher for the GaN trench samples (Figure 2.9b). Moreover, surface defects formed during the Cl-based dry etching could contribute more to the elevated leakage current in the GaN mesa isolation sample [86].

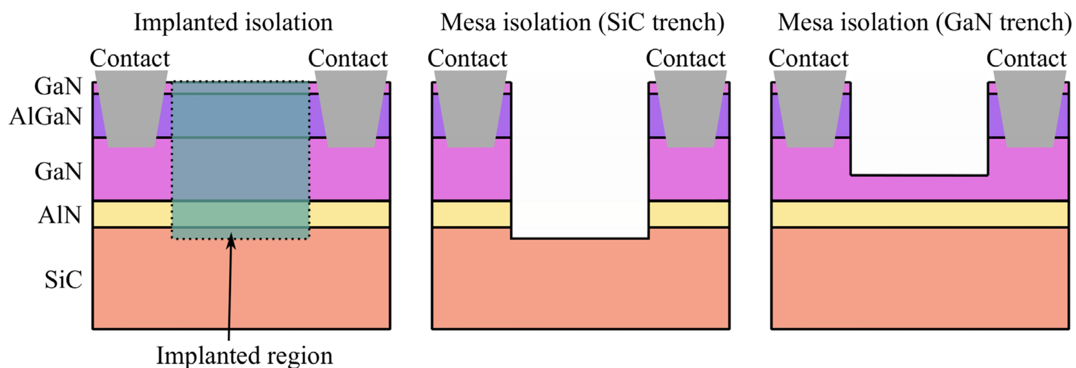

Figure 2.8. Schematic of implantation isolation and mesa isolation test structures. Dimensions are not to scale.

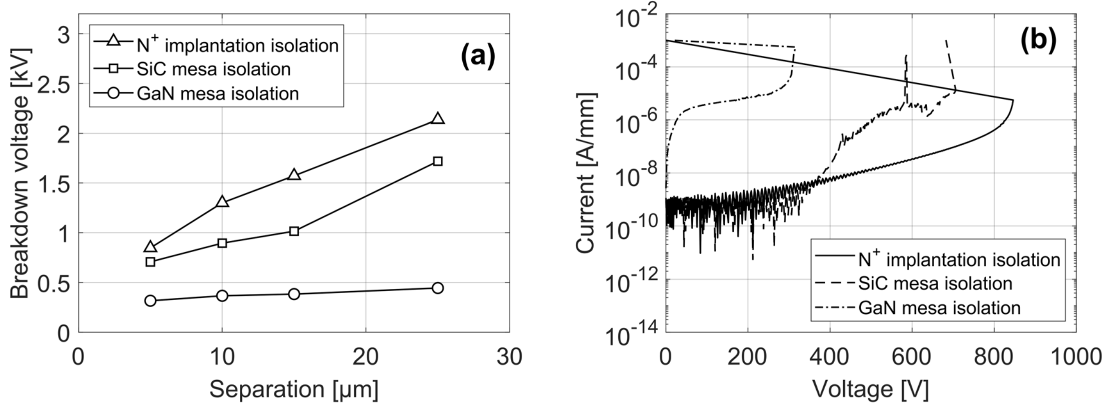

Figure 2.9. (a) Destructive breakdown voltage for mesa and nitrogen implantation isolation structures with separations between 5 μm and 25 μm. (b) Current-voltage characteristics of an isolation structure with a 5 μm separation for mesa and nitrogen implantation isolation.

The planar isolation structures with implanted N^+ tended to have the highest breakdown voltages and the lowest leakage currents for all contact separations. Both the N^+-implanted sample and the SiC-etched mesa isolation sample can suppress the leakage current to sub-nA/mm levels under biases of 350-700 V (depending on the separation). However, at higher voltages, the leakage increases by at least two orders of magnitude for the SiC-etched mesa isolation, which means that the SiC substrate is less resistive and has a lower breakdown field than implanted GaN. Also, the electric field tends to concentrate at the corners of the mesa trench [19], leading to a lower breakdown due to the smaller bandgap of SiC. By contrast, in the planar isolation structures, the peak electric field tends to concentrate at the edge of the ohmic contacts, where the properties of the implanted GaN limit the breakdown voltage. Similar to the GaN trench isolation, the Cl_2/Ar plasma may have affected the SiC surface by introducing additional leakage paths at the surface. For these reasons, the highest breakdown voltage for the SiC trench isolation sample is limited to ~1700 V at 25 μm. On the other hand, the N^+-implantation can sustain voltages up to ~2100 V, making it more suitable for high voltage HEMTs.

The N^+-implanted sample was intentionally annealed using an AccuThermal AW610 rapid thermal processing (RTP) system to test its temperature stability. The sample was annealed at six different temperatures in the 300-600 °C range for 10 min each. The average leakage current between 150 V and 200 V for a 5 μm contact separation is shown in Figure 2.10. No significant change in leakage current can be observed. The current remains at the nA/mm current level up to 600 °C, which is consistent with what has been reported elsewhere [81], [84].

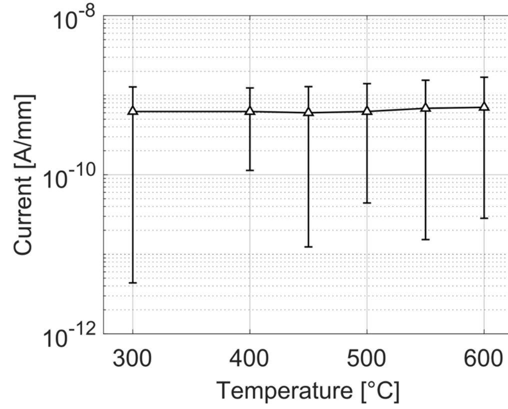

Figure 2.10. Leakage current through the nitrogen implanted GaN sample between 150 V and 200 V (errorbars indicate variation in noise) after annealing the sample at 300-600 °C. The separation between the contacts is 5 μm.

2.3.2 Three-Terminal Breakdown

In this section, MISHEMTs with mesa isolation and N^+ implantation isolation are compared. The results presented in the figures in this section are measured on MISHEMTs with a Si-rich LPCVD SiN_x passivation and L_g, L_{gd}, L_{gfp} and L_{sfp} of 4 μm, 12-25 μm, 0.75 μm, 0 μm, respectively.

In Figure 2.11a, the subthreshold characteristics measured at V_{ds} = 40 V are shown for the samples with SiC trench isolation and N^+ implantation isolation. The off-state drain and gate leakage current in the SiC trench isolation is higher by a factor of 2-3. However, at high V_{ds}'s, the difference increases, and the leakage currents are higher by up to a factor of 6 (Figure 2.11b). In addition, catastrophic breakdown occurs at 1187 V and 2201 V in MISHEMTs with mesa isolation and N^+ implantation, respectively (L_{gd} = 20 μm in both devices). This shows that the N^+ implantation isolation is superior to SiC in limiting off-state leakage currents and increasing the maximum destructive breakdown. Moreover, damage formed by the Cl_2/Ar etch could have created extra leakage paths along the mesa sidewall or at the SiC trench (Figure 2.11c). Etch-induced leakage paths have been observed in both GaN diodes and in AlGaN/GaN HEMTs [87]–[89]. For these reasons, N^+ implantation was used instead of mesa isolation when fabricating devices for [Paper A-B].

Breakdown voltages of MISHEMTs and isolation structures with varying L_{gd} / contact separation for SiC trench isolation and N^+ implantation isolation can be seen in Figure 2.11d. Overall, MISHEMTs with N^+ implantation display higher off-state breakdown voltages for all L_{gd} compared to SiC mesa isolation. A three-terminal breakdown between 1480 V and 2496 V was achieved for L_{gd} = 12-25 μm, corresponding to breakdown fields (BV/L_{gd}) between 123 V/μm and 0.98 V/μm. The SiC isolation limits the two-terminal and three-terminal breakdown, where breakdown fields below 80 V/μm could be obtained. Similar to the N^+ implantation devices, the breakdown field tend to decrease with increasing L_{gd}. Furthermore, the

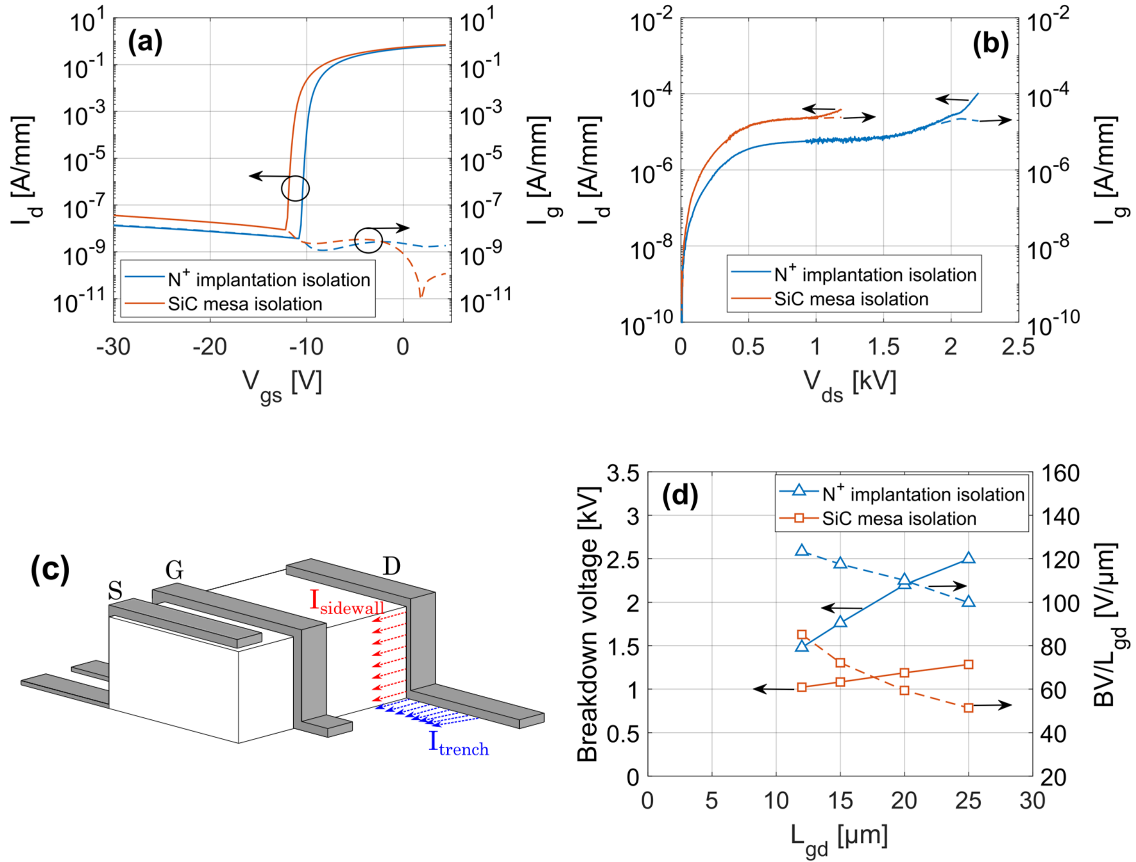

Figure 2.11. (a) Subthreshold characteristics MISHEMTs with a SiC mesa isolation and N^+ implantation isolation. (b) Off-state breakdown characteristics for MISHEMTs with a SiC trench isolation and N^+ implantation isolation and L_{gd} = 20 µm. (c) Schematic displaying potential leakage paths in a MISHEMT with mesa isolation. (d) Off-state destructive breakdown voltage and breakdown field of MISHEMTs with N^+ implantation and SiC mesa isolation with different L_{gd}.

difference in breakdown voltage for the SiC-etched MISHEMTs and the SiC-etched isolation structures is less than 100 V for most L_{gd}/contact separations. This indicates the same type of breakdown mechanism, which is probably caused by current paths formed at the mesa sidewall, at the SiC trench surface or in the SiC bulk material.

To conclude, N^+ implantation is the best technique to improve isolation, increase the breakdown field, and reduce the number of unintentional leakage paths induced by etching or other device processing steps. Additionally, the breakdown field could be further improved by increasing the implantation dose. Sun et al. used a higher N^+ dose for HEMTs with a C-doped buffer and could achieve a breakdown voltage of 1.8 kV at L_{gd} = 10 µm, but was limited to voltages below 2 kV due to vertical leakage current through the GaN buffer and Si substrate [19]. The 'buffer-free' HEMTs used in this work is not limited by vertical leakage currents. Therefore, it could be possible to obtain breakdown voltages above 2 kV with an L_{gd} above 12 µm. Although N^+ implantation can significantly improve the insulating properties of

GaN, leakage currents in the MISHEMT are two orders of magnitude higher than the two-terminal measurements. This means that the passivation layers, gate dielectrics and field plate need to be improved to reduce leakage currents and increase the breakdown voltage futher.

2.4 Passivation Layer

The passivation layer in GaN-based HEMTs has two major functions: (a) to protect the barrier layer (e.g. AlGaN) or capping layer surface from damage and adsorption of contaminants during the device processing, and (b) to reduce negative surface-related trapping effects [90], [91]. The choice of passivation is also important since different passivation affects the barrier surface – and therefore the electron transport properties – differently. One of the most popular passivation layers is SiN_x due to its positive effects on channel carrier concentration and suppression of interface states and surface traps [92]–[95].

In general, SiN_x is deposited using LPCVD, PECVD, or *in situ* MOCVD. The choice of deposition techniques has a large impact on device performance. LPCVD-SiN_x displays a lower concentration of surface traps, higher interface quality, and lower leakage currents than PECVD-SiN_x [96], [97]. MOCVD enables SiN_x deposition without exposure to air or any contaminants (e.g. resist residues). Additionally, MOCVD-SiN_x effectively reduces both leakage currents and $R_{on,dyn}$ dispersion [98]. However, MOCVD-SiN_x has not yet been optimized for the type of heterostructures studied in this work. Therefore, LPCVD becomes the preferred choice.

SiN_x passivation layers with varying stoichiometries have been reported. Stoichiometric SiN_x passivation layers tend to be more resistive compared to Si-rich SiN_x, but have been associated with higher $R_{on,dyn}$ [29]. Highly resistive passivation layers are preferable for high voltage devices since the electric field tends to concentrate at the edge of the gate at high voltages, leading to a high gate leakage current and a premature destructive breakdown. Therefore, the stoichiometry of the SiN_x has to be optimized to achieve a low $R_{on,dyn}$ dispersion while maintaining a low gate leakage current.

In [Paper B], two types of LPCVD SiN_x passivation layers are compared in terms of their impact on off-state leakage currents at high voltages in 'buffer-free' MISHEMTs. The two films were grown with different growth temperatures, reactant gas flow ratios, and deposition times, which resulted in a difference in thickness and stoichiometry. The reactant gases used in this LPCVD system are dichlorosilane (DCS) and ammonia (NH_3). One layer was grown with a high Si content, while the other was grown to have a 3/4 ratio between Si and N (stoichiometric passivation). The Si-rich SiN_x layer was deposited at a temperature of 820 °C, a pressure of 250 mTorr, and a DCS/NH_3 ratio of 224/23 sccm, while the stoichiometric SiN_x was deposited at a temperature of 770 °C, a pressure of 250 mTorr and a DCS/NH_3 ratio of 98/360 sccm. Ellipsometry was used to estimate the stoichiometry of the films. A refractive index of 2-3 is typically seen for Si-rich films, while stoichiometric films have a refractive index of 2 [99]. The Si-rich and

stoichiometric films used in this study had a refractive index of 2.38 and 2.02, respectively. Additionally, the resulting thicknesses of the Si-rich and stoichiometric passivation layers were 177 nm and 100 nm, respectively.

A leakage test structure was fabricated (Figure 2.12a-b) [100]. This test structure consists of three terminals: a terminal connected to the 2DEG through an ohmic contact, and two terminals connected to the MIS structure formed by the gate metal, SiN_x gate dielectric and GaN/AlGaN surface. The ohmic contact and one of the MIS-structure (the guard) are grounded, while the second MIS structure (the gate) has a negative bias applied to it. The current to the guard and gate terminals are monitored as the gate bias is ramped down from 0 V to -150 V. This test structure makes it possible to separate surface/interface-related leakage currents and leakage currents through the gate dielectric and barrier by observing the difference in the magnitude of the two leakage components. The separation between the gate and guard contacts is 10 μm in this test.

In Figure 2.12c, the two leakage components are shown for a sample with a Si-rich SiN_x passivation layer. Both the gate and guard currents can maintain a current at (or below) the measurement limit (~100 pA) of the system between 0 V and -40 V. However, when the gate bias decreases from -40 V to -150 V, the gate

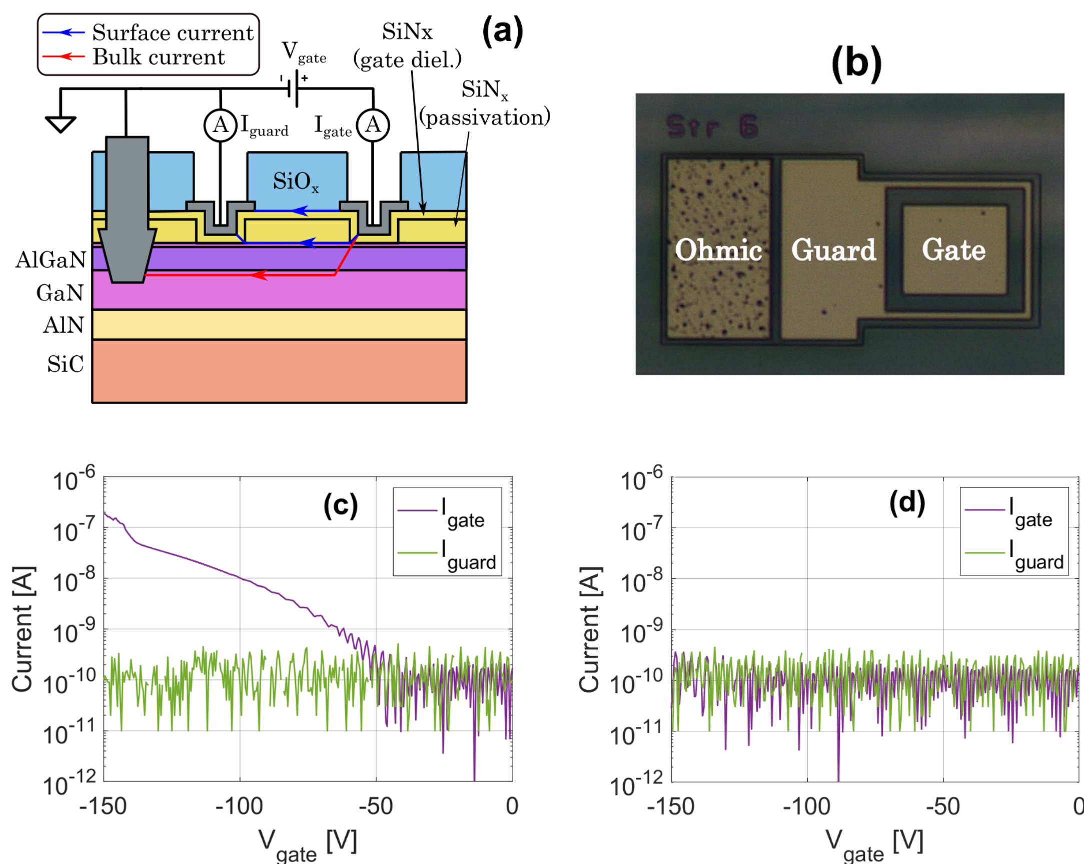

Figure 2.12. (a) Cross-section schematic of a leakage test structure. (b) Microscope image of a leakage test structure. (c-d) Leakage test structure results with (c) a Si-rich SiN_x passivation layer and (d) a stoichiometric SiN_x passivation layer [Paper B].

current increases by more than three orders of magnitude. In contrast, the guard current remains at (or below) the detection limit throughout the rest of the measurement interval. This implies that most of the leakage current flow from gate-to-2DEG through the SiN_x gate dielectric, passivation, and AlGaN barrier to the ohmic contact. On the other hand, the stoichiometric SiN_x passivation maintains a sub-nA guard and gate current in the whole measurement interval (Figure 2.12d), which is up to three orders of magnitude lower compared to the gate leakage current in the Si-rich SiN_x passivation.

The impact of SiN_x stoichiometry on off-state characteristics of the MISHEMTs is seen in Figure 2.13. AlGaN/GaN MISHEMTs with gate lengths of 2 μm and 4 μm were fabricated for the Si-rich SiN_x and stoichiometric SiN_x, respectively. Gate-source distance, gate-drain distance, source field plate length, gate field plate length and gate width were designed to 2 μm, 20 μm, 5 μm, 4 μm and 100-200 μm, respectively. Nitrogen implantation was used as isolation in both samples.

The gate and drain current were measured as V_{gs} was swept from -30 V to 5 V, and V_{ds} = 40 V (Figure 2.13a). At V_{gs} = -20 V, the drain current decreases from ~$4.1 \cdot 10^{-8}$ A/mm to ~$4.7 \cdot 10^{-11}$ A/mm when the stoichiometric SiN_x passivation is employed. The off-state leakage current in MISHEMTs with a Si-rich SiN_x passivation is limited by gate-drain leakage currents, which is likely caused by the poor insulating properties of the Si-rich SiN_x, and not surface/interface currents, as was demonstrated in Figure 2.12c-d.

In Figure 2.13b, the off-state breakdown characteristics of MISHEMTs with Si-rich and stoichiometric SiN_x passivations are shown. The drain and gate current were measured at V_{gs} = -20 V and V_{gs} = -30 V for the stoichiometric and Si-rich passivation layers, respectively. MISHEMTs with a stoichiometric SiN_x passivation layer can maintain a gate leakage current below 10 nA/mm up until breakdown, which occurred at 1622 V ([Paper A]). The drain leakage current increase is likely caused by drain-to-source leakage paths between the source field plate and the drain contact or by current flowing under the depleted region at the gate.

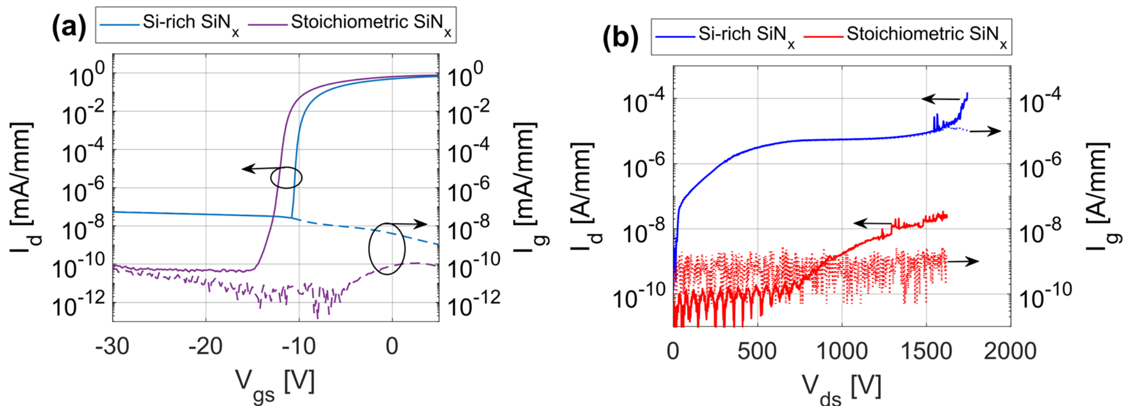

Figure 2.13. (a) Subthreshold characteristics with V_{ds} = 40 V for MISHEMTs with Si-rich and stoichiometric SiN_x passivation [Paper B]. (b) Off-state breakdown characteristics of MISHEMTs with Si-rich and stoichiometric SiN_x passivation [Paper A-B].

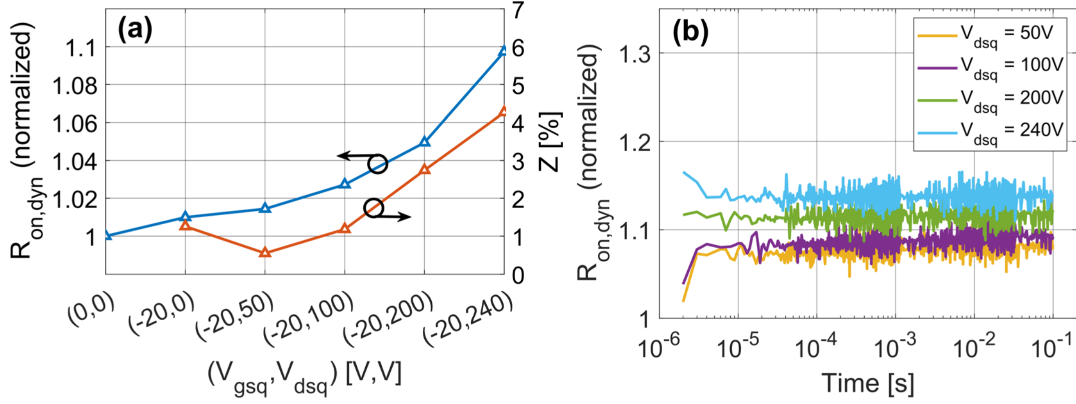

Figure 2.14. (a) $R_{on,dyn}$ and slump ratio at different gate and drain quiescent bias points. (b) Time dependence of $R_{on,dyn}$ after stress at gate quiescent V_{gsq} = -20 V and at different drain quiescent [Paper A].

MISHEMTs with a Si-rich SiN_x passivation layer exhibit an off-state breakdown voltage of 1742 V, but with a significantly higher gate-drain leakage current above 1 μA/mm when V_{ds} increases above 300 V. This increases up to 154 μA/mm until breakdown occurs due to destructive gate-drain breakdown.

Passivation layers with a low Si/N ratio have previously been shown to cause large $R_{on,dyn}$ dispersion in GaN-on-Si HEMTs with C-doped buffer layers [29], [30], [101]. However, this could not be observed for 'buffer-free' HEMTs with gate and source field plates presented in [Paper A]. The normalized $R_{on,dyn}$ increases by up to a maximum of 10% when the drain quiescent voltage (V_{dsq}) increases from 0 V to 240 V (Figure 2.14a). Here, the $R_{on,dyn}$ was calculated using the drain current at V_{ds} = 1 V, V_{gs} = 0 V, and an on/off-state time of 1/99 μs. Furthermore, the slump ratios, defined as

$$Z_g\ [\%] = \left|\frac{I_d(-20\ V, 0\ V) - I_d(0\ V, 0\ V)}{I_d(0\ V, 0\ V)}\right| \cdot 100 \tag{2.5}$$

$$Z_d\ [\%] = \left|\frac{I_d(-20\ V, V_{dsq}) - I_d(0\ V, 0\ V)}{I_d(0\ V, 0\ V)}\right| \cdot 100 \tag{2.6}$$

was calculated using the drain current at V_{ds} = 25 V, V_{gs} = 1 V above the knee in the PIV characteristics. The ratios in Equation 2.5 and 2.6 estimates the decrease in current in the saturation region due to trapping effects (current collapse). The slump ratio Z_g is less than 2% and Z_d increases up to a maximum of 4% at a V_{dsq} = 240 V. In the DCT characteristics (Figure 2.14b), the normalized $R_{on,dyn}$ is 4-7 percentage points higher compared to what can be seen in Figure 2.14a. This is most likely due to a longer stress time (on/off-state time of 100/100 ms). The $R_{on,dyn}$ does not significantly change in the 3 μs - 100 ms interval for any quiescent V_{dsq}. Therefore, traps with time constants above 100 ms are most likely causing the increase in $R_{on,dyn}$ in the Figure 2.14a. A further study of the off-state stress (V_{gsq}, V_{dsq}) and stress time at different temperatures is required better to understand the trapping effects in these heterostructures.

In conclusion, the LPCVD-grown stoichiometric SiN_x is a promising alternative to Si-rich SiN_x for high power MISHEMTs due to its good insulating properties. No large dispersive effects could be seen for the stoichiometric SiN_x passivation in the measured bias range. Additionally, the stoichiometry of the SiN_x does not seem to affect the static R_{on} (calculated using $I_d(V_{ds} = 1$ V, $V_{gs} = 0$ V)) to any significant degree (Figure 2.15a). The difference in R_{on} between the two samples can be attributed to sheet resistance and contact resistance variations between the two samples. MISHEMTs with a stoichiometric SiN_x passivation layer and a 20 µm gate-drain distance display a max current of 752 mA/mm (Figure 2.15b) and a $R_{on,sp}$ of 3.61 mΩ·cm², resulting in a $BV^2/R_{on,sp}$ figure of merit (FOM) of 729 MW/cm², using a breakdown voltage of 1622 V. The FOM is comparable to other HEMTs found in the literature, where values of 524-877 MW/cm² have been reported [20], [64], [102]–[105]. This can also be seen in the $R_{on,sp}$-BV plot in Figure 2.16, where the 1 µA/mm breakdown current criterion has been used instead of the 1 mA/mm criterion. Lastly, two-terminal breakdown voltages of 744-1920 V at contact separations of 5-20 µm indicate that the power FOM could increase to ~1 GW/cm² by optimizing the field plate design and dielectric stack further (Figure 2.17).

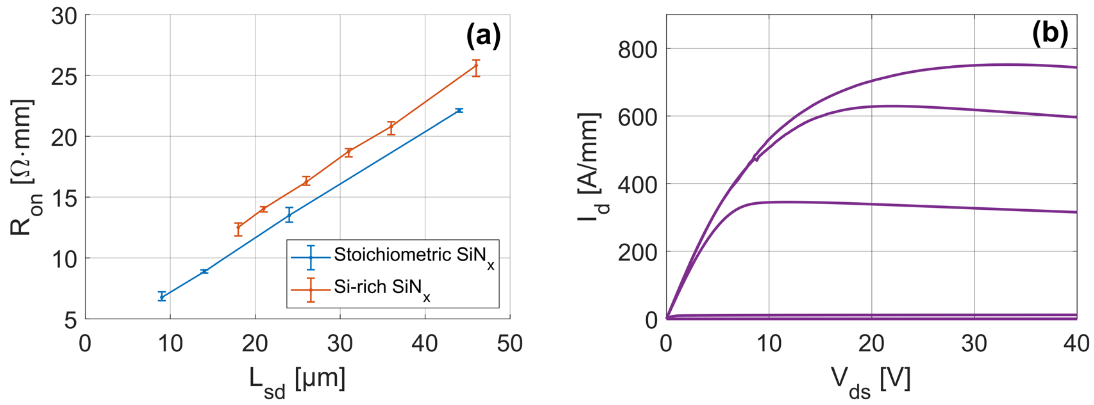

Figure 2.15. (a) Static on-resistance measured at different source-drain separations. Three devices for each sample were used. (b) Output characteristics of MISHEMTs with a $L_{gd} = 20$ µm and stoichiometric SiN_x passivation layer.

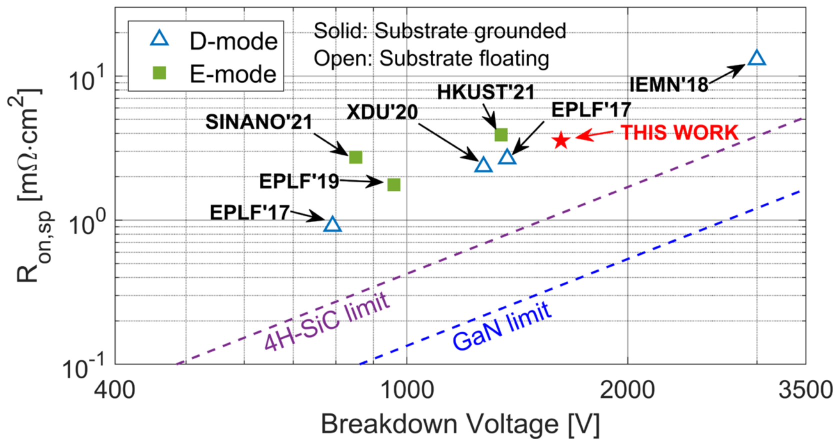

Figure 2.16. $R_{on,sp}$ versus breakdown voltage benchmark, using the 1 µA/mm breakdown criterion [Paper A].

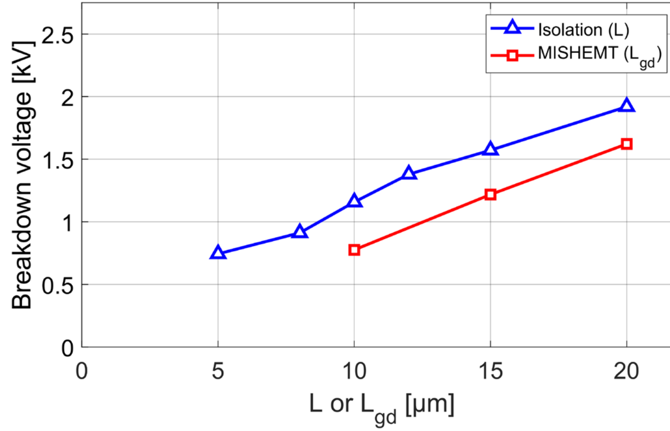

Figure 2.17. Three-terminal breakdown voltage of MISHEMTs with stoichiometric passivation layer and varying L_{gd}. Two-terminal (isolation) breakdown voltage is included as a comparison. The 1 μA/mm current criterion has been used in these measurements [Paper A].

2.5 Gate Dielectric

Designing a HEMT with minimal gate leakage currents is essential to minimize losses and prevent the premature off-state breakdown of the device. A large peak electric field typically causes a high gate current and gate-drain breakdown at the drain side of the gate. Measures to reduce gate leakage involve depositing a high work function metal to form a Schottky barrier, or by depositing a thin intermediate insulating layer between the barrier (or capping) layer and the gate metal. Insulators can provide a larger energy barrier for the electrons compared to a Schottky gate. Moreover, the gate leakage can be further reduced by increasing the insulator thickness. Commonly used gate dielectrics include SiO_x [62], SiN_x [98], [106], and Al_2O_3 [107], [108]. These insulators have a high critical electric field that can withstand the peak field caused by the high drain bias. Gate insulators such as HfO_2 and Ta_2O_5 are less studied for GaN-based HEMTs. The potential advantage of these insulators is their high dielectric constants (high-κ dielectrics) combined with good insulating properties. The high dielectric constant prevents the negative V_{th}-shift, which can be seen in the following relation

$$V_{th} \propto -\frac{t_{in}}{\varepsilon_{in}} \tag{2.7}$$

where t_{in} and ε_{in} represent the thickness and dielectric constants of the gate dielectric, respectively. This allows thicker gate dielectric layers to be grown without significantly decreasing the V_{th}. Moreover, depositing a gate dielectric with a high dielectric constant can be combined with gate recess-etched enhancement-mode HEMTs. For this purpose, it is necessary to have a high-κ gate insulator to prevent V_{th} from becoming negative.

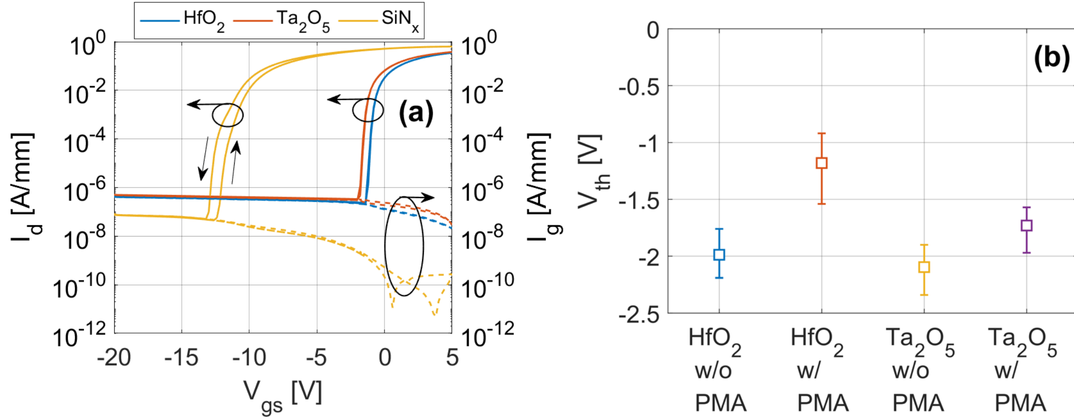

Figure 2.18. (a) Transfer characteristics of MISHEMTs with HfO_2, Ta_2O_5 and SiN_x, (b) Transfer characteristics before and after post-metallization anneal at 375 °C for 12 min for four MISHEMTs with HfO_2 and Ta_2O_5 .

In this work, Ta_2O_5 and HfO_2 are compared with a stoichiometric SiN_x gate dielectric in terms of their impact on gate leakage currents and threshold voltage in MISHEMTs. The oxides were deposited after the deposition and annealing of the ohmic contacts. Both oxides have a thickness of 20 nm and were deposited using an Oxford FlexAI plasma-enhanced atomic layer deposition (PEALD). A post-metallization anneal (PMA) at 375 °C for 12 min was implemented after the gate metal deposition. The SiN_x gate dielectric has a thickness of 40 nm and was deposited using an LPCVD system. Mesa isolation and a Si-rich passivation were utilized for this study.

The transfer characteristics of all three MISHEMTs (L_{gd} = 30 µm, L_g = 4 µm) are shown in Figure 2.18a. The SiN_x gate dielectric display a V_{th} of -12.7-(-11.5) V and gate-drain leakage currents of 60-70 nA/mm range at V_{ds} = 40 V. Gate leakage currents are higher by a factor of 6-7 in the devices with HfO_2 and Ta_2O_5 insulators. This difference could partly be explained by the difference in thickness between the SiN_x, and the two oxides. Annealing the oxides up to 375 °C after gate metallization did not significantly change the gate leakage current. However, V_{th} (measured at ~10 µA/mm) increased from -2 V and -2.1 V to -1.2 V and -1.7 for the HEMTs with HfO_2 and Ta_2O_5, respectively (Figure 2.18b). This shows the impact of high-κ gate dielectrics. In addition, the small hysteresis in MISHEMTs with oxide gate insulators indicates that the trap concentration in the oxides or at the metal-insulator interface is small (Figure 2.18a). The MISHEMT with a SiN_x gate dielectric displays a small-to-moderate negative shift in the reverse sweep direction, which means some positive charges are present at the metal/SiN_x or SiN_x/GaN interfaces.

The three samples' leakage currents at high V_{ds} were also studied. The gate-source voltage was set to -20 V for the devices with SiN_x gate dielectric, and -10 V for the devices with the oxide gate dielectrics, respectively. MISHEMTs used for these measurements were designed with a L_{gd} = 20-30 µm. The predominant leakage mechanism at high voltages in all three samples was gate-drain leakage (Figure 2.19a). MISHEMTs with a SiN_x insulator display the highest breakdown

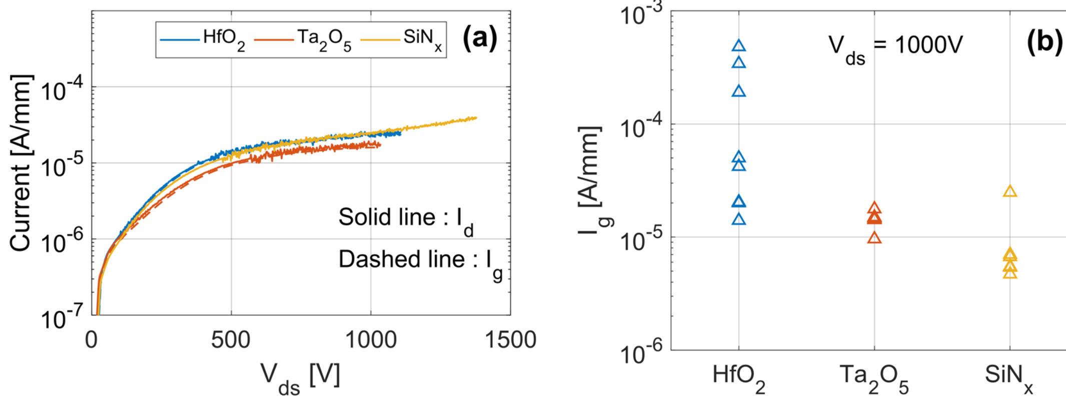

Figure 2.19 (a) Off-state breakdown characteristics of MISHEMTs with HfO_2, Ta_2O_5 and SiN_x gate insulators (L_{gd} = 30 μm). (b) Gate leakage current for eight HEMTs with Lgd = 20-30 μm at measured at V_{ds} = 1000 V in the off state.

voltages and the lowest leakage currents on average (Figure 2.19b). However, the gate current through the Ta_2O_5 is only higher by a factor of 2-3. Moreover, the samples with Ta_2O_5 and SiN_x exhibit a smaller device-device variation. MISHEMTs with a HfO_2 dielectric resulted in the highest gate currents overall and a gate current that varies from 10-500 μA/mm between devices, which worsens the reproducibility.

This study facilitates the development of high voltage enhancement mode MISHEMTs, where the small negative V_{th}-shift resulting from the ALD-grown HfO_2 or Ta_2O_5 can be combined with a partial recess etch into the barrier. This type of technique has been successfully implemented using SiO_2 [20], Al_2O_3 [109] and ZrO_2 [110]. However, it has not yet been seen for ALD-grown HfO_2 or Ta_2O_5. Furthermore, gate leakage currents can be suppressed below 10^{-10} A/mm for $V_{ds} < 100$ V using sputtered HfO_2 [111], which is significantly lower than shown in Figure 2.18a. Therefore, ALD growth parameters could be optimized to achieve higher quality HfO_2.

Realizing high voltage operation with sub-1 μA/mm leakage current requires further reduction of gate leakage current. The gate leakage current is highly dependent on the type of passivation, as was demonstrated in section 2.4. A 2-3 order of magnitude decrease in gate leakage current should be possible by employing stoichiometric SiN_x passivation instead of a Si-rich passivation. However, the gate oxide quality could also be improved by optimizing the PEALD parameters, including Ta and Hf precursor gas flow, chamber temperature and chamber pressure to achieve better insulating properties.

Chapter 3

A New Method to Characterize Short-Channel Effects in GaN HEMTs

Downscaling the gate length of GaN HEMTs is one of the most common approaches when it comes to improving device performance, both in terms of increasing the operating frequency and in terms of reducing the power lost due to the channel resistance [112]. In HEMTs designed for microwave applications, the current gain cut-off-frequency (f_T) and the maximum power-gain cut-off frequency (f_{max}) are affected by L_g reduction through the expressions:

$$f_T = \frac{v_{sat}}{2\pi L_g} = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \quad (3.1)$$

$$f_{max} = \frac{f_T}{2\sqrt{(R_i + R_s + R_g)/R_{ds} + (2\pi f_T)R_g C_{gd}}} \quad (3.2)$$

where v_{sat} is the electron saturation velocity, g_m is the transconductance, C_{gd} and C_{gs} are the gate-drain and gate-source capacitances, and R_i, R_s, R_g, R_{ds}, are the gate-charging, source, gate and output resistances, respectively [113]. However, when the gate length is reduced below 100 nm, SCEs become apparent. These effects cause a reduction of the potential barrier formed under the gate in the off-state due to an applied V_{ds} [114]. In a long-channel HEMT, the energy barrier height reduction at the source side of the gate is typically negligible (Figure 3.1a), leading to a small drain-source leakage current. However, when the gate length is sufficiently short, the voltage applied at the drain contact can influence the barrier height at the source side of the gate (Figure 3.1b). In turn, electrons are capable of surmounting the energy barrier due to thermal excitations, resulting in an increased drain-source leakage current. This manifests as a negative shift of V_{th} in the device's transfer characteristics (Figure 3.1c), which is termed DIBL. The inability of the gate to

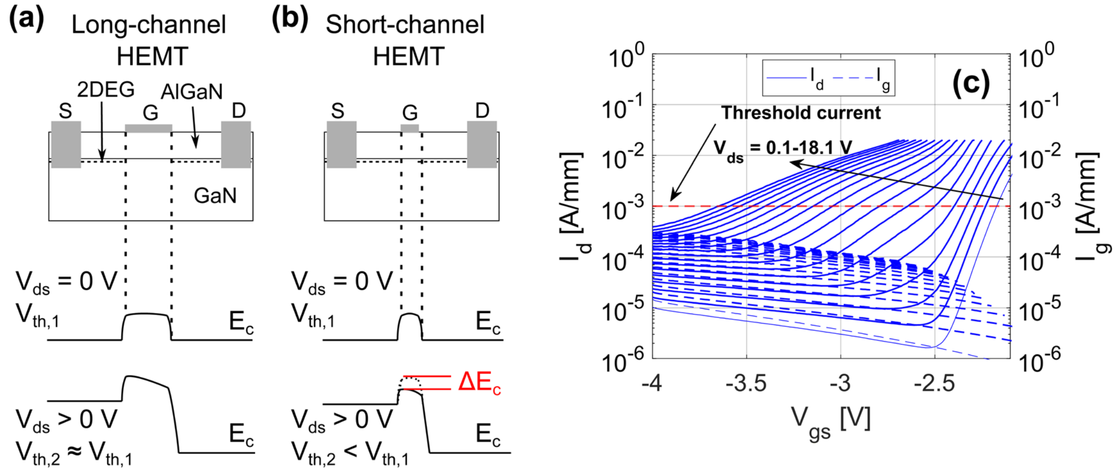

Figure 3.1. A schematic showing the conduction band profile close to the AlGaN/GaN interface at two drain biases for a (a) long-channel HEMT, and (b) short-channel HEMT. (c) An example of the transfer characteristics at different drain biases for a AlGaN/GaN HEMT with L_g = 50 nm.

modulate the electron concentration channel due to SCEs results in a reduction of g_m, which consequently reduces f_T and f_{max} (Equation 3.1-3.2). Additionally, as the V_{ds}-dependence of V_{th} becomes stronger, R_{ds} decreases, leading to a reduction of f_{max}.

In GaN-based HEMTs, DIBL can also be caused by a high leakage current through the buffer underneath the depleted gate region (punch-through) rather than at the AlGaN/GaN interface [115]. It is, therefore, important to increase the resistivity in the buffer layer so that the electron distribution is confined to a small region in the vicinity of the III-nitride interface. Another approach is to improve the electron confinement in the quantum well by incorporating a back-barrier with a larger bandgap (e.g. AlGaN). High electron confinement enables improved gate control, which effectively reduces DIBL. Gate modulation can also be enhanced by employing a lattice-matched InAlN, which enables a reduction of the barrier thickness while maintaining a high sheet carrier concentration [116]. This allows for further L_g reduction in GaN HEMTs.

Additionally, gate length downscaling of power switching HEMTs is necessary to minimize on-state losses. However, this eventually results in increased off-state drain-source leakage current at high voltage due to DIBL/punch-through, which lowers the breakdown voltage set by the breakdown current criteria. This especially becomes a problem in GaN power switching HEMTs operating voltages below 300 V, where L_{gd} is less than 5 µm. In these devices, L_g-downscaling becomes even more important to reduce on-state losses. Optimization of L_g in terms of R_{on} and DIBL requires a measurement technique where V_{th} shifts can be straightforwardly characterized at high voltages.

The Conventional Measurement Technique

When characterizing SCEs, it is common to use two measured transfer characteristics with different V_{ds} (as in Figure 3.1c). The threshold voltage is either defined as V_{gs} at some fixed threshold drain current density ($I_{d,th}$), or at some fixed ratio of the maximum drain current. With two values of V_{ds} and V_{th}, the DIBL parameter (σ) is calculated using

$$\sigma = -\frac{V_{th,high} - V_{th,low}}{V_{ds,high} - V_{ds,low}} \tag{3.3}$$

where ($V_{th,low}$, $V_{ds,low}$) and ($V_{th,high}$, $V_{ds,high}$) are the threshold and drain-source voltages for the first and second transfer curves, respectively. The downside of using this method is that it only captures V_{th}-shift for two (or a few) V_{ds}. This makes a comparison between different technologies difficult since the choice of reference voltages ($V_{th,low}$, $V_{ds,low}$) and comparing voltages ($V_{th,high}$, $V_{ds,high}$) is more or less arbitrary. Furthermore, to see the effect of DIBL over a large range of V_{ds} with small steps in between, one would have to measure the transfer characteristics for each step from the lowest V_{ds} to the highest, resulting in long measurement times.

The Drain Current Injection Technique

In [Paper C], an alternative measurement method is proposed. This method is based on the drain current injection technique (DCIT), which was introduced to characterize the off-state breakdown voltage of field-effect transistors [117]. With this measurement technique, the drain current used as the criterion for V_{th} is kept constant, while V_{gs} is decreased from an 'open channel' to a 'depleted channel' condition. As the channel becomes more depleted, V_{ds} increases to maintain a constant threshold current. This will yield a large range of V_{th}-V_{ds} data in one measurement, which then can be used to calculate the DIBL parameter in Equation 3.3. Furthermore, the DIBL parameter can be expressed as a difference between any V_{th} data point ($V_{th,i}$) and its neighboring data point $V_{th,i-1}$, divided by the difference between their respective $V_{ds,i}$ and $V_{ds,i-1}$. This new definition of the DIBL parameter is given by

$$\sigma_{DCIT} = -\frac{\Delta V_{th}}{\Delta V_{ds}}\bigg|_{I_d = I_{d,th}} \tag{3.4}$$

where $I_{d,th}$ is arbitrarily set to 1 mA/mm. The standard definition given by Equation 3.3 will only reflect the threshold shift relative to an arbitrary reference voltage $V_{th,low}$, whereas in Equation 3.4, SCEs can instead be interpreted as the degree to which the barrier (formed by the gate) decreases if the drain-source voltage is incrementally increased. Furthermore, it is possible to observe large variations in DIBL in small V_{ds}-intervals, which then can be linked to variations in epitaxial design or processing-related parameters.

3.1 Heterostructure Design Variations

The DCIT measurements were applied to AlGaN/GaN HEMTs with a standard Fe-buffer (Type I), and to InAlN/GaN HEMTs with an AlGaN back-barrier with different channel thicknesses (Type II). See Table 3.1 for detailed data on device design and each epitaxial heterostructure design.

In Figure 3.2, σ_{DCIT}-V_{ds} and V_{th}-V_{ds} data for the standard Fe-buffer (Type I) with L_g varying from 50–250 nm is shown. The maximum σ_{DCIT} ($\sigma_{DCIT,max}$) decreases with respect to L_g when V_{ds} = 5-20 V. The 50-70 nm gate lengths display similar behaviour in which σ_{DCIT} at low V_{ds}'s decreases and reaches a minimum, then increase to a maximum value, followed by a decrease toward a constant value. The rapid increase of σ_{DCIT} seen for L_g = 50 nm and L_g = 70 nm is caused by the barrier lowering in the off-state. A relatively small increase in V_{ds} can maintain $I_{d,th}$ given a fixed decrease in V_{gs}, resulting in a large σ_{DCIT}. This is also seen in the inset of Figure 3.2, where a rapid decrease in V_{th} occur at Vds ≈ 10 V. The poor electron confinement in the buffer is likely causing electrons to move through the buffer under the depleted AlGaN/GaN more easily. This effect becomes more pronounced when L_g is downscaled since the drain bias is able to affect the conduction band profile under the source side of the gate. This will be discussed in more detail in section 3.2. The overall barrier lowering effect diminishes in HEMTs with gate lengths above 70 nm, resulting in an almost constant decrease of V_{th} with respect to V_{ds} (inset in Figure 3.2).

The gate current (I_g) likely affects the V_{th} behavior at high voltages (Figure 3.2). When I_g constitute a significant proportion of $I_{d,th}$, σ_{DCIT} becomes a measure of the potential barrier reduction between gate and drain, instead of between drain and source. Therefore, σ_{DCIT} becomes a poor measure of DIBL. To ensure that the σ_{DCIT} primarily captures barrier lowering that causes drain-source leakage, I_g should be limited to 10-30 % of the injection current. Additionally, limiting I_g reduces the risk of destructive gate-drain breakdown.

Table 3.1. AlGaN/GaN and InAlGaN/GaN epitaxial heterostructures used for studying SCEs.

Heterostructure	Type I	Type II
Cap	GaN (1 nm)	-
Barrier	$Al_{0.3}Ga_{0.7}N$ (10 nm)	$In_{0.13}Al_{0.8}Ga_{0.06}N$ (7 nm)
Spacer	AlN (1 nm)	AlN (1 nm)
Channel	-	UID-GaN (50 nm, 100 nm, 150 nm)
Back barrier	-	C-doped ($3 \cdot 10^{17}$ cm^{-3}) AlGaN (800 nm)
Buffer	Fe-doped (exponential 10^{16}-10^{18}) GaN (0.8 μm)	C-doped GaN
Gate length (L_g)	50-250 nm	50 nm

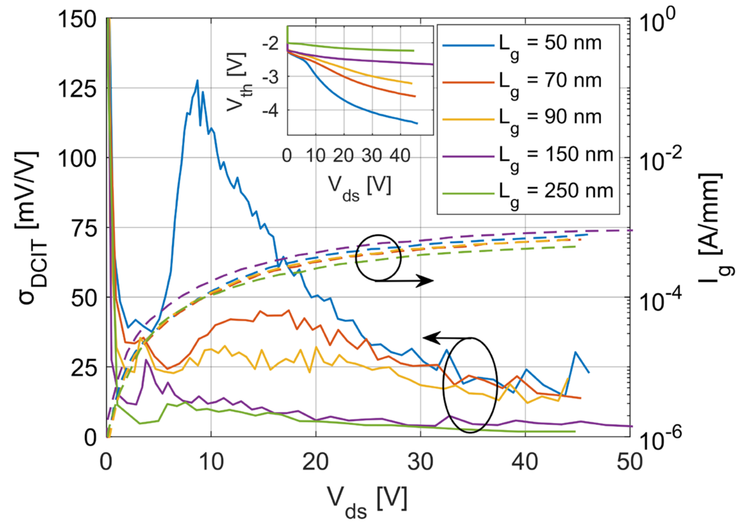

Figure 3.2. DIBL characteristics of HEMTs fabricated on Type I heterostructure with five different gate lengths [Paper C]. Inset: The V_{th} characteristics for the same five HEMTs.

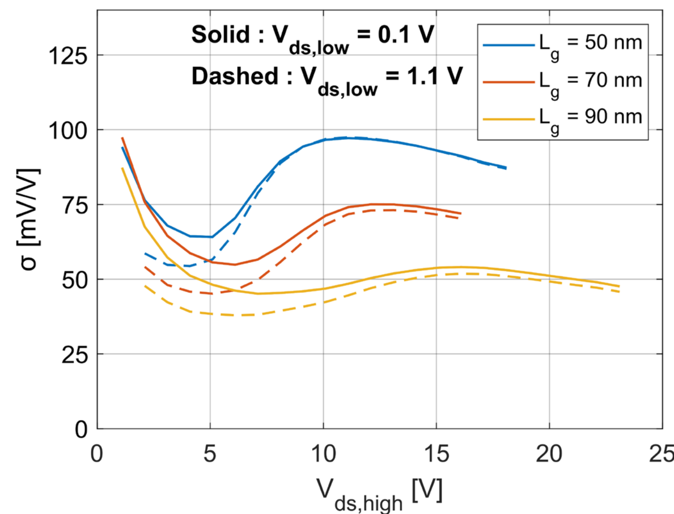

Figure 3.3. DIBL characteristics using the conventional technique with two reference voltages [Paper C]. HEMTs with three different gate lengths fabricated on Type I heterostructure were used.

The conventional method is applied to HEMTs of Type I (Figure 3.3). Two sets of reference voltages ($V_{th,low}$, $V_{ds,low}$) remain fixed, while the comparing voltages ($V_{th,high}$,$V_{ds,high}$) are varied. The standard definition of the DIBL parameter (σ) produces a similar behaviour to σ_{DCIT}, where a minimum and maximum value can be discerned. However, the absolute values of σ and σ_{DCIT} can differ. This is because Equation 3.3 reflects the rate of change of V_{th} relative to a fixed voltage, whereas Equation 3.4 approximates the derivative of V_{th} with respect to V_{ds}. Large sudden V_{th} changes can be observed more easily using σ_{DCIT} rather than σ. Moreover, the choice of reference voltages can impact σ, depending on whether the transistor is biased in the linear region or the saturation region. By contrast, Equation 3.4 is not

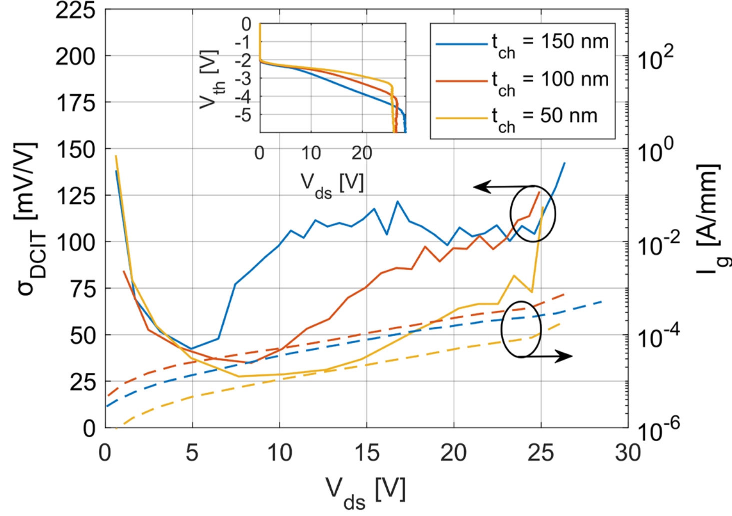

Figure 3.4. DIBL characteristics of HEMTs fabricated on Type II heterostructure with three different channel thicknesses and L_g = 50 nm. Inset: V_{th} characteristic for the same three HEMTs.

dependent on the choice of two arbitrary reference voltages, making it more suitable for comparing different technologies.

In Figure 3.4, the σ_{DCIT}-V_{ds} characteristic is shown for three different channel thicknesses in InAlN/GaN HEMTs (Type II). The impact of channel thickness on V_{th} is mostly pronounced in the V_{ds} range 5-25 V (inset in Figure 3.4). The channel thickness is positively correlated with σ_{DCIT} in this range. This correlation is consistent with previous studies [118], [119]. A 100 nm increase in channel thickness (from 50 nm to 150 nm) can result in a threefold increase in DIBL. The channel thickness is a growth parameter that affects the channel layer's electron distribution. A thicker channel produces an electron distribution whose tail end extends deeper vertically in the channel layer [93]. This facilitates conduction between drain and source underneath the depleted channel region. Conversely, the electron distribution is more compressed when the channel thickness is reduced (e.g. to 50 nm) due to the resistive C-doped AlGaN back-barrier. Therefore, a thick channel layer is expected to give rise to a higher leakage current than a thin channel. In the DCIT, this results in a smaller ΔV_{ds} to force the injection current through the channel layer, leading to a higher σ_{DCIT}. A thin channel layer is better at suppressing the punch-through effect due to the proximity of the resistive back barrier to the InAlGaN/GaN interface. As a consequence, the gate has improved control of the electrons in the channel region, and a larger ΔV_{ds} is needed to maintain the injection current.

In conclusion, the strength of the DCIT is the ability to extract V_{th}-V_{ds} trends quickly without introducing arbitrary reference voltages. This technique also facilitates the calculation of DIBL in terms of the slope in the V_{th}-V_{ds} characteristic, which gives an alternative interpretation of DIBL.

3.2 Physics-Based Device Simulations

Understanding the behaviour of the current density, electron density and E_c under varying bias conditions is important when minimizing DIBL through material or device processing optimization. In [Paper C], a qualitative physical computer-aided design (TCAD) model was utilized to simulate the DCIT applied to AlGaN/GaN HEMTs with 50-250 nm gate lengths and a Fe-doped buffer. Equation 3.4 was then employed to obtain the simulated DIBL-V_{ds} characteristics (Figure 3.5).

All simulations were performed using Sentaurus Synopsys Device simulations. The 2DEG was simulated by including a single donor trap level at the AlGaN combined with a spontaneous and piezoelectric polarization in the AlGaN and GaN layers. A single acceptor level 0.7 eV below the conduction band edge was introduced to simulate trapping effects related to Fe in the buffer layer [52]. A 0.8 μm thick buffer layer with an exponentially decreasing Fe doping concentration layer was added. The negatively charged acceptors also affect the mobility in the buffer layer. Therefore, an Arora doping-dependent mobility model was added to simulate the mobility degradation caused by impurity scattering [120].

The trend for short gate lengths is similar to what is seen in Figure 3.5, where the DIBL characteristics display a minimum and maximum value at low V_{ds}'s and an overall decrease in DIBL as V_{ds} increase. Furthermore, as L_g increases, the maximum and minimum σ_{DCIT} diminishes.

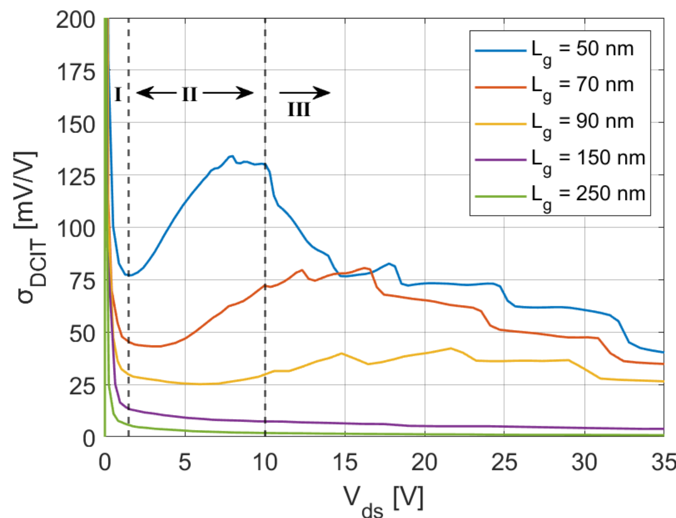

Figure 3.5. TCAD-simulated DIBL characteristics for GaN HEMTs with a Fe-doped buffer and varying gate lengths [Paper C].

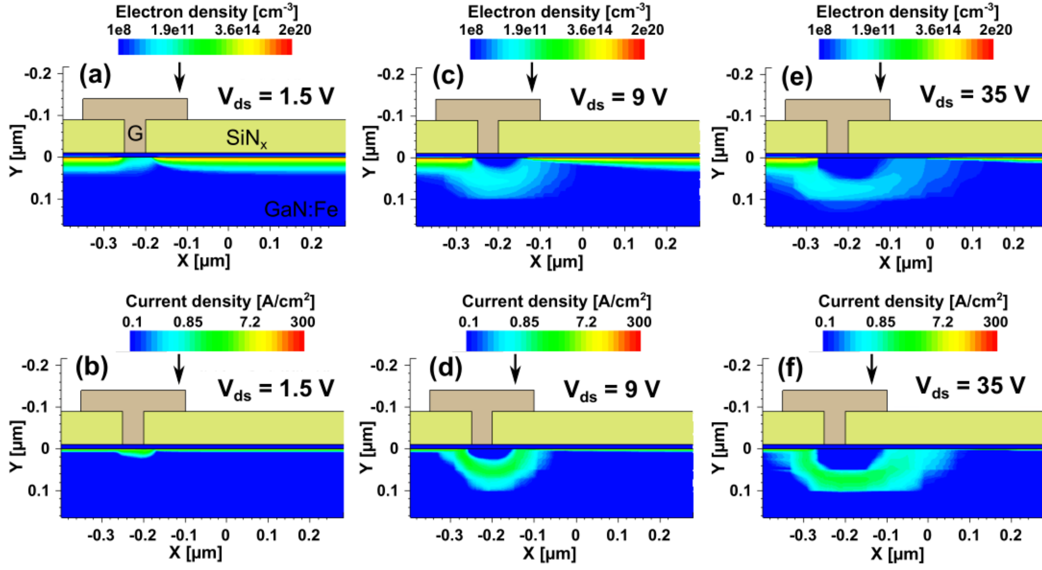

Figure 3.6. Electron concentration (a,c,e) and current densities (b,d,f) in at the AlGaN/GaN interface and in the GaN:Fe buffer the heterostructure of a GaN HEMT with L_g = 50 nm at different biases [Paper C].

The characteristics in Figure 3.5 can roughly be divided into three regions. A HEMT with a 50 nm gate length was chosen to demonstrate how different biases in these regions influence the electron concentration and electron current density at the AlGaN/GaN interface and in the Fe-doped buffer layer (Figure 3.6). When V_{ds} << 1 V (Region I), most of the electrons in the channel region are concentrated at the AlGaN/GaN interface. In these conditions, only a small change in V_{ds} is required to maintain the injection current, despite the channel becoming more depleted due to a decreasing V_{gs}. This leads to an apparent high DIBL. However, the transistor can be considered biased in the on-state, due to the high electron concentration at the AlGaN/GaN interface. Therefore, this region can be disregarded when studying DIBL.

As V_{gs} further decreases, the 2DEG gradually becomes depleted of electrons, which forces a larger V_{ds}, resulting in a sharp reduction of σ_{DCIT}. This trend continues until V_{ds} = 1.5 V (upper limit of Region I), where the electron concentration is small and non-uniform across the channel (Figure 3.6a). However, most of the electrons are still located near the AlGaN/GaN interface, which forces a large increase in V_{ds} given a small change in V_{th} to maintain the injection current. In these conditions, the gate's ability to modulate the electron concentration in the channel region is high. However, E_c is simultaneously lowered in the buffer layer due to the increasing drain bias (Figure 3.7), allowing a portion of the electron current to increase in the buffer region (Figure 3.6b).

In Region II (1.5 V < V_{ds} ≤ 10 V), the current density in the buffer becomes more pronounced as a greater portion of the electron concentration at the AlGaN/GaN interface is depleted (Figure 3.6c-d). The conduction band profile increases close to

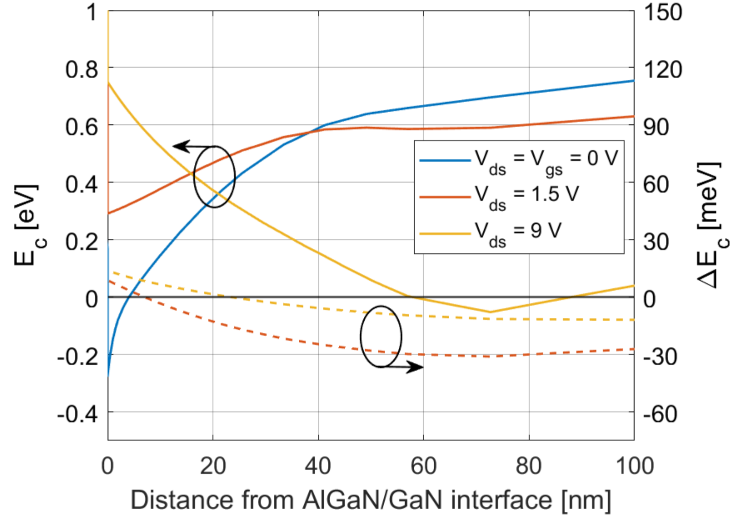

Figure 3.7. The conduction band profile (left y-axis) at the source side of the gate in thermal equilibrium and at two biases. The change in conduction band energy after a small change in V_{th} and V_{ds} (right y-axis) [Paper C].

the AlGaN/GaN interface but is reduced in the buffer region (Figure 3.7). Moreover, most of the reduction of E_c, given a change in V_{ds}, is located in the buffer region. Compared to Region I, the gate's ability to modulate the electron concentration diminishes as a greater portion of the electron concentration is displaced into the buffer region. In these conditions, a small change in V_{ds} can change E_c sufficiently to allow electrons to move under the depleted region, resulting in an increasing σ_{DCIT}. Uren et al. reported the same type of phenomena in Fe-doped buffers with short gate lengths [115]. The punch-through effect that causes an increased buffer current is most likely the main cause of the V_{th}-shift in short-channel HEMTs with doped buffer layers. It was shown that an increase of the Fe doping concentration in the buffer layer consequently leads to a lower DIBL. However, unwanted trapping effects are simultaneously introduced, which negatively affect device performance.

In Region III (V_{ds} > 10 V), the depleted region under the gate expands into the access region toward the drain contact as V_{ds} increases (Figure 3.6e). Electrons are displaced from the AlGaN/GaN interface into the buffer, where they start to occupy Fe trap states. This creates an effective channel that is longer than L_g, and whose length increases as V_{gs} decreases and V_{ds} increases. Therefore, an increasingly larger V_{ds} must sustain $I_{d,th}$, since a greater portion of the current is forced into the resistive buffer (Figure 3.6f). This leads to a reduction of σ_{DCIT}.

A TCAD model with a better agreement with the measured results requires a more in-depth understanding of different traps in the GaN buffer and at the III-nitride interfaces. In addition, to simulate the effects of high gate currents, a more advanced Schottky model has to be implemented. Nevertheless, the TCAD model presented in [Paper C] can be utilized to observe general trends of the electron concentration and current density at different biases.

Chapter 4

Conclusions and Future Work

When fabricating power electronic GaN-based HEMTs, it is crucial to minimize leakage currents and prevent sudden current surges during off-state operation at high voltages while maintaining low static and dynamic on-state resistances. Device processing-related parameters can have a significant negative impact on both on-state and off-state operations. These problems must be addressed before the material limits can be reached. The main objective of this work has been to optimize the device design and the fabrication process for power electronic MISHEMTs on a 'buffer-free' GaN-on-SiC heterostructure in terms of off-state leakage currents, breakdown and on-resistance. Additionally, a new measurement technique for analyzing DIBL in short-channel FETs was also presented in this thesis.

Ta-based ohmic contacts were successfully implemented in the 'buffer-free' device process. Contact resistances of 0.44-0.47 Ω·mm could be obtained. However, lower contact resistances should be attainable by carefully controlling the bottom Ta layer thickness, recess depth and recess sidewall angle. The latter two are determined by the dose applied by the lithography system and the etching time in the dry etching system. Further optimization could be achieved by varying the lithography dose and dry etching time on a single sample. Moreover, the impact of different in-situ and ex-situ pre-treatment should be explored.

Mesa isolation and N^+ implantation isolation were compared in terms of their impact on off-state leakage currents and breakdown voltage. The UID-GaN channel layer displays a low resistivity, likely caused by O-donors and N-vacancies. GaN mesa isolation is therefore limited in terms of high voltage operation. The SiC mesa isolation resulted in improved electrical isolation. However, breakdown voltages above 2000 V could not be achieved due to the limitations of SiC and possibly due to damages formed as a result of the dry etching process. GaN with nitrogen implantation isolation displays superior two-terminal and three-terminal leakage currents and breakdown voltages than GaN and SiC mesa isolation. A maximum three-terminal off-state breakdown voltage of 2496 V at an L_{gd} of 25 μm could be achieved by implementing nitrogen implantation isolation. Post-implantation

anneals up to 600 °C did not negatively affect the resistivity significantly. Higher breakdown voltages have been reported using implantation isolation in GaN. Future work should explore the impact of other implantation species such as He^+, Ar^+, or Kr^+ in 'buffer-free' heterostructures. Moreover, further optimization of the N^+ concentration and the implantation profile is required to achieve higher resistivity.

A stoichiometric LPCVD-grown SiNx passivation is capable of reducing gate leakage currents below 10 nA/mm above 1000 V, which is more than two orders of magnitude lower than Si-rich SiN_x passivation layers. The high gate-drain current in the samples with the Si-rich passivation is likely caused by poor isolation through the AlGaN barrier, SiN_x passivation and gate dielectric. Stoichiometric SiN_x enables high voltage operation with off-state drain leakage currents below 100 nA/mm and a $BV^2/R_{on,sp}$ FOM of 729 MW/cm^2, which is comparable to GaN-on-Si and GaN-on-SiC HEMTs found in the literature. However, optimization of gate field plate lengths and source field plate lengths is expected to further increase the off-state breakdown voltage in 'buffer-free' GaN HEMTs with a stoichiometric SiNx passivation layer. Additionally, the stoichiometric SiN_x passivation does not negatively impact the static on-resistance and displays a small dynamic on-resistance dispersion up to at least 240 V. However, the impact of high voltage stress on dynamic on-resistance has not yet been explored for this heterostructure. Moreover, the time constant, location, and voltage dependence of the traps that give rise to the observed dynamic on-resistance dispersion is not fully understood. Therefore, future work should explore the nature of the traps existing in the 'buffer-free' heterostructure by performing high voltage, PIV, and DCT measurements on HEMTs with and without buffer and varying passivation layers.

High-κ Ta_2O_5 and HfO_2 gate oxides exhibit high threshold voltages and low hysteresis in the transfer characteristics. In addition, MISHEMTs with Ta_2O_5 display gate leakage currents 2-3 times higher than MISHEMTs with SiN_x gate dielectrics. However, fixed charges and surface traps formed in the oxide or at the oxide/AlGaN interface can negatively impact dynamic on-resistance. This was not investigated in detail for Ta_2O_5 and HfO_2 gate oxides. Therefore, future work should explore potential surface-related trapping effects in these high-κ dielectrics. Moreover, the next step in developing high voltage switching HEMTs is to obtain normally-off behavior. One common approach is to combine recess etching into the AlGaN barrier with a thin insulating gate dielectric. Gate oxides with a high dielectric constant are preferable since they minimize the negative threshold voltage shift. Ta_2O_5 or HfO_2 should therefore be used instead of SiN_x for this purpose.

The DCIT can be used as an alternative to the transfer characteristics when studying the evolution of V_{th} in GaN-based HEMTs. Moreover, this method allows for a new interpretation of DIBL, where the derivative of V_{th} with respect to V_{ds} is used instead of two sets of arbitrarily chosen reference voltages. The advantage of this approach is the ability to observe large variations in DIBL in small V_{ds} intervals and relate them to variations in epitaxial design or variations in the device fabrication process. However, this new definition is sensitive to noise from the measurement system. Therefore, future work should explore the effect of integration time, step size, and noise filters in more detail. In this thesis, the DCIT

was primarily used to study DIBL in HEMTs with short L_g and L_{gd} at low voltages. However, this method should be utilized to optimize L_g in power switching HEMTs in terms of DIBL and R_{on}. Simulated DCIT show that the peak observed in the DIBL characteristics at short gate lengths is likely related to the punch-through effect, where the electrons move under the depleted channel region in the buffer region. The simulated and measured data are related to uncertainties in doping concentrations, doping profiles, and trap levels in the GaN buffer. These parameters have to be calibrated further to obtain a better agreement with the measured data.

GaN power switching HEMTs operating at voltage levels below 600 V and switching frequencies above 1 MHz are also of interest. This requires downscaling of gate length and access region to reduce on-state losses and optimization of field plates to improve off-state and switching performance. Future work should therefore focus on optimizing these device processing parameters in 'buffer-free' power switching HEMTs to achieve low voltage and high-frequency operation. Here, the DCIT should be utilized to explore appropriate V_{th} ranges for HEMTs with gate lengths in the range of 100-200 nm.

Normally-off behavior is preferable for power electronic switches since it prevents current conduction in the case of gate drive failure. GaN-based HEMTs are normally-on due to the intrinsic properties of the III-nitride heterostructures. However, normally-off operation can be achieved by partially etching the barrier, or by growing a p-doped capping layer on top of the barrier. These two techniques should be implemented for both high voltage and low voltage 'buffer-free' power switching HEMTs.

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Paper A

High Voltage and Low Leakage GaN-on-SiC MISHEMTs on a 'Buffer-Free' Heterostructure

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High Voltage and Low Leakage GaN-on-SiC MISHEMTs on a "Buffer-Free" Heterostructure

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***Abstract*—The performance of a novel 'buffer-free' AlGaN/GaN-on-SiC MISHEMTs for power switching applications is demonstrated in this letter. High voltage operation with exceptionally low gate and drain leakage currents is shown. A specific on-resistance of 3.61 mΩ·cm^2 and an abrupt breakdown voltage of 1622 V at a drain current of 22 nA/mm is achieved. Using two-terminal breakdown measurements, nitrogen-implanted GaN display breakdown fields of 0.96 MV/cm. The semi-insulating SiC substrate is capable of suppressing vertical leakage currents, ensuring that off-state operation is limited by lateral breakdown. The impact of electron trapping effects on dynamic on-resistance is small up to a drain quiescent voltage of at least 240 V. Drain current transient characteristics display a 14% increase in dynamic on-resistance with respect to quiescent drain bias, and a negligible change in resistance up to 100 ms. These types of 'buffer-free' heterostructures are of interest for power electronic applications above 1000 V and with potential for co-integration of power and RF-electronics.**

***Index Terms*—MISHEMT, 'buffer-free', normally-on, power switch, high voltage, AlGaN/GaN, GaN-on-SiC.**

I. Introduction

THE interest in wide-bandgap Gallium Nitride (GaN) and its compounds (AlGaN, InGaN, etc.) has increased substantially over the past decades owing to their high critical electric fields in combination with excellent electron transport properties [1]. These properties make III-nitride materials suitable for both high-power and high-frequency applications. GaN-based high electron mobility transistors (HEMTs) provide additional advantages, such as small parasitic capacitances and reverse recovery charge, which results in low switching losses in power applications [2].

High voltage GaN-based HEMTs grown on both Si and SiC substrates have been demonstrated [3]. When GaN is grown on Si or SiC, a thick carbon-doped GaN buffer layer is usually introduced to minimize lateral and vertical leakage currents and increase the lateral and vertical breakdown voltages [4], [5]. Moreover, the buffer layer also reduces the number of dislocations, which further decreases leakage currents and breakdown voltage [6]. In GaN-on-Si devices, high vertical leakage currents and limited vertical breakdown voltages are two major challenges. Several buffer designs have been proposed to improve vertical isolation, e.g. thicker buffer layers [6], optimization of carbon-doping concentration [5], and carbon-doped GaN or AlGaN superlattices [7], [8]. In GaN-on-SiC devices, GaN buffers with carbon doping or iron doping reduce lateral drain leakage, but the deep level traps also lead to current collapse and an increase in dynamic on-resistance ($R_{on,dyn}$) [4], [9], [10].

Currently, low-cost Si substrates are the most attractive alternative for power switching GaN HEMTs. However, SiC offers a higher electrical resistivity and a higher thermal conductivity than Si, allowing lower substrate leakage currents and improved heat dissipation [11]. Furthermore, the lattice mismatch between GaN and SiC is lower, enabling GaN growth with reduced dislocation densities [11].

The manufacturing cost of SiC wafers currently prevents GaN-on-SiC devices from gaining more traction. However, the price is expected to decrease as SiC wafer manufacturing technology improves [12]. Additionally, vertical leakage through a buffer layer does not primarily limit the breakdown voltage in GaN-on-SiC HEMTs as opposed to GaN-on-Si. Therefore, SiC could become a viable alternative at higher voltages.

In this study, high voltage AlGaN/GaN metal-insulator-semiconductor (MIS)HEMTs were fabricated on a heterostructure that has the potential to improve electron confinement, reduce leakage currents, and reduce trapping effects associated with carbon or other deep level elements that cause $R_{on,dyn}$ dispersion. The MISHEMTs were realized on a novel 'buffer-free' heterostructure with excellent crystal quality and electron transport properties. In addition, the heterostructure was grown on a semi-insulating (SI) SiC substrate, which limits the breakdown voltage to lateral breakdown in the III-nitride heterostructure. The MISHEMTs presented here are normally-on (D-mode) with double passivation and field plates. The off-state breakdown voltage, on-state resistance (R_{on}), pulsed IV (PIV) and drain current transient (DCT) characteristics demonstrate the potential of this type of material.

II. Experimental

The heterostructure was grown on a 500 μm high purity SI-SiC substrate and consists of (from the SiC substrate) a 43 nm thick AlN nucleation layer, a 265 nm unintentionally doped (UID) GaN channel, an 18.5 nm $Al_{0.22}Ga_{0.78}N$ barrier layer and a 2.5 nm GaN cap layer. The UID GaN channel has

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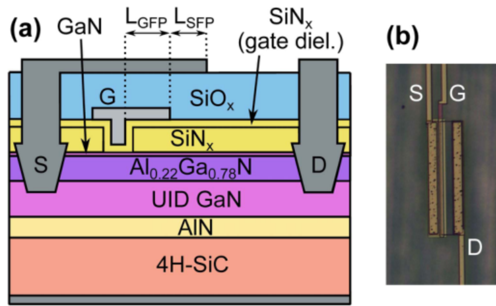

Fig. 1. (a) Schematic of a MISHEMT fabricated on a 'buffer-free' heterostructure. Dimensions are not to scale. (b) Top view microscope image of a typical MISHEMT.

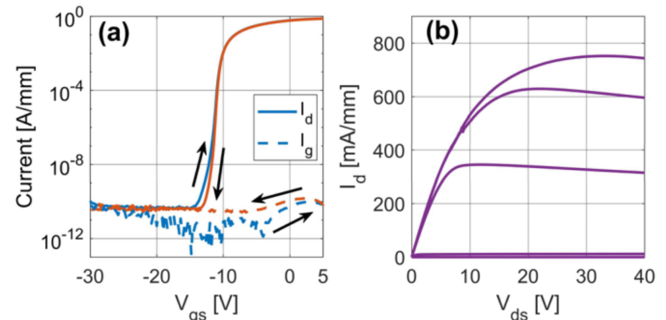

Fig. 2. (a) DC transfer characteristics for V_{ds} = 40 V with hysteresis (arrows showing sweep direction). (b) DC output characteristics with V_{gs} ranging from -20 V to 5 V in steps of +5 V.

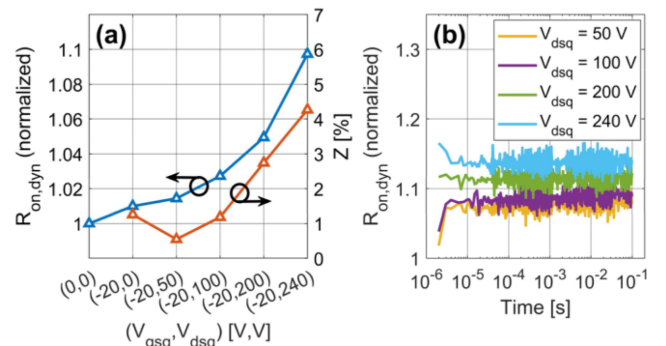

Fig. 3. (a) Normalized $R_{on,dyn}$ and slump ratio at different quiescent gate and drain biases. (b) Drain current transient measurement (expressed in normalized $R_{on,dyn}$) at different quiescent drain biases with gate quiescent V_{gsq} = -20 V.

an unintentional carbon doping concentration of $3\cdot10^{16}$ cm^{-3}. The heterostructure was grown with metal-organic chemical vapor deposition (MOCVD) by SweGaN AB employing their QuanFINE® concept [13]. The electron sheet carrier concentration (n_s) is 7.1 · 10^{12} cm^{-2} and the electron mobility is 2018 cm^2/V·s, as measured with contactless Hall measurements.

The MISHEMT fabrication started with a deposition of a 100 nm stoichiometric SiN_x passivation layer using low-pressure chemical vapor deposition (LPCVD) [14]. After a gate recess etch into the SiN_x passivation, a 43 nm stoichiometric SiN_x gate dielectric was deposited with LPCVD. Recessed Ta/Al/Ta-based ohmic contacts with a contact resistance of 0.44 Ω·mm were defined using a self-aligned process [15]. Nitrogen implantation was used to isolate the active areas. The implantation profile covers the entire GaN layer with a nitrogen concentration of $(0.5-1)\cdot10^{18}$$cm^{-3}$ and penetrates 50 nm into the SiC substrate. The gate electrodes (Ni/Pt/Au/Ti) were deposited using e-beam evaporation. A 600 nm SiO_x layer was then deposited using plasma-enhanced chemical vapor deposition (PECVD). Ti/Au/Ti was deposited to form source-connected field plates. Lastly, the backside of the sample was metallized with Ti/Au.

The MISHEMTs have a width (W) of 200 μm, a gate length (L_g) of 2 μm, a gate-source distance (L_{gs}) of 2 μm, gate-drain distances (L_{gd}) of 10-20 μm, a gate-integrated field plate length (L_{GFP}) of 4 μm, and a source-connected field plate length (L_{SFP}) of 5 μm (measured from the gate field plate edge). A schematic and a microscope image of the HEMT can be seen in Fig. 1a and 1b, respectively. In addition, isolation structures consisting of two ohmic contacts with separations (L) ranging from 5-20 μm were also defined in the fabrication process.

III. Results

MISHEMTs with an $L_{gd} = 20$ μm was used in the DC, PIV and DCIT measurements. Transfer and output characteristics were measured with a Keysight B1500A parameter analyzer. The transfer characteristics (Fig. 2a) were obtained for V_{ds} = 40 V in both forward and reverse sweep directions with V_{gs} swept in steps of 0.2 V. The output characteristics (Fig. 2b) were measured up to 40 V, with V_{gs} in the range of -20 V to 5 V in steps of +5 V.

Drain and gate currents are in the sub-100 pA/mm range during off-state operation in both forward and reverse directions due to the highly insulating properties of the nitrogen-implanted GaN and the high-quality SiN_x passivation and gate dielectric (Fig. 2a). The transfer characteristics display small hysteresis, indicating few trapped charges. The threshold voltage (V_{th}) is −11.2 V (at 10 μA/mm), and the I_{on}/I_{off}-ratio is $\sim10^{10}$ (measured between V_{gs} = 5 V and −20 V with V_{ds} = 40 V). The maximum saturation current (at V_{gs} = 5 V) is 752 mA/mm (Fig. 2b). The specific on-resistance ($R_{on,sp}$) was calculated using the drain current at (V_{ds} = 1 V, V_{gs} = 0 V), and the active area, defined as A = (L_{gs}+L_g+L_{gd}+ 2L_T)· W, where L_T is the transfer length of the ohmic contact (from the TLM measurement). With an L_T = 1.04 μm, and a L_{gd} = 20 μm, the specific on-resistance $R_{on,sp}$ = R_{on}·A is 3.61 mΩ·cm^2.

PIV and DCT characteristics were obtained using an AMCAD 3200 system. In these measurements, the MISHEMT is switched from an off-state quiescent point (V_{dsq}, V_{gsq}), to an on-state bias (V_{ds}, V_{gs}) where $R_{on,dyn}$ is extracted. V_{dsq} was varied between 0 V and 240 V (system limit), while V_{gsq} was set to -20 V. $R_{on,dyn}$ was extracted at V_{ds} = 1 V and V_{gs} = 0 V. On/off-state times were set to 1 μs / 99 μs for the PIV measurement and 100 ms / 100 ms for the DCT measurement. The gate pulse and measurement time were delayed 200 ns and 300 ns after the drain pulse, respectively. This ensures that the measurements capture trapping effects with short time constants.

The PIV measurements display a 10% increase in $R_{on,dyn}$ at a quiescent of (V_{gsq},V_{dsq}) = (-20 V,240 V) compared to the quiescent reference point, (V_{gsq},V_{dsq}) = (0 V,0 V) (Fig. 3a). The increase in $R_{on,dyn}$ is comparable to other HEMTs found in literature, where $R_{on,dyn}$ in the range of 30-70% above the static value have been reported for V_{dsq} = 200-240 V with short on-state durations [16]–[18]. The trapping effects were further characterized by calculating the gate and drain slump

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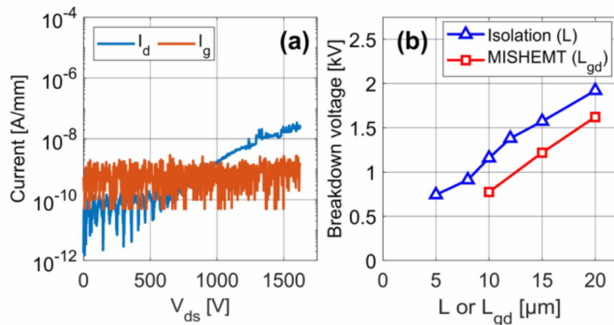

Fig. 4. (a) Off-state breakdown characteristics at V_{gs} = -20 V of a MISHEMT with L_{gd} = 20 μm. (b) Breakdown voltage of MISHEMTs and two-terminal isolation structures with varying L_{gd} and L.

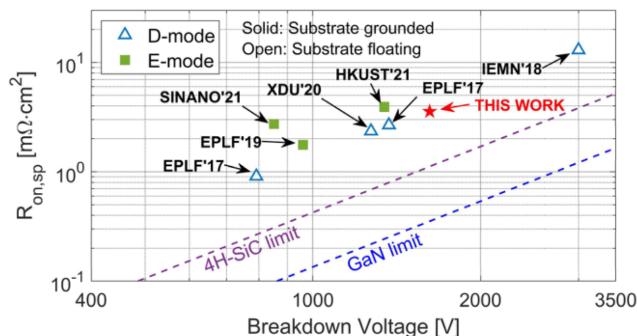

Fig. 5. Specific on-resistance versus breakdown voltage benchmark using the 1 μA/mm current criterion.

ratios (Z_G and Z_D) at V_{gs} = 1 V and V_{ds} = 25 V for all quiescent points (Fig. 3a). The Z_G (-20 V,0 V) ratio is less than 2%, and Z_D increases up to 4% with V_{dsq} increasing from 0 V to 240 V. A similar increase in $R_{on,dyn}$ has been reported for 'buffer-free' HEMTs with a Si-rich SiN_x first passivation [10], which indicate that the dispersion is caused by trapping centers in the III-nitride heterostructure or at its interfaces. Due to the low UID carbon concentration, the trapping effects associated with carbon should be small in this type of heterostructure. Therefore, it is likely that deep trap states at (or in the vicinity of) the GaN/AlN interface get ionized during the off-state stress, which partially depletes the channel in the on-state.

In the DCT characteristics where V_{dsq} is varied from 50 V to 240 V, there is no significant change in $R_{on,dyn}$ from 3 μs up to 100 ms for all four quiescent points (Fig. 3b). Therefore, the trap concentration with time constants in this interval is small. A similar trend has been seen in GaN buffers with low carbon doping concentrations in the same time interval [19], indicating that there are other traps in the heterostructure with time constants longer than 100 ms.

The off-state breakdown voltage was measured with a Keysight 1505A parameter analyzer with a grounded substrate and V_{gs} = − 20 V. The breakdown criterion was set to 1 μA/mm. In addition, Fluorinert™ was added onto the surface to prevent arcing through the air. All measurements were carried out at room temperature and in dark conditions.

The gate and drain leakage currents for a HEMT with L_{gd} = 20 μm were measured with increasing V_{ds} until at least one exceeded the breakdown voltage criterion (Fig. 4a). A sub-22 nA/mm drain current could be maintained until an abrupt drain-source current surge at 1622 V. This results in a $BV^2/R_{on,sp}$ figure of merit (FOM) of 729 MW/cm^2. The substrate current measured between the drain pad and the chuck remained below the current compliance level up to the measurement limit of 3000 V. This means that the breakdown is not limited by vertical leakage currents, as seen in GaN-on-Si devices with thick buffers [6], [20]. Instead, it is primarily laterally limited. A gate leakage current below 10 nA/mm shows that the SiN_x gate insulator and first passivation successfully suppress leakage current at high voltages. The current surge observed in this device, and similar devices were caused by a non-destructive source-drain current path or a destructive gate breakdown.

The two-terminal (isolation) breakdown voltages are higher than the three-terminal breakdown voltages (Fig. 4b). A breakdown field of 0.96 MV/cm can be obtained for a contact separation of 20 μm. The peak electric field in planar isolation structures should be located at the edge of the ohmic contacts [21], limiting the two-terminal breakdown to the critical electric field of the implanted GaN. This indicates that further optimization of the MISHEMT layout parameters related to field plate dimensions could increase the three-terminal breakdown voltage.

In Fig. 5, the off-state breakdown voltage and $R_{on,sp}$ is benchmarked against other D-mode and enhancement-mode (E-mode) HEMTs with grounded and floating substrates found in the literature [22]–[27], where the 1 μA/mm breakdown current criterion has been used. Devices fabricated in this work show comparable $BV^2/R_{on,sp}$ FOM to other high voltage HEMTs in literature, which ranges from 524-877 MW/cm^2 [22], [24], [26]–[28]. Generally, breakdown measurement performed on grounded Si substrates reduces the breakdown voltage (compared to floating substrates) due to a high vertical leakage through the buffer layer [23]–[25], [29]. However, this does not become a problem for GaN-on-SiC 'buffer-free' HEMTs due to the SI-SiC substrate.

IV. Conclusion

In this study, high voltage normally-on GaN-based MISHEMTs fabricated on a 'buffer-free' heterostructure grown on SI-SiC are characterized in terms of DC, switching and high voltage performance. Low off-state drain and gate leakage current can be achieved using highly insulating SiN_x gate and passivation layers, combined with nitrogen implantation for device isolation. These measures enable FOM comparable with similar GaN-on-Si and GaN-on-SiC devices from the literature. The pulsed IV characteristics display a small increase in dynamic on-resistance due to trapping effects, which is likely associated with growth defects or interface traps. The dynamic on-resistance increases with increasing drain quiescent bias but displays a minor change over the measured time interval. In conclusion, this study demonstrates the first GaN-on-SiC power switching HEMT that combines high voltage and low leakage operation without requiring a carbon or iron-doped buffer.

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Paper B

AlGaN/GaN/AlN 'Buffer-Free' High Voltage MISHEMTs with Si-rich and Stoichiometric SiN_x First Passivation

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AlGaN/GaN/AlN ‘Buffer-Free’ High Voltage MISHEMTs with Si-rich and Stoichiometric SiN_x First Passivation

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***Abstract*— ‘Buffer-free’ AlGaN/GaN/AlN high electron mobility transistors (HEMTs) with a thin GaN channel layer and a thin AlN nucleation layer grown on a semi-insulating SiC substrate are presented. Si-rich and a stoichiometric low-pressure chemical vapor deposition (LPCVD) SiN_x first passivation were employed to study the impact of stoichiometry on off-state leakage currents in GaN-based metal-insulator-semiconductor (MIS)HEMTs. Nitrogen implantation isolation, SiO_x second passivation, gate and source field plates were utilized. Off-state drain leakage current was reduced 2-3 orders of magnitude by depositing a stoichiometric instead of a Si-rich SiN_x passivation. The gate leakage current was suppressed below 10 nA/mm until breakdown. A destructive breakdown voltage of 1742 V and 1532 V was measured for the MISHEMTs with Si-rich and stoichiometric SiN_x passivation, respectively. This demonstrates how high voltage, low leakage MISHEMTs can be achieved using a ‘buffer-free’ heterostructure by optimizing the first passivation stoichiometry.**

Keywords—AlGaN/GaN/AlN, ‘buffer-free’, MISHEMT, GaN-on-SiC, high voltage, SiN_x passivation

I. INTRODUCTION

GaN-based HEMTs exhibits high breakdown voltage, high electron mobility, and high switching frequency, making them excellent devices for power electronic applications [1]. The most popular substrate alternative for GaN devices is low-cost Si [2], but GaN-on-SiC HEMTs have also been reported [3]. GaN growth on Si and SiC typically require a thick carbon-doped buffer to reduce growth defects and/or to lower vertical and lateral leakage currents [4]-[6]. In this paper, a novel ‘buffer-free’ AlGaN/GaN/AlN heterostructure grown on a semi-insulating SiC substrate is utilized to fabricate high voltage HEMTs. The heterostructure consists of a thin AlN nucleation layer and a thin unintentionally doped (UID) GaN layer, both of which display high crystal quality. MISHEMTs with Si-rich and stoichiometric SiN_x first passivation layers were fabricated. The devices were characterized in terms of DC (output/subthreshold characteristics) and off-state breakdown voltage. Additionally, leakage test structures were used to further analyze leakage current through the SiN_x layers.

II. GROWTH AND FABRICATION

The epitaxial heterostructure consists of four layers: a 43 nm AlN nucleation layer, a 265 nm UID GaN layer, an 18.5 nm $Al_{0.22}Ga_{0.78}N$, and a 2.5 nm GaN cap (Fig. 1a). A 500 µm high-purity semi-insulating SiC substrate was used for the growth. The layers were grown by SweGaN AB using a metal-organic chemical vapor deposition (MOCVD) system. The device fabrication started with the growth of a SiN_x first passivation layer using a low-pressure chemical vapor deposition (LPCVD) system. Two different passivation layers were grown: A 100 nm stoichiometric layer (Device A), and a 177 nm Si-rich layer (Device B). The Si-rich and stoichiometric films were deposited using a 224/23 sccm and a 98/360 sccm dichlorosilane/ammonia (H_2SiCl_2/NH_3) ratio, respectively. A 40-43 nm LPCVD stoichiometric SiN_x gate dielectric, and a 600 nm plasma-enhanced chemical vapor deposition (PECVD) SiO_x second passivation was deposited after gate recess etch, ohmic contact deposition and gate metal deposition. The gate-source distance, gate-drain distance and device width were designed to 2 µm, 20 µm and 100-200 µm, respectively. The gate lengths were 2 µm and 4 µm for Device A and Device B, respectively. A 4 µm gate-integrated field plate and a 5 µm source-integrated field plate was included in the gate metal and source metal deposition steps. Nitrogen implantation was utilized to isolate the material surrounding the active area. A top view microscope image was taken of the device (Fig. 1b). Moreover, a dielectric leakage test structure like the one used in [7] was utilized. A schematic of the test structure can be seen in Fig. 1c.

III. RESULTS

The MISHEMT output characteristics were obtained for V_{gs}=-20-5 V in steps of 5 V for Device A and Device B (Fig. 1d). A maximum current of 764 mA/mm for Device A and 655 mA/mm for Device B was measured at V_{ds}=35 V, V_{gs}=5 V. For Device A, a 13.5 Ω·mm on-resistance was calculated at V_{ds}=1 V, V_{gs}=0 V. This gives a specific on-resistance $R_{on,sp}=R_{on}\cdot(L_{sd}+2L_T)\cdot W$ of 3.5 mΩ·cm², with a source-drain distance (L_{sd}) of 24 µm and a transfer length (L_T) of 1.04 µm. The subthreshold characteristics for Device A and B measured at V_{ds}=40 V can be seen in Fig. 2a. The threshold voltage measured at ~10 µA/mm for Device A and B was -12.1 V and -10.4 V, respectively. The gate and drain leakage current was reduced from $4\cdot10^{-8}$ A/mm to $4.7\cdot10^{-11}$ A/mm at V_{gs}=-20 V by using a stoichiometric SiN_x film. Additionally, the leakage test structure was used to decouple surface/interface leakage currents and barrier leakage currents by sweeping the gate voltage from 0 V to -150 V. Barrier leakage currents through the SiN_x film(s) and AlGaN layer increased by almost three orders of magnitude for the sample

with Si-rich SiN_x from -40 V to -150 V (Fig. 2b), as exhibited by the large discrepancy between I_{guard} and I_{gate}. However, the stoichiometric SiN_x maintained a barrier leakage below 1 nA from 0 V to -150 V (Fig. 2c). Drain and gate currents were measured in the off-state condition using V_{gs}=-30 V, with V_{ds} being ramped up from 0 V until hard breakdown occurred (Fig 3a). For Device A and B, breakdown occurred at 1532 V and 1742 V, respectively. However, the drain current was more than three orders of magnitude higher in Device B compared to Device A at breakdown. The leakage current increase in Device A was predominantly drain-source leakage at high voltages. In Device B, the drain current was limited by the gate leakage through the first passivation layer and the gate dielectric layer. Gate leakage currents up to 1000 V were also measured for HEMTs with Si-rich SiN_x passivation and gate lengths between 1-4 µm to make the comparison between Device A and B fairer (Fig. 3b). No significant difference in gate leakage can be seen between the three different gate lengths.

IV. Conclusion

Normally-on MISHEMTs with double passivation, nitrogen implantation, gate field plate and source field plate designs were fabricated to study a novel 'buffer-free' AlGaN/GaN/AlN-on-SiC heterostructure in terms of DC and high voltage capabilities. Gate and drain leakage current was successfully suppressed by using a stoichiometric SiN_x gate insulator and first passivation layer, which limits barrier leakage currents.

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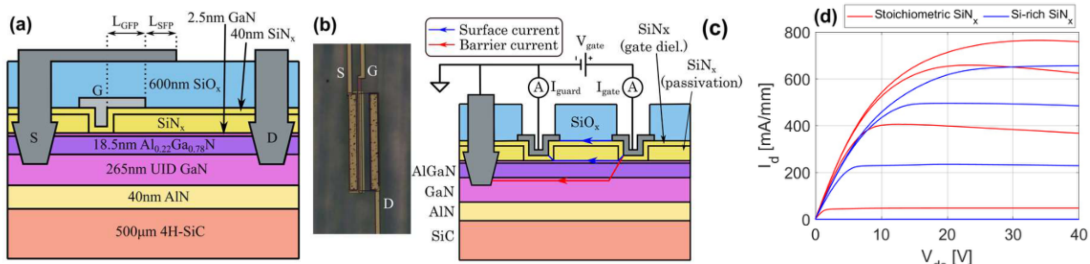

Fig. 1. (a) A schematic of the GaN-on-SiC MISHEMT. (b) Top view microscope image of the MISHEMT. (c) Dielectric leakage test structure. (d) Output characteristics of Device A and Device B with V_{gs}=-20-5 V with +5 V steps.

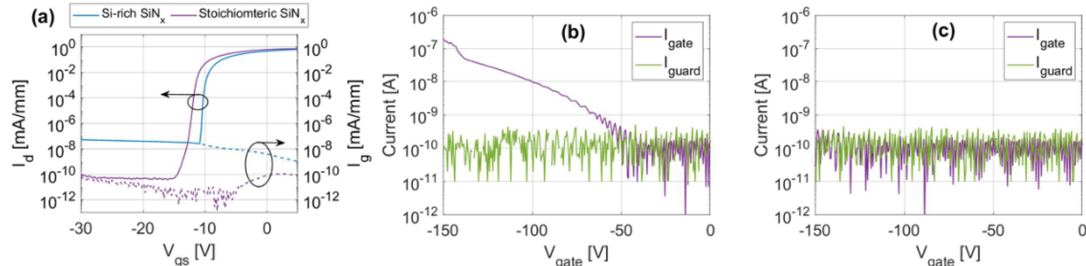

Fig. 2. (a) Subthreshold characteristics for Device A and B with V_{ds}=40 V. (b) Leakage test structure measurement with a Si-rich SiN_x passivation. (c) Leakage test structure measurement with a stoichiometric SiN_x passivation.

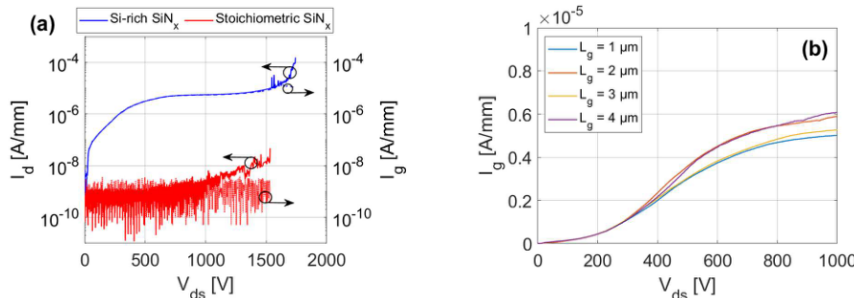

Fig. 3. (a) OFF-state breakdown characteristics for Device A and B with V_{gs}=-30V. (b) Gate leakage test for Device B with different gate lengths up to 1000 V.

Paper C

Investigation of Electron Confinement in GaN HEMTs with a Drain Current Injection Technique

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Investigation of Electron Confinement in GaN HEMTs with a Drain Current Injection Technique

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***Abstract*—The assessment of short channel effects is crucial in the high-frequency optimization of downscaled field-effect transistors such as GaN high electron mobility transistors (HEMTs). Drain-induced barrier lowering (DIBL) is commonly used to characterize and evaluate electron confinement in HEMTs fabricated on heterostructures with different epitaxial layers. This short channel effect is traditionally characterized in terms of the relative shift of the threshold voltage obtained from the transfer characteristics at different drain-source voltages. In this paper, we propose a drain current injection technique to assess DIBL. This method facilitates a direct measure of the threshold voltage over a wide range of drain-source voltages in a single measurement. The method is demonstrated and compared to the conventional method using AlGaN/GaN HEMTs with a Fe-doped buffer and different gate lengths. The measurements are analyzed and discussed with supporting physical technology computer-aided design (TCAD) simulations. The proposed method facilitates a more general and detailed measurement of the DIBL for HEMTs.**

***Index Terms*— DIBL, DCIT, SCE, GaN, HEMT**

I. Introduction

GaN-based HEMTs have proven to be suitable for both high power and high-frequency applications. The large bandgap and good electron transport properties of GaN and its associated heterostructures allows for the fabrication of III-nitride HEMTs with high breakdown voltages, low losses and high-frequency operation. GaN-based HEMTs and MMICs operating up to K_a-band are commercially available from several foundry services. In addition, there has recently been an increased interest in GaN-technology working even beyond the V- and E-bands [1]-[4]. Operation at these frequencies requires downscaling of gate length (L_g) and access regions. However, this eventually results in short-channel effects (SCE), which causes a reduction in gain, efficiency, and output power [5]. Several techniques have been suggested to mitigate these unwanted effects. One approach is to grow a thinner top barrier to improve gate modulation [6]. Another method is to improve the electron confinement in the channel with an AlGaN back-barrier (BB) [7], or by introducing deep-level Fe or C traps in the buffer layer [8] [9].

A common measure used to make a quantitative assessment of the level of SCEs is drain-induced barrier lowering (DIBL). It manifests as a negative shift in the threshold voltage (V_{th}) with increasing drain-source voltage (V_{ds}). This shift is one of the many consequences of SCEs, emerging due to the loss in drain current (I_d) modulation. DIBL is conventionally obtained from the transfer characteristics, where I_d is measured while the gate-source voltage (V_{gs}) is swept from an off-state to an on-state condition (or vice versa) for two different values of V_{ds}. However, the drawback of this method is the wide range of V_{ds} intervals used by different research groups [4] [8] [10]-[13], which prevents a direct comparison between transistor technologies. Furthermore, the conventional method does not provide insight into the electron confinement outside the selected interval.

In this paper, we propose an alternative method based on the drain current injection technique (DCIT) to characterize DIBL in GaN-based HEMTs. DCIT has previously been used to study off-state breakdown voltage in field-effect transistors (FETs) [14]. Here, we suggest that DCIT can be used to directly study the evolution of V_{th} with respect to V_{ds}, which, in turn, can be used to calculate DIBL as a function of V_{ds}. In this way, DIBL can be calculated for any V_{ds} interval, or as a function of V_{ds}. This provides insight into the appropriate bias range and facilitates the comparison with other transistor technologies in different bias ranges.

The measurement technique is demonstrated on AlGaN/GaN HEMT technologies with a standard Fe-doped buffer and varying gate lengths. Technology computer-aided design (TCAD)

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simulations were utilized to explore the physics in the heterostructure at different V_{th} and V_{ds} for short gate length devices. Additionally, we compare the DCIT with the conventional method of acquiring DIBL.

II. Method

In the conventional method, DIBL (σ) is calculated from two values of V_{th} obtained from the transfer characteristics measured at different V_{ds} using

$$\sigma = -\frac{V_{th,high} - V_{th,low}}{V_{ds,high} - V_{ds,low}} \quad (1)$$

where $V_{ds,high}$ and $V_{ds,low}$ are two selected drain-source voltages, while $V_{th,low}$ and $V_{th,high}$ are the corresponding V_{gs} at a chosen threshold drain current $I_{d,th}$. The threshold current is commonly set to a fixed current density (mA/mm), or to a percentage of the saturated drain current density.

We instead apply the DCIT, where V_{ds} is monitored as V_{gs} is reduced from an "open channel" to a "depleted channel" condition while injecting an I_d equal to the pre-defined threshold current criterion ($I_{d,th}$). As V_{gs} (corresponding to V_{th}) decreases, the channel region becomes increasingly resistive, which leads to an increase in V_{ds} to force the same $I_{d,th}$. This allows for the acquisition of V_{th}-V_{ds} data in a single measurement. Moreover, the data extracted from the DCIT measurement can be utilized to calculate the DIBL parameter in terms of the rate of change between two neighboring (V_{th},V_{ds}) points, i.e.

$$\sigma_{DCIT} = -\frac{\Delta V_{th}}{\Delta V_{ds}}\bigg|_{I_d = I_{d,th}} \quad (2)$$

where ΔV_{th} and ΔV_{ds} are the differences between two adjacent V_{th} and V_{ds}, respectively. The DCIT combined with Eq. 2 will reflect the change in barrier height under the gate resulting from a small increase in V_{ds}. This makes it possible to track large changes in V_{th} (and consequently the barrier lowering) in small V_{ds} intervals and relate them to the device design. It is also easier to discern general V_{th}-trends than in the conventional method (Eq. 1).

During measurements, the step in V_{gs} (or ΔV_{th}) should be kept as small as possible in regions where V_{ds} rapidly changes. Typically, a step size in the 10-75 mV range is sufficient. Noise can be suppressed by altering the step size and increasing the integration time in the measurement system. Additionally, it is possible to readily assess the progression of V_{th} for different threshold criteria ($I_{d,th}$) by setting the drain current as a secondary sweep in the measurement system.

In this study, all measurements were performed with a parameter analyzer (Keysight B1500A). The threshold current was set to 1 mA/mm for all measurements. While keeping I_d constant, V_{gs} was swept from 0 V to –8 V in small steps (10-30 mV). The difference between neighboring V_{th} and V_{ds} were used to calculate σ_{DCIT} (Eq. 2). The DIBL parameter from Eq. 1 was calculated after measuring the transfer characteristics. The drain current was measured as V_{gs} was swept from -3 V to 0 V for V_{ds} = 0.1-25.1 V in steps of 1 V.

III. Experimental

We demonstrate the method using AlGaN/GaN HEMTs with a Fe-doped buffer. The total GaN buffer thickness is 1.8 µm, where approximately 1 µm has a constant Fe-doping concentration (~10^{18} cm^{-3}), and 0.8 µm has an exponentially decreasing Fe-doping concentration to around 10^{16} cm^{-3} close to the AlGaN/GaN interface. The epitaxial structure was grown on a semi-insulating SiC substrate using metalorganic chemical vapor deposition (MOCVD). An $Al_xGa_{1-x}N$ top barrier layer was grown with a constant Al content of 30 %. Additionally, an AlN spacer layer was incorporated between the GaN and AlGaN barrier to improve the electron confinement and increase the electron mobility [15].

The processing of the HEMTs started with the deposition of a 60 nm thick Si-rich SiN_x passivation using a low pressure chemical vapor deposition (LPCVD) system [16] [17]. Mesa isolation structures were dry-etched with a chlorine-based plasma in an Oxford Plasmalab 100 ICP/RIE system. Ohmic contacts were formed by recessing and evaporation of a Ta/Al/Ta metal stack [18]-[20]. The gates were formed by two electron beam lithography (EBL) processes. The first EBL step was used to define a etch mask for the SiN_x, while the second EBL step defined the gate metallization pattern. The first step effectively defines the gate length. After the second lithography step, a Ni/Pt/Au Schottky metallization was electron beam evaporated. This process enabled a gate-integrated field plate. HEMTs with gate lengths of 50 nm, 70 nm, 90 nm, 150 nm, and 250 nm were fabricated. The gate-source distance, gate-drain distance and gate width were design to 0.75 µm, 1.5 µm and 50 µm, respectively.

IV. Results and discussion

A. *Impact of gate length in HEMTs with a Fe-doped buffer*

In Fig. 1, the σ_{DCIT} -V_{ds} and V_{th}-V_{ds} characteristics are shown. Gate lengths below 90 nm tend to display a distinct minimum and maximum value for σ_{DCIT}, both of which have a inverse relationship with L_g. The decrease in σ_{DCIT} with increasing L_g is expected because of the significant change in potential across the channel region caused by a high V_{ds} [21]. This results in a reduction of the potential barrier height for the electrons at the source side of the gate. The barrier lowering appears to be most pronounced for V_{ds} = 5-20 V for HEMTs with L_g = 50 nm and L_g = 70 nm. This causes V_{th} to shift by -1.25 V in the same interval (inset in Fig. 1). The highest rate of change occurs at around 9 V for the HEMT with the shortest gate length, where $\sigma_{DCIT,max}$ is 125-128 mV/V. This value decreases down to 45 mV/V when L_g increases to 70 nm. HEMTs with longer gate lengths (L_g > 70 nm) tend to have a smaller variation in σ_{DCIT}, resulting in an almost constant decrease in V_{th}.

The low DIBL seen for L_g = 150 nm and L_g = 250 nm requires a reduction of the step size to obtain more data points when V_{ds} sharply increases (inset in Fig. 1). In Fig. 1, the V_{gs} step size was lowered from 30 mV to 20 mV for L_g = 90 nm and 10 mV for L_g = 150-200 nm.

B. *TCAD simulations*

A qualitative model was utilized to analyze the underlying physics that give rise to the behavior seen for HEMTs with a Fe-doped buffer and varying gate lengths (Fig. 2). The simulations were carried out using Synopsys Sentarus TCAD simula-

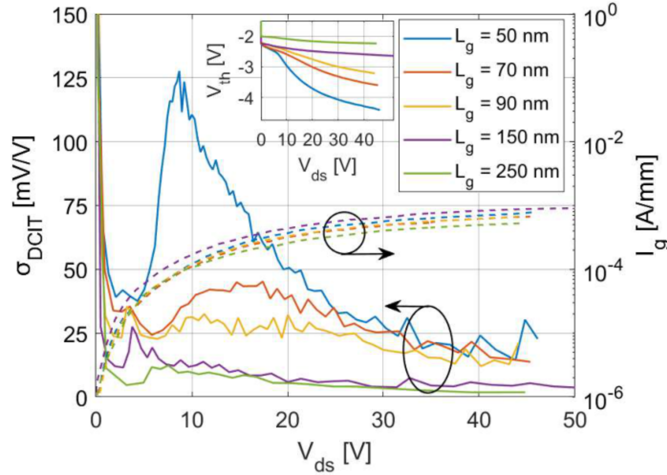

Fig. 1. DIBL characteristics for HEMTs with five gate lengths using the DCIT. Inset: corresponding threshold voltage plot of the five transistors.

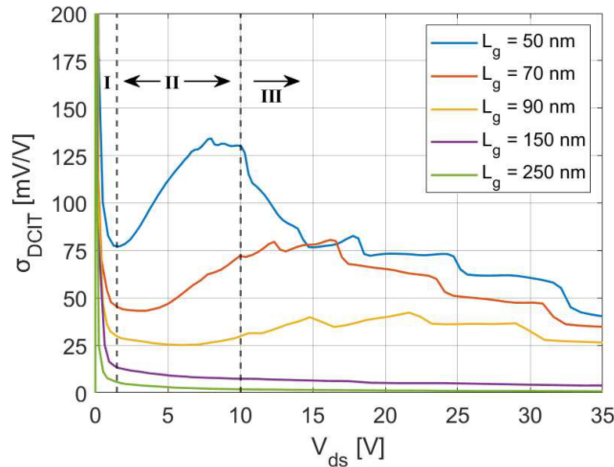

Fig. 2. Simulated DIBL characteristics of AlGaN/GaN HEMTs with a GaN:Fe buffer and different gate lengths.

tions. Surface traps at the AlGaN surface and piezoelectric polarization were included to simulate the formation of the 2DEG. Additionally, a single trap level 0.7 eV below the conduction band edge associated with Fe was added to the GaN layer [22]. A doping-dependent mobility model was included to account for scattering between electrons and charged Fe traps [23]. Discrepancies between Fig. 1 and Fig. 2 are related to uncertainties in L_g, net doping concentrations, doping profiles and trap energy levels. Nevertheless, general trends in the σ_{DCIT}-V_{ds} characteristics can be analyzed in terms of the distribution of the electron concentration and current densities in the GaN buffer. A 1 mA/mm injection current was used in the simulations.

The L_g-dependence of the simulated σ_{DCIT} behaves in a similar way as the measured data, where longer gate lengths tend to reduce the maximum and minimum σ_{DCIT}. Additionally, an overall decrease of DIBL is seen as V_{ds} increases beyond the peak DIBL value. The characteristics of a HEMT with L_g = 50 nm in Fig. 2 can be divided into three regions.

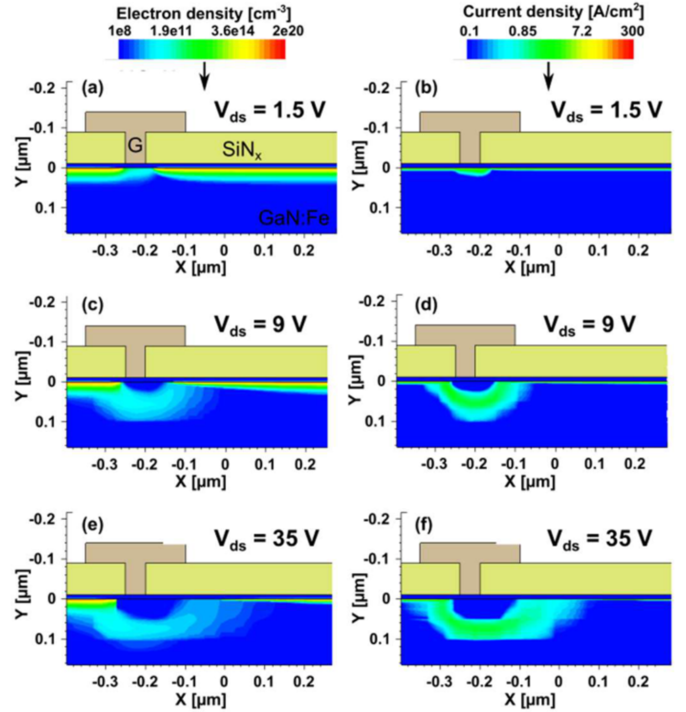

Fig. 3. Simulated electron concentrations (a, d, e) and electron current densities (b, d, f) in the channel and access regions at three biases.

Region I (V_{ds} ≤ 1.5 V) correspond to biases where the electron density and current density is concentrated at the AlGaN/GaN interface. When V_{ds} << 1 V, the electron concentration at the AlGaN/GaN interface in the channel is high and relatively uniform across the channel region. Only a small change in V_{ds} is required to maintain $I_{d,th}$, given a constant reduction in V_{gs}. In this condition, the transistor is biased in a more or less pure on-state, making this region less significant when studying DIBL.

As V_{ds} increases, the channel region in the vicinity of the AlGaN/GaN interface becomes increasingly depleted of electrons (Fig. 3a). Moreover, the electron concentration becomes non-uniform across the channel at the AlGaN/GaN interface, with a maximum concentration at the source side. A relatively large increase in V_{ds} is required to reduce the conduction band edge (E_c) under the gate (Fig. 4) to force the injection current through the channel when most of the electrons are located in the vicinity of the AlGaN/GaN interface. The E_c-reduction is greater in the buffer region, which gradually increases the electron concentration and current density and allows electrons to be funnelled under the partially depleted 2DEG (Fig 3b).

In Region II (1.5 V < V_{ds} ≤ 10 V), the conduction band edge is further reduced in the buffer layer (Fig. 4). The electron concentration and current density have shifted deeper into the buffer layer and have become more distributed vertically under the gate (Fig 3c-d). Under these conditions, the gate has less impact on the electrons deeper in the buffer. Therefore, only a small change in V_{ds} is required to sufficiently change E_c in the buffer layer (Fig. 4) in order to increase the electron concentration and allow the electrons to bypass the depleted region close to the AlGaN/GaN interface. This leads to a large V_{th} shift for a slight V_{ds} increase. A higher Fe doping concentration would

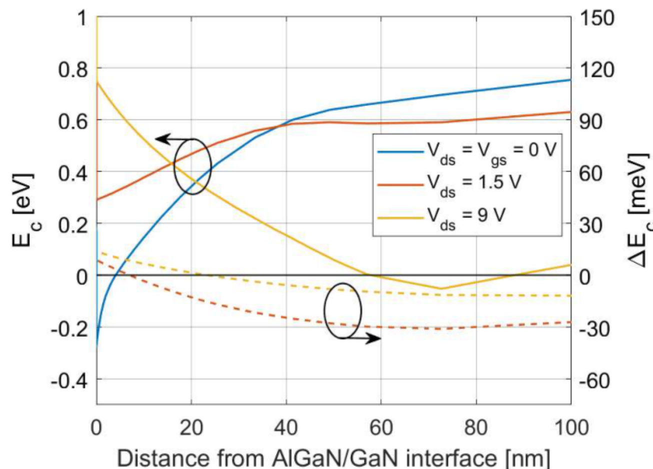

Fig. 4. Conduction band profile (left y-axis) and conduction band profile change (right y-axis) after a change in V_{th} and V_{ds} at the source side of the gate.

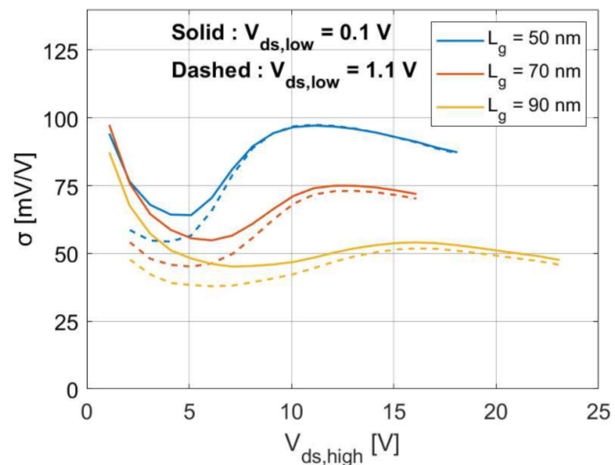

Fig. 5. The conventional method of calculating the DIBL parameter at different reference voltages using HEMTs with three different gate lengths.

result in more trapped electrons in the buffer, facilitating better gate control and a reduced overall DIBL [24]. Moreover, a HEMT with a longer gate length requires a larger increase in V_{ds} to lower E_c at the source side of the gate to force a current through the resistive buffer. This leads to a reduction of the minimum value and maximum value of σ_{DCIT}, and a $\sigma_{DCIT.max}$-shift toward higher V_{ds}.

In Region III ($V_{ds} > 10$ V), σ_{DCIT} tend to decrease and converge as V_{ds} increases (Fig. 2). In this voltage range, the electron concentration and current density expand further into the buffer and towards the drain contact (Fig 3e-f). The electron concentration at the AlGaN/GaN interface in the access region is increasingly depleted of electrons, effectively extending the depleted channel length toward the drain. At the same time, Fe trap occupation expands vertically and laterally towards the drain side as the electrons are displaced into the buffer. The extended depletion of the channel region forces a large V_{ds} change to maintain $I_{d,th}$. In other words, the effective barrier lowering in the channel region is small relative to a change in V_{ds}. As V_{ds} increases, the depleted channel region is broadened further, resulting in an overall decreasing DIBL (Fig. 2). In the measured HEMTs (Fig. 1), this decrease in DIBL is also accompanied by a high gate leakage current. The applicability of the DIBL parameter will be discussed further for this region in Section D.

C. DIBL characteristics using the conventional method

The conventional method (Eq. 1) was used to obtain the σ-V_{ds} dependence for HEMTs with three gate lengths (L_g = 50 nm, 70 nm, and 90 nm) over a large V_{ds}-range (Fig. 5). The reference voltage $V_{ds,low}$ was set to 0.1 V and 1.1 V, while the $V_{ds,high}$ varied from $V_{ds,low}$ until $I_{d,th}$ was out of the measurement range ($V_{th,high} < -3$ V). Depending on the choice of $V_{ds,high}$ and $V_{ds,low}$, σ can vary between 54 and 97 mV/V, 45 and 73 mV/V, 38 and 52 mV/V for the HEMTs with 50, 70, and 90 nm gate length, respectively.

The DIBL parameter σ display a similar trend as σ_{DCIT} in Fig. 1. However, the absolute value between the two definitions can differ by up to a factor of 2. The reason for this is that σ_{DCIT} approximates the derivative of V_{th} (with respect to V_{ds}), whereas σ reflects the change relative to some fixed reference voltage. The new definition (σ_{DCIT}) is more sensitive to small local changes in the V_{th}-V_{ds} characteristics. Moreover, σ can differ by 10-20 mV/V at low $V_{ds,high}$, depending on the chosen reference voltages ($V_{th,low}$,$V_{ds,low}$). This difference can become even larger depending on whether the ($V_{th,low}$,$V_{ds,low}$) is in the resistive or in the saturation region. These somewhat arbitrarily chosen reference voltages can complicate comparison between different technologies and make inter-lab comparisons difficult.

A large difference between σ_{DCIT} and σ can also be seen at high voltages. The reason is that the V_{th}-V_{ds} characteristics tend to level out in these devices, which results in a small derivative (and therefore a small σ_{DCIT}). The conventional definition will instead express the rate of change with respect to some set of reference voltages, which is usually set close to the resistive region. This result in a larger DIBL value. Another downside of measuring V_{th} over an extensive range of V_{ds}'s through the transfer characteristics is that it requires many measurements, which results in long measurement times. This also makes it unsuitable together with Eq. 2. Additionally, the cumulative off-state stress time over many measurement sweeps can cause charging of traps in the buffer or at the barrier surface, which affect V_{th} [25] [26].

D. Impact of gate current

It becomes increasingly difficult to estimate DIBL using Eq. 1 or Eq. 2 when I_g constitute a significant part of the injection current since DIBL manifest itself as a drain-source leakage current. Elevated gate leakage currents are common in FETs – especially at high V_{ds} – due to the high electric field at the drain side of the gate [27].

In the HEMT with an L_g = 50 nm (Fig. 1), I_g constitute less than 10 % of the injection current in the range V_{ds} = 5-10 V but increases to 37 % and 54 % at 20 V and 30 V, respectively. At V_{ds} higher than 30 V, I_g gradually increases and then saturates at 80 % of $I_{d,th}$. At this point, the transistor resembles a reverse-biased Schottky barrier diode, where the current is dependent on field emission and thermionic emission through the barrier formed at the metal-semiconductor interface, rather than by a

reduced barrier height in the channel region. The decline and convergence of DIBL in Fig. 1 is likely affected by this increase in gate current.

No I_g limit was applied to the measurements in Fig. 1. However, limiting I_g to a fixed percentage of the drain injection current in the measurement system is recommended if σ_{DCIT} is to reflect DIBL more accurately. This value should preferably be between 10-30 % of the drain current to exclude the impact of the gate-drain barrier lowering effect on σ_{DCIT} without ending the measurement prematurely. Furthermore, setting a limit to the gate current also reduces the risk of destructive gate-drain breakdown caused by the high electric field at the edge of the gate.

V. CONCLUSIONS

A new method of assessing DIBL in HEMTs is demonstrated. The main advantage of this method is the ability to easily measure the V_{ds} dependence of V_{th} at a fixed drain current corresponding to the threshold current. The measured voltages are used to calculate DIBL as a slope between neighboring measurement points. The method is demonstrated on AlGaN/GaN HEMTs with a Fe-buffer and different gate lengths. Significant local variations of DIBL observed for short channel HEMTs is likely caused by a potential barrier lowering in the buffer layer. These variations cannot easily be monitored using the conventional method. At high V_{ds}, DIBL is reduced due to an effective increase in channel region length through a lateral and vertical displacement of electrons at the AlGaN/GaN interface to the Fe-doped buffer.

The choice of reference voltages used in the conventional method may significantly impact the evaluation of DIBL, especially in regions with considerable V_{th}-variations. A large gate current can also influence the threshold voltage behavior at high V_{ds}. This can be prevented by limiting the gate current in the measurement system.

With these aspects taken into consideration, we believe that this measurement technique facilitates comparisons of DIBL between different publications by using a graphical comparison, as opposed to a fixed numerical value which has been obtain using two sets of reference voltages ($V_{th,low}$,$V_{ds,low}$) and ($V_{th,high}$,$V_{ds,high}$). From the DCIT, it is also possible to extract the maximum rate of change in V_{th} ($\sigma_{DCIT,max}$) at its corresponding V_{ds}, which can be used as a figure of merit for comparisons between different III-nitride technologies.

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