Table-Based Total Power Consumption Estimation of Memory Arrays for Architects

Minh Q. Do, Per Larsson-Edefors, and Lars Bengtsson

Department of Computer Engineering, Chalmers University of Technology,
SE 41296 Gothenburg, Sweden
{minh,perla,labe}@ce.chalmers.se

Abstract. In this paper, we propose the White-box Table-based Total Power Consumption (WTTPC) estimation approach that offers both rapid and accurate architecture-level power estimation models for some processor components with regular structures, such as SRAM arrays, based on WTTPC-tables of power values. A comparison of power estimates obtained from the proposed approach against circuit-level HSPICE power values for a 64-b conventional 6T-SRAM memory array implemented in a commercial 0.13-um CMOS technology process shows a 98% accuracy of the WTTPC approach.

1 Introduction

Nowadays, as a result of CMOS technology scaling, leakage power dissipation has become a significant portion of the total power consumption in deep-submicron VLSI chip [1]. The 2001 International Technology Roadmap for Semiconductors (ITRS) predicts that by the 70-nm generation, leakage may constitute as much as 50% of total power dissipation [2]. Thus, it is really important for architects to have the ability to rapidly estimate, with sufficient accuracy, both dynamic and static power consumption of the architectural design while exploring several alternatives searching for the optimal one.

Leakage power consumption due to subthreshold leakage currents is closely related to the physical behavior of MOS transistors, the type of circuitry involved and the process technology parameters. Therefore, it can only be accurately estimated by using circuit-level power estimation-simulation tools like SPICE, PowerMill, etc. However, due to the large number of circuit-level nodes, the complexity and time required to perform power estimation at this level are prohibitively large making rapid analysis of large designs impractical. In contrast, architecture-level tools provide faster results as compared with circuit-level ones while sacrificing accuracy.

Recently, some research have been directed towards developing models for estimating dynamic and static power consumption at architectural design level. Wattch is a collection of architecture-level power models that are based on the Simple-Scalar toolset (together with CACTI 2.0) which is commonly used to model micro-architectures in educational and some research environments [3]. Wattch divides the main microprocessor units into four categories, i.e. array structures, CAMs, combinational logic, and clocking, and then uses activity-based statistical power estimation models to produce the power estimates. Nevertheless, since Wattch uses a simple

E. Macii et al. (Eds.): PATMOS 2004, LNCS 3254, pp. 869–878, 2004.
© Springer-Verlag Berlin Heidelberg 2004

technology scaling mechanism to scale down from 0.8-um to 0.1-um technology and since Wattch does not have any model to efficiently estimate static power consumption, it has relatively poor accuracy compared to circuit-level power estimation tools, especially for deep-submicron technologies. Butts and Sohi [4] proposed a genetic, high-level model for micro-architecture components. The model is based on a key design parameter, K_{design}, capturing device type, device geometry and stacking factors that can be obtained based on simulations. This model of subthreshold leakage accurately addresses some different issues affecting static power in such a way that it makes it easy to reason about leakage effects at the micro-architectural level. However, it turns out not to be well suited for some types of SRAM circuits with power-saving and leakage-reduction techniques like MT-CMOS, Gated-Vdd, and Drowsy Cache. Also, it was never released as publicly available software. Parikh *et al.* [5] developed an architectural model for subthreshold and gate leakage that explicitly captures temperature, voltage, and parameter variations. This model was implemented in the micro-architectural HotLeakage simulation tool based on Wattch and the Cache-decay simulator. This was an attempt to develop the methodology of Butts and Sohi to address the effect of temperature on leakage power consumption. However, the accuracy of the leakage power estimation for any complex circuit structures like memory arrays, caches, etc., is unknown. Another effort to develop further the methodology of Butts and Sohi is the work by Mahesh *et al.* [6]. In this work, the authors developed analytical models parameterized in terms of high-level design parameters to estimate leakage power in SRAM arrays. An error margin of "less than 23.9%" compared to HSPICE power values is achieved by this method.

Schmidt *et al.* [7] developed an automatic black box memory-modeling approach based on nonlinear regression, which intends to combine good *model properties* (i.e. accuracy, speed, etc.) with good *modeling properties* (i.e. automatism, fit to design flow, low overhead and IP protection). Nevertheless, this approach offers its advantages at the price of a complex and computationally expensive model characterization phase. For typical memory arrays whose regular *internal structures* are known and can easily be analyzed, a white box modeling approach (e.g. our WTTPC approach) can be a good alternative to the black box one, offering a simpler and faster model characterization phase.

In [8] Eckerbert *et al.* presented a methodology to accurately estimate total power consumption (including static power) at the RT-level using simulation-based power estimation models. The methodology takes into account the changes in the component environment, which occur between characterization and estimation. By separating the different power dissipation mechanisms this methodology achieves high degrees of accuracy in estimating power consumption. Although it is a complex and accurate, RT-level simulation approach and it mainly focuses on estimating total power consumption of complex components, such as arithmetic-logic circuits, it still serves as a good hint for us. Furthermore, this methodology can be used together with our proposed approach, where necessary, providing an architecture-level solution to the problem of estimating total power consumption of all processor components.

In this paper, we propose the White-box Table-based Total Power Consumption estimation approach (WTTPC) that offers accurate architecture-level power estimation models for some processor components with regular structures, such as SRAM arrays, based on tables of power values. The structure of these tables is created before the characterization based on the structure of the component (since this is a white-box approach), while the actual simulation values are entered during the characterization.