

# 1 The ALICE Pixel Readout Upgrade

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2 **Valerio Sarritzu<sup>a,\*</sup> on behalf of the ALICE collaboration**

3 <sup>a</sup>*Università e INFN*

4 *Cagliari, Italy*

5 *E-mail: [valerio.sarritzu@ca.infn.it](mailto:valerio.sarritzu@ca.infn.it)*

6 The ALICE experiment at CERN is developing an upgrade of the three innermost layers of the Inner Tracking System (ITS3) to be installed during the Long Shutdown 3 of the LHC (2026–28). Based on a commercial 65 nm CMOS imaging technology for monolithic active pixel sensors, it consists of truly cylindrical wafer-scale bent stitched detectors that can be installed as close as 18 mm to the interaction point and will dramatically reduce the material budget in the region close to the interaction point to 0.05%  $X_0$  per layer. This contribution provides an overview on the development of sensor readout for prototypes based on the 65 nm technology within the context of the ITS3 upgrade R&D, as well as an outlook on the final readout system, including requirements, plans, and current advancements.

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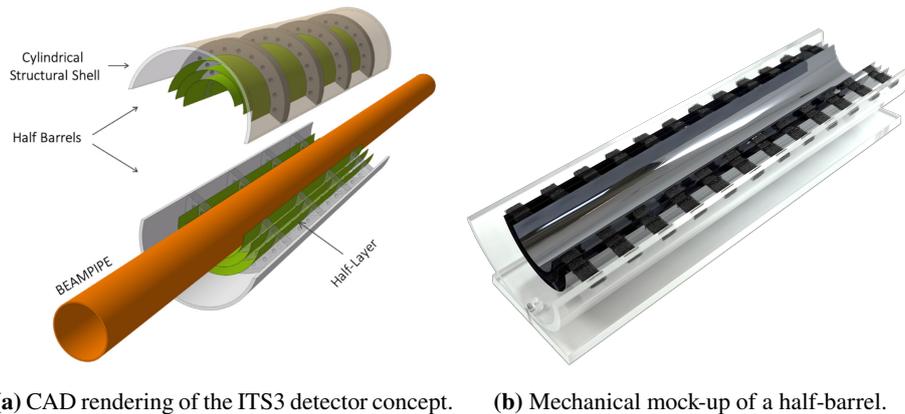
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\*Speaker

## 1. Towards a truly cylindrical inner tracker

A novel vertexing detector is currently under development, which will replace the three innermost layers of the Inner Tracker System of the ALICE experiment at CERN during the Long Shutdown 3 of the LHC (2026–28) [1]. The concept is based on wafer-scale bent CMOS monolithic active pixel sensors manufactured in a new 65 nm technology developed by Tower Partners Semiconductor Co. (TPSCo). It will consist of three truly cylindrical layers wrapped around the beam pipe, with the closest one at a radial distance of 18 mm from the interaction point.

This design is enabled by a process called *stitching* [3] used to manufacture sensors that are much larger than the design reticle, which normally measures approximately  $3 \times 2 \text{ cm}^2$ . The layout of the photomask is structured into subunits that are lithographed onto the wafer over adjacent locations according to a predefined pattern with accurate translations and alignment. By repeating the subunits in space and interconnecting them at the abutment boundaries, chips can be produced with diagonals close to the wafer diameter, that is up to 300 mm in length. The stitched sensor then undergoes dicing and thinning to below  $50 \mu\text{m}$ , with the latter being the key to take advantage of the flexible nature of silicon [5]. These large sensors can be wrapped around the beam pipe, as shown in the CAD drawing in figure 1a. A mechanical mock-up of a half-barrel built with dummy chips is shown in figure 1b, with layers measuring 280 mm in length and 56, 75, and 94 mm in width from innermost to outermost.



**Figure 1:** The ITS3 detector design concept. Layers measure 280 mm in length and 56, 75, and 94 mm in width from innermost to outermost.

This upgrade aims to provide a substantial reduction of the material budget from the current  $0.35\% X_0$  of the ITS2 to approximately  $0.05\% X_0$  per layer in the region close to the interaction point [1, 6]. It is expected to provide a factor two improvement and a 30% improvement on the impact parameter resolution for charge-particle tracks with  $p_T = 1 \text{ GeV}/c$ . This will significantly improve the measurement of low-momentum charm hadrons and low-mass dielectrons in heavy-ion collisions at the LHC, which are among the main goals of the ALICE physics program in the next decade.

An intensive R&D effort is currently ongoing, and some milestones have already been achieved. A first submission in TPSCo 65 nm named Multi-Layer Reticle 1 (MLR1) was received in summer 2021 and focused on a large number of small prototype structures in different processing flavors as a

35 test of the technology. The following Engineering Run 1 (ER1) submission was completed in autumn  
36 2022 and includes the first prototypes of wafer-scale stitched sensors, with an expected delivery  
37 by mid-2023. Two additional submissions labeled Engineering Run 2 (ER2) and Engineering Run  
38 3 (ER3) are in the planning stage with a target for completion of second half of 2023 and 2024,  
39 respectively, and will include full-scale sensors as prototypes for the final system.

## 40 2. MLR1 Test System

41 The TPSCo 65 nm technology needs to be thoroughly verified both in terms of radiation  
42 hardness and pixel performance for high-energy physics applications. For this reason, MLR1  
43 included a large number of dies in different processing flavors that provided crucial insight and  
44 input for the design of larger and more complex structures.

### 45 2.1 Test structures of MLR1

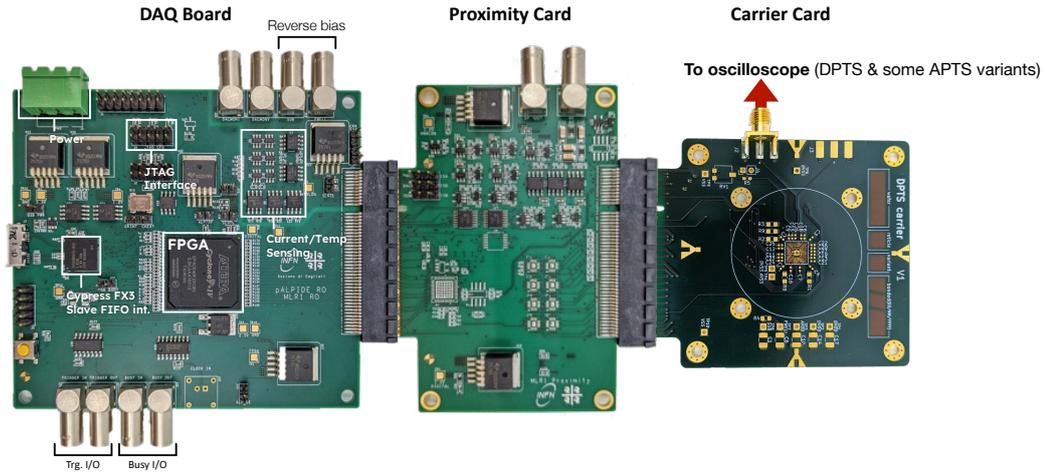
46 Among the numerous structures in MLR1, the following were of particular significance in  
47 testing different design options:

- 48 • APTS is a  $6 \times 6$  pixel matrix with pixel pitch of 10–25  $\mu\text{m}$ . It has an analog front-end with  
49 parallel analog output from the central  $4 \times 4$  pixels. Produced in almost fifty variants, its  
50 purpose is to finely test the parameters of the technology itself.
- 51 • DPTS is a larger matrix of  $32 \times 32$  pixels with a pitch of 15  $\mu\text{m}$ . It has a digital front-end  
52 that outputs the time-encoded position of the hit pixels and it is instrumental to test in-pixel  
53 discrimination.
- 54 • CE65 is an even larger matrix available in different sizes up to  $64 \times 32$  pixels with pitch  
55 of 15  $\mu\text{m}$ . It has an analog front-end with a single-output rolling-shutter readout. This  
56 structure is intended to test large-scale matrices and get preliminary information of the  
57 tracking capabilities.

### 58 2.2 Readout system

59 A portable readout system (figure 2) has been developed to characterize and test some of the  
60 chips of MLR1. Given the hundreds of sensors to test, one of the main goals was an inexpensive  
61 readout system, which allowed the distribution of approximately fifty units to collaborating institutes  
62 for a joint characterization effort. The starting point for the design was the data acquisition (DAQ)  
63 board for ALPIDE [8], the sensor currently used in the ITS2, that was revised for the operation of  
64 MLR1 sensors.

65 A proximity card plugged into the PCIe connector of the DAQ board provides features that  
66 are specific to the chip being operated via 28 digital I/Os of adjustable logic voltage (1.5–3.3 V),  
67 which were not part of the original ALPIDE DAQ board design. For APTS, all 16 pixels are  
68 sampled simultaneously at up to 4 MHz by eight dual-channel ADCs. DPTS requires a  $\sim$ GHz  
69 bandwidth, which exceeds the DAQ board capabilities, so the output is sent to an oscilloscope  
70 through a SMA connector located on the carrier card. The output is recorded and then decoded by  
71 the host computer. The proximity card also provides an output for the analog monitoring of pixel



**Figure 2:** MLR1 test system, from left to right: the FPGA-based DAQ board, the chip-specific proximity card, and chip carrier card.

[0,0]. CE65 is sampled by a single-channel 16-bit ADC at an adjustable sampling frequency up to 40 MHz, with a readout phase with respect to steering that can be tuned in 1 ns increments. A custom carrier card hosts the actual chips and is plugged into the proximity card, with power and digital or analog signals carried via a PCIe connector.

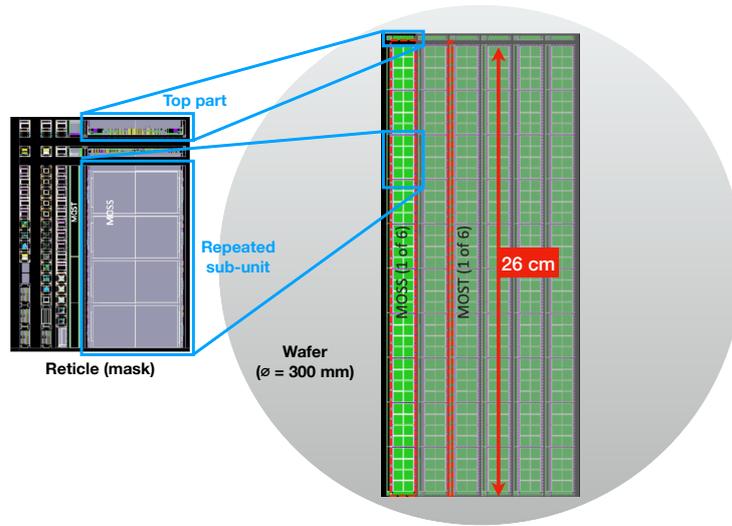
### 3. ER1

The ER1 submission includes two large stitched sensors named Monolithic Stitched Sensor (MOSS) and Monolithic Stitched Sensor with Timing (MOST) that are built, as shown in figure 3, by joining ten subunits only limited in length by the size of the reticle, measuring approximately 25 cm. Both have digital front-ends with a different approach in the readout design, as described in the following sections.

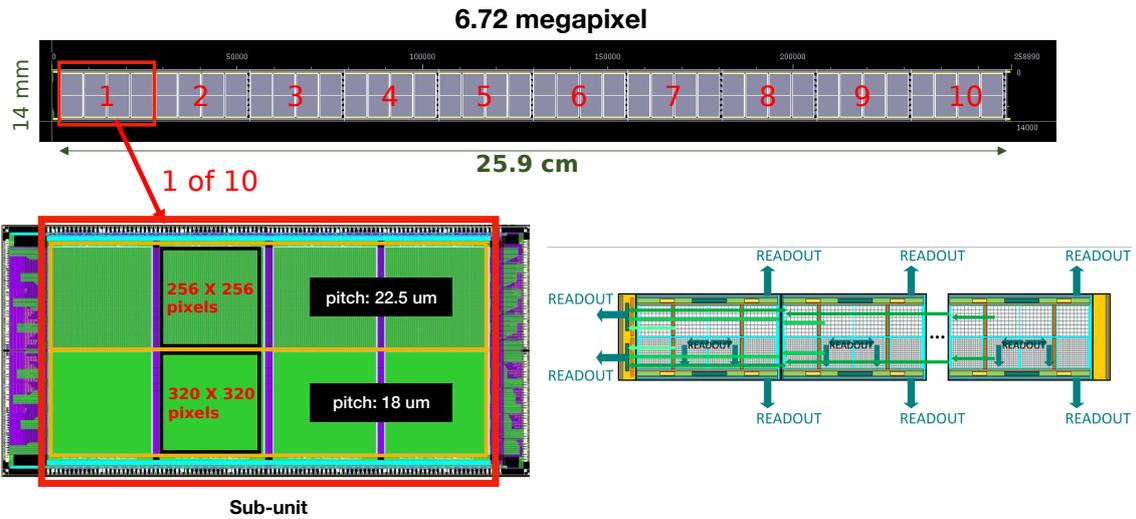
#### 3.1 MOSS

The MOSS is a 6.7 megapixels sensor, measuring  $1.4 \times 25.9 \text{ cm}^2$ . As shown in figure 4, each of its ten subunits is composed of two half-units (*top* and *bottom*) that are also the power segmentation domains. Each half-unit contains four matrices, with a pixel pitch of  $22.5 \mu\text{m}$  at the top and  $18 \mu\text{m}$  at the bottom, and a pixel count of  $256 \times 256$  and  $320 \times 320$  pixels respectively.

The chip features a binary zero-suppressed readout with parameterizable strobe duration that sequentially encodes the addresses of pixels containing hits. Pixels can be masked and feature analog charge injection and digital pulse testing. Readout requests are sent over the serial slow control and the data can be read out either locally from a single half-unit via 8-bit synchronous port or from the sensor as a whole chip, provided that the stitching works, via a 4-bit synchronous bus on the left endcap. On-chip signal relaying and regeneration ensure successful long-range transmission over the considerable length of the chip. Eighteen bits are needed per matrix per hit for the encoding, that is nine bits for the row address and nine bits for the column address. The data is packaged into an event according to the structure detailed in table 1.



**Figure 3:** Stitched sensors included in the Engineering Run 1 submission: Monolithic Stitched Sensor (MOSS) and Monolithic Stitched Sensor with Timing (MOST).



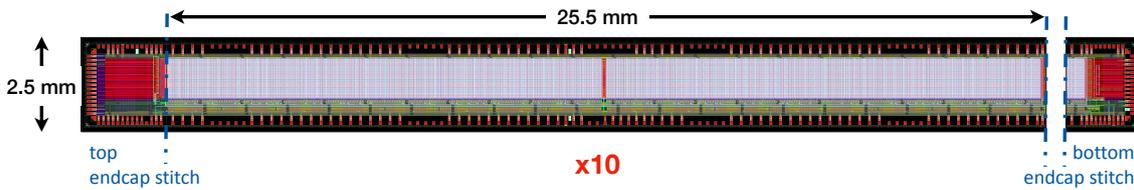
**Figure 4:** MOSS structure and readout paths.

96 **3.2 MOST**

97 As shown in picture 5, the MOST measures  $0.25 \times 25.5 \text{ cm}^2$  and its design features an event-  
 98 driven asynchronous readout, schematically presented in picture 6. The data is time-stamped,  
 99 which allows for measurements of time of arrival and time over threshold. Its structure is based on  
 100 independent groups of four pixels organized in 64 columns. Each pixel group is equipped with a  
 101 ring oscillator and a shift register to injecting serial hit data on shared transmission lines, of which  
 102 there are four per column. The serial hit data are tagged with column ID by column encoders at chip

Word	Word Size	Binary data
IDLE	8 bits	1111_1111
UNIT_FRAME_HEADER	8 bits	1101_<unit_id[3:0]>
UNIT_FRAME_TRAILER	8 bits	1110_0000
REGION_HEADER	8 bits	1100_00_<region_id[1:0]>
DATA_0	8 bits	00_<hit_row_pos[8:3]>
DATA_1	8 bits	01_<hit_row_pos[2:0]>_<hit_cln_pos<8:6>
DATA_2	8 bits	10_<hit_cln_pos<5:0>

**Table 1:** Data packets included in an event according to the MOSS communication protocol.



**Figure 5:** MOST structure. Note that only one of the ten subunits is shown here, for the purpose of better illustrating a design of an extremely thin aspect ratio.

103 bottom periphery, after which the transmission lines are merged, reducing the number of required  
 104 channels from 256 to four. The data is then sent off chip by four current-mode logic output buffers.  
 105 The maximum data rate on the bus in the matrix is 2 Gb/s, and since data is transferred directly to  
 106 one of the four outputs, the maximum data rate per output is 2 Gb/s. Decoding of hit data is not  
 107 included in the MOST prototype.

108 The MOST architecture presents a series of trade-offs. The higher power granularity reduces  
 109 the number of pixels or the size of the sectors that need to be powered down in case of defects. The  
 110 dead-area is also reduced as the readout is distributed in active matrix area, and it is more power  
 111 efficient at low hit rates, as it requires no strobing or clock distribution. However, drawbacks include  
 112 the need to have asynchronous decoding off-chip at data rates up to 2 Gbit/s, which requires more  
 113 development, potentially requiring oversampling to compensate for group transmission mismatch.  
 114 The asynchronous sharing of transmission lines might lead to hit data packets colliding at high hit  
 115 rates, thus incurring potential data loss, although it could be mitigated by parallelism and interleaved  
 116 geometry of pixel groups.

### 117 3.3 MOSS Test System

118 A dedicated test system for MOSS has been developed. The main goals for the readout system  
 119 revolve around testing the very first large sensor design with stitching for high-energy physics. More  
 120 specifically, all of its basic features need to be accessible with the goal to assess manufacturing  
 121 yield and design for manufacturability, and functional yield at half unit, block, column/row/pixel  
 122 level granularity. It also needs to provide proper mechanical support for a huge and delicate chip  
 123 in a variety of use cases, e.g. lab testing or test beams. The concept for the test system is shown in  
 124 figure 7 and it is based on three different types of boards:

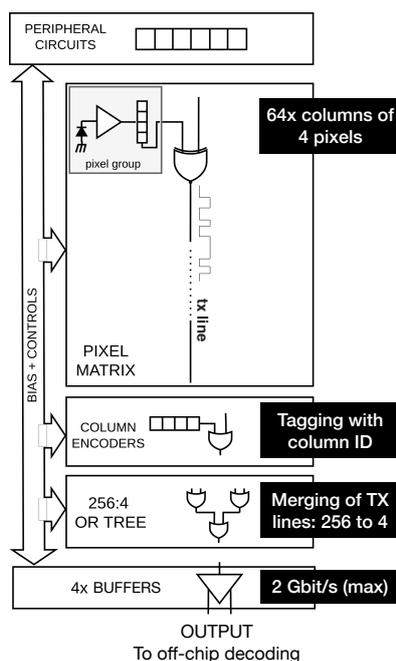


Figure 6: MOST readout flow.

- 125 • A *carrier card*, used to host and connect the MOSS chip as shown in figure 8a. The board
- 126 provides access to all features of the chip via five 560-pin connectors located along its
- 127 perimeter. As shown in figure 8b, four connectors are dedicated to the chip’s four quadrants,
- 128 each containing five independently operable half-units. A fifth connector operates the chip
- 129 as two halves via the stitched backbone.
  
- 130 • Five *proximity cards*, one to control and read out each quadrant, and one for the whole top
- 131 and bottom halves via the stitched backbone.
  
- 132 • *Automation and readout modules* to steer the proximity boards and interface the sensor control
- 133 and readout with a computer.

134 All active components have been acquired and a prototype is currently under validation, with

135 the goal of commissioning by the time the chips are delivered in mid-2023.

#### 136 4. Final Readout

137 Due to the design for the final chip being in its very early stages, the specifics of the final

138 readout system have yet to be delineated. However, some preliminary considerations can already

139 be made at this stage, on the bases of which some important R&D has already started. This section

140 outlines the ITS readout requirements and summarizes the work that is currently being carried out

141 on some key components of the final readout system.

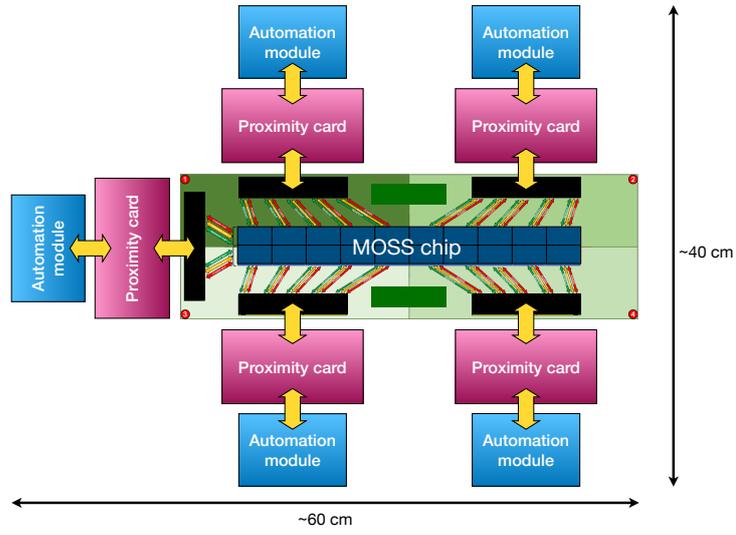
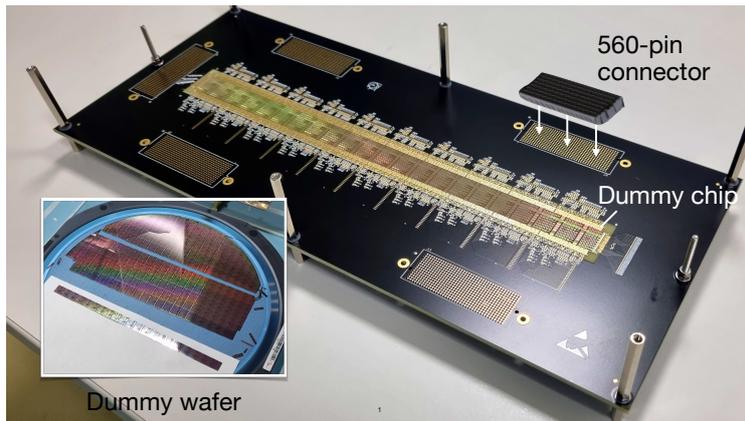
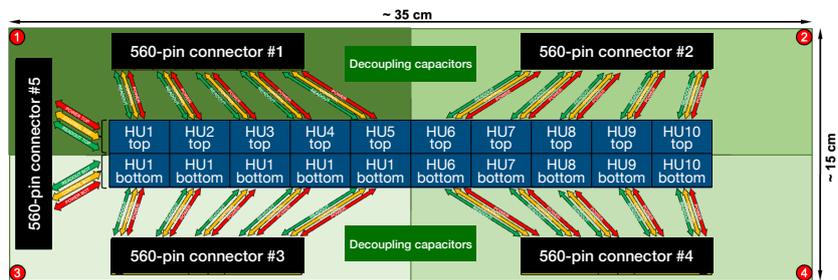


Figure 7: MOSS test system concept.



(a) Prototype with a bonded dummy chip.



(b) Connection scheme.

Figure 8: MOSS carrier board.

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## 142 4.1 Requirements and plans

143 The Inner Layers of ITS3 will be closer to interaction point with the innermost one moving  
 144 from a radial distance of 23 mm to 18 mm, which results in a 70% flux increase as shown in table 2.  
 145 This translates to a rate of 2.2 MHz cm<sup>-2</sup> for Pb–Pb collisions at 50 kHz, which is already within  
 146 the capabilities of the current ITS. Furthermore, the minimum integration time of its sensors is 1  
 147 microsecond, so there is already the margin for the ITS2 to operate well beyond a rate of 100 kHz  
 148 for Pb–Pb collisions. The main conclusion that can be drawn from this data is that the readout units  
 149 and power distribution system of the ITS2 can be reused for the ITS3, with considerable savings in  
 150 terms of budget.

Layer	Particle density (cm <sup>-2</sup> )			
	ITS2		ITS3	
	Hadronic <sup>a</sup>	QED electrons <sup>b</sup>	Hadronic <sup>a</sup>	QED electrons <sup>b</sup>
L0	43	7	73	12
L1	25	3	43	8
L2	17	2	29	6

**Table 2:** Comparison between expected maximum particle rates in the layers of the ITS2 and ITS3 inner barrel.

<sup>a</sup> Maximum particle density in central Pb–Pb collisions (including secondaries produced in material) for a magnetic field of 0.2 T.

<sup>b</sup> For an integration time of 10 μs, an interaction rate of 50 kHz, and a magnetic field of 0.2 T.

## 151 4.2 Current R&D

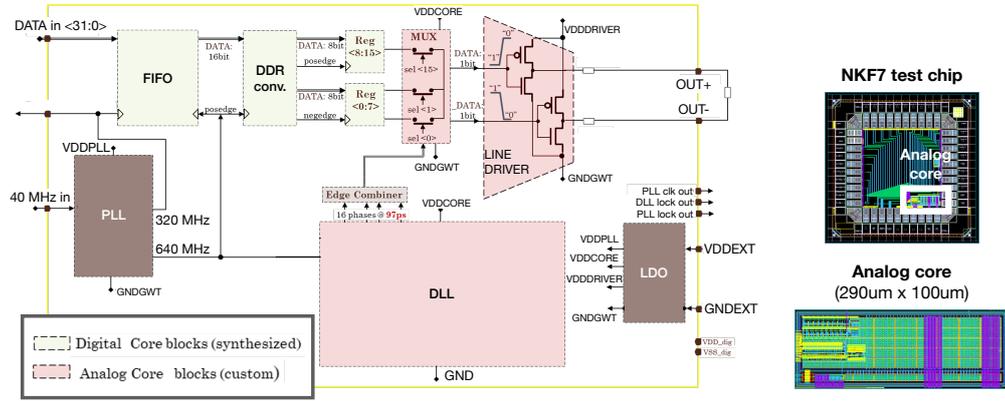
### 152 4.2.1 Serializer

153 A serializer is in development under the name GWT-PSI with a target for data rates up to 10.24  
 154 Gbps and the added advantage of a fairly contained power budget, operating at around 24 mW. The  
 155 main blocks in the design, shown in figure 9a, are a synthesized digital core and a custom analog  
 156 core. A prototype of the latter (figure 9b) has been submitted with ER1 and it includes features that  
 157 will be instrumental to its characterization, such as adjustable data rates in the range 1.28–10.24  
 158 Gbps and preset pattern generation. Testing will start as soon as the ER1 submission is delivered.

### 159 4.2.2 Flexible printed circuit

160 In order to route the signals of the ITS3, a custom flexible printed circuit (FPC) has been  
 161 designed that can suit the cylindrical shape of the tracker. Figure 10 shows a rendering of how the  
 162 installed FPC will look within the mechanical support frame around the beam pipe.

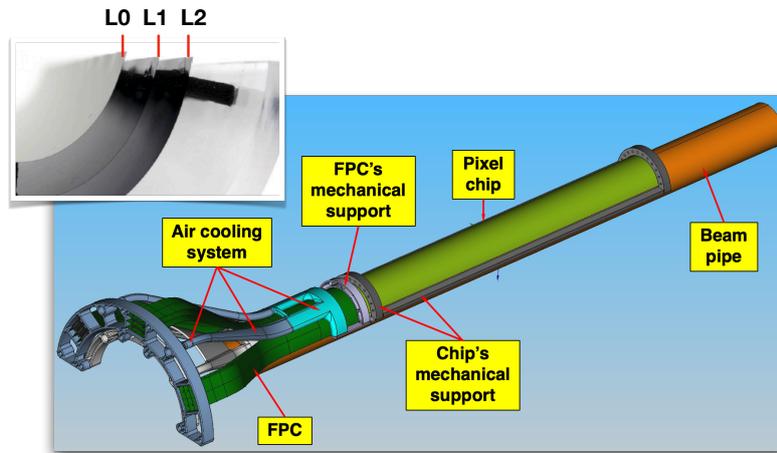
163 Since each layer covers a different area depending on the radial distance from the interaction  
 164 point, the requirements for the FPC also depend on the layer. In order to accommodate this, the  
 165 sensors are partitioned in 18 mm stripes, each requiring eight lines for the data, one for the clock and  
 166 two for control. The bandwidth requirements are about 5 Gbps per link for the data and on the order  
 167 of a few tens of MHz for the CLK & CTRL lines. Table 3 summarizes the overall requirements for  
 168 each layer. A prototype has been produced and testing will start shortly.



(a) Design blocks.

(b) Analog core test chip.

**Figure 9:** GWT-PSI serializer block diagram and layout. Notable features include data rates up to 10.24 Gbps, no high-frequency external clock needed (a 40 MHz input is sufficient to generate the internal 320 and 640 MHz clocks), bypassable clock-cleaning PLL (ring-oscillator) with internal jitter below 30 ps peak to peak, and built-in power-supply-cleaning LDO.



**Figure 10:** Flexible printed circuit.

Layer	Size	Data Lines	Clock Lines	Control Lines
L0	54 mm	24	3	6
L1	72 mm	32	4	8
L2	90 mm	40	5	10

**Table 3:** Lines required in the FPC for data, clock, and control, for the three layers of the ITS3.

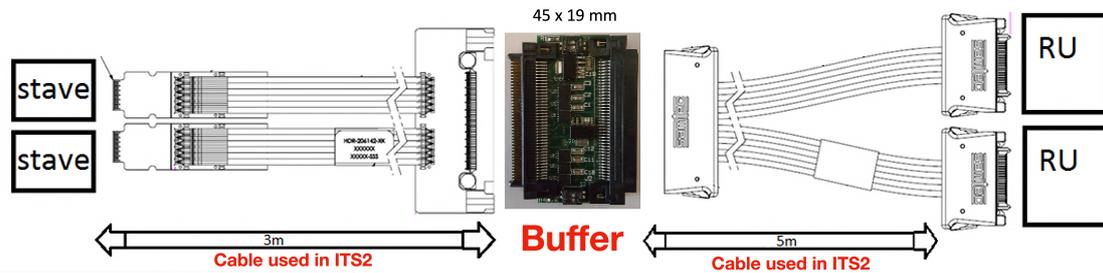
### 169 4.2.3 Cables and repeaters

170 As discussed in section 4.1, cables from ITS2 are in principle compatible with ITS3. To further  
 171 test their limits, a more in-depth study has been conducted on the data rate realistically achievable  
 172 between the staves and readout units currently in operation in the ITS2. The setup is schematically  
 173 shown in figure 11.

174 The maximum data rate achievable by the cables is 2 Gbps. A decision feedback equalizer  
 175 (DFE) provide a minor improvement by amplifying the high frequency component of a signal  
 176 without amplifying the noise content. When the DFE is enabled, 2.5 Gbps is feasible but the  
 177 communication fails at 3 Gbps. A buffer has been developed to achieve a major improvement in  
 178 data rate up to 6 Gbps, with the DFE having little to no impact. The results of the various connection  
 179 scenarios are summarized in table 4.

Buffer	DFE	Maximum Data Rate
no	no	<2 Gbps
	yes	2.5 Gbps
yes	no	6.25
	yes	Gbps

**Table 4:** Summary of the maximum data rate achievable by the cables used in ITS2 in different configurations.



**Figure 11:** Test setup for measuring the data rate achievable with the ITS2 cables when using a buffer between the staves and readout units.

### 180 4.3 Engineering Run 2 & 3: first full-size sensors

181 The ER2 submission will include the first full-size sensor, that will be the actual prototype of  
 182 the final sensor (including its readout) for ITS3. The work has started but it is at a very preliminary  
 183 stage. ER3 will contain the final ASIC for installation and commissioning.

## 184 5. Conclusion and Outlook

185 The ITS3 upgrade will provide the ALICE experiment with a truly cylindrical inner tracker.  
 186 Its bent wafer-scale sensors are based on a new 65 nm technology by TPSCo. The first steps in  
 187 the R&D program involved the characterization of small ( $1.5 \times 1.5 \text{ mm}^2$ ) test structures that were  
 188 produced with the MLR1 submission in many different flavors. A custom test system was developed  
 189 for this purpose, and the workload is shared by collaborating institutes over three continents.

190 The next submission (ER1) includes the first wafer-scale sensors with two different designs.  
191 The MOSS is the largest sensor, whereas the MOST is designed with a different approach, providing  
192 more granular power segmentation, less dead area, and better power efficiency, with some tradeoffs  
193 such as the need for off-detector decoding the possibility of data loss at high hit rates. A test system  
194 for the MOSS is currently under validation, with the goal of having it commissioned by the time  
195 the ER1 wafers are delivered in mid-2023.

196 An outlook has been provided on the final readout, which is expected to sustain a data rate  
197 approximately twice that of the ITS2. Power and readout units are compatible with the ITS3,  
198 whereas some ancillary components have been purposefully designed and prototyped. A serializer  
199 is included in the ER1 submission and will be tested as soon as it is delivered. A signal repeater  
200 has also been developed to reuse existing cables at a bandwidth up to 6.25 Gbps by buffering the  
201 signal midway. A custom FPC has been designed to provide signal routing to the cylindrical sensors  
202 according to the expected bandwidth requirements and a prototype is in production for validation.

203 The design of the new sensor is now entering its very early stages but the feedback from ER1,  
204 which is primarily intended to learn about stitching, will be crucial before the submission of the  
205 next chip. ER2 and ER3 will include, respectively, the first full-scale prototype of the final sensor  
206 and the final ASIC to be installed in the ITS3.

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POS(Pixel2022)027