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Development of a Macro-Pixel sensor for the Phase-2 Upgrade of the CMS experiment

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Part I.

Introduction and Basics

1 Introduction

The natural curiosity of mankind has always led us to build ever better and larger instruments to better understand the world around us. This is no different with particle physicists and their search for elementary particles and forces that have been predicted by their theories. For almost a century now, they have been building particle accelerators with ever higher energies to generate these particles and the necessary experiments to detect them or their decay products. All these efforts culminate in what is currently the world's largest and most powerful particle accelerator, the Large Hadron Collider (LHC) at the European Organization for Nuclear Research (CERN) near Geneva in Switzerland. The LHC and its experiments have now been running for ten years, including various maintenance phases, before they went into the currently ongoing Long Shutdown (LS2) to prepare the accelerator and the experiments for the upcoming three year long Run 3, in which the center of mass energy and the instantaneous luminosity of the colliding proton beams will be increased to a new record of 14 TeV and $2 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, respectively. Probably the greatest achievement of the LHC and two of its four main experiments, ATLAS and the Compact Muon Solenoid (CMS), within the last ten years is the discovery of the long predicted Higgs boson with a mass of 125 GeV in 2012 [CMS12b] [ATL12]. In 2024, the LHC and the experiments will enter the third Long Shutdown (LS3), in which the accelerator will be upgraded to the High Luminosity LHC (HL-LHC) that is able to provide twice or even three times the instantaneous luminosity that is targeted for Run 3. After ten years of operation, the HL-LHC will thereby approximately tenfold the existing data set, which will increase the discovery potential of ATLAS and CMS as well as their ability for more accurate precision measurements of known couplings between particles. Both approaches can provide new evidence for so far undiscovered processes, like physics beyond the Standard Model or supersymmetry.

The enormous particle rate and density that result from the increased instantaneous luminosity will set new requirements on all the detectors and their individual components. Especially the all-silicon tracker of CMS, the innermost system of the detector closest to the interaction point, has to withstand enormous radiation damage and deal with the highest particle fluence. For that reason, new radiation hard silicon sensors and readout chips have to be developed that are able to operate under such harsh conditions throughout the entire lifetime of the detector. Furthermore, due to the increased number of high-energy particles in the detector, current trigger criteria, which are necessary to reduce the number of recorded events that are read out of the detector, will no longer be efficient enough to ensure a maximum manageable trigger rate of about 750 kHz [CMS17c] at the collision frequency of 40 MHz. Therefore, CMS also decided to include track information from the Outer Tracker into their first stage of trigger system. However, due to the limited bandwidth and processing time only a small amount of data can be passed to the trigger system at the collision frequency. To achieve this, a new Outer Tracker layout had to be developed, that includes modules which either comprise two silicon strip sensors (2S) or a combination of a strip and a macro-pixel sensor (PS). By comparing the the offset of the hit coordinates in the two sensor layers due to the curvature of the particle track in the presence of the magnetic field, each module is able to identify charged particles with a transverse momentum larger than 2 GeV/c. Only the hit coordinates and the track curvature of these high momentum particles are sent to the trigger system at every bunch-crossing of

the accelerator. While 2S modules will be mounted in the outer part of the Outer Tracker, PS modules with their shorter strip sensor and the pixelated layer are going to be installed in the inner part of the detector volume. The resulting higher granularity reduces the occupancy of the modules and provides additional z information for the tracking algorithms. However, choosing a macro pixel sensor over a second strip sensor also poses a number of challenges that have to be addressed. In contrast to strip sensors for example, pixelated sensors have to rely on a comprehensive biasing scheme to connect each individual pixel to the all-surrounding bias ring, which is necessary to test the sensor before assembling it with a readout chip. These biasing structures will not be connected to any amplification circuit in the final module and thus introduce additional inefficient areas in the pixel matrix, which could impair the overall performance of the detector. For this reason, special attention must be paid to this topic during the development of a pixelated sensor in order to find the optimal compromise between testability and reliable as well as efficient operation of the sensor. This thesis is dedicated to these kind of considerations and the development of the first full-size macro-pixel sensor for the PS modules of the future CMS Outer Tracker: the PS-p.

In Chapter 2 and 3 of this work, the LHC and the CMS experiment, together with the Phase-2 Upgrade of the Outer Tracker are introduced. The introduction is supplemented by a brief description of silicon sensors and the effects of radiation damage in Chapter 4. The subsequent main part of this work is split into two major topics.

The first topic is dedicated to the characterization of the first small macro-pixel prototypes that have been produced by CiS in Germany: the PS-p light. In Chapter 5, the methodology and the results of extensive laboratory measurements of these sensors are presented. These measurements allow to determine all important sensor parameters that are necessary to qualify the sensor material and to verify whether the sensors comply with the electrical specifications defined by the CMS Outer Tracker sensor community. After the characterization in the laboratory, some of the sensors have been assembled with dedicated readout chips, to form a fully functional particle detector, called Macro-Pixel SubAssembly (MaPSA) light. These assemblies have been operated in an electron beam to verify the sensor design by locating any possible inefficient areas in the pixel matrix. Such an electron beam is operated by the DESY research center in Hamburg, Germany. Their test beam facility, together with the measurement procedure, the analysis chain as well as the results of the efficiency measurements are presented in Chapter 6. These measurements revealed that the area between the pixel rows show severe inefficiencies that are caused by the aluminum rails of the biasing structure. This information is used as a starting point for a comprehensive Technology Computer Aided Design (TCAD) simulation study to develop an improved design of the existing PS-p light, which is presented in Chapter 7. In this process, the maximum electric field in the silicon bulk as well as the position dependent charge collection efficiency of the various sensor layouts has been determined. The final elaboration of an optimized design for the future PS-p marks the end of the first topic of this thesis and concludes the investigation of the PS-p light prototype.

The second major topic of this thesis is devoted to the design and qualification process of the first full-size PS-p as well as several smaller single sensors that are placed on the same prototype wafer. Chapter 8 starts with the design process of this PS-p prototype wafer, including two standard full-size sensors and eight single sensors with four different layout variations that are based on the results of the preceding TCAD simulations. These single sensors will be equipped with only one instead of 16 readout chips, like the full-size sensor, and are intended for a sensor design study to find an optimal layout for the final PS-p. In Chapter 9 the focus is set on the laboratory measurements of these various PS-p sensors on the prototype wafer. In order to determine the performance of the various sensor designs, a selection of single sensors has been subsequently assembled with their corresponding readout chip and investigated in an electron beam, similar to the PS-p light and the MaPSA light. In Chapter 10, the results of

the hit efficiency analysis of the various assemblies are presented. The measurements have been performed with both, unirradiated as well as irradiated assemblies, to simulate the condition of the detector after 10 years of operation at the HL-LHC.

The final Chapter 11 summarizes the results of both parts of this thesis and concludes with an outlook on the last steps that are necessary to select the final sensor material and design for the PS-p.

2

The Large Hadron Collider and the CMS experiment

The Large Hadron Collider (LHC), located at the European Organization for Nuclear Research (CERN) near Geneva in Switzerland is the largest and most powerful particle accelerator ever built. It is able to accelerate two counter-rotating proton beams up to an energy of 6.5 TeV each, which are brought into collision at four **I**nteraction **P**oints (IPs) along the ring. Each of the four IPs is enclosed by a particle detector which is designed to reliably detect the collision products and, among other things, determines their energy and transverse momentum (p_T). One of these four detectors is the Compact Muon Solenoid (CMS) experiment which is described in the following section together with the LHC [CER17].

2.1. The Large Hadron Collider (LHC)

The LHC is located in a 26.7 km long circular tunnel which runs at a depth between 45 m and 170 m below the surface. The tunnel was built between the years 1984 and 1989 to originally house the LHC's predecessor, the Large Electron Positron Collider (LEP). After eleven years of operation, the CERN council decided to discontinue and disassemble the LEP collider in order to clear the tunnel for the Large Hadron Collider, whose construction began in 2000 and ended in 2008 [EB08].

Unlike the LEP collider, the LHC accelerates protons (hadrons) instead of electrons and positrons (leptons) which leads to a reduced energy loss by synchrotron radiation, the main limiting factor of a lepton synchrotron at such high energies. Synchrotron radiation is emitted by charged particles that are deflected in a magnetic field due to the Lorentz force. The total power emitted by synchrotron radiation depends on the mass m_0 and energy E of the particle as well as the accelerator radius r [Mes15].

$$P = \frac{e^2}{6\pi\epsilon_0 (m_0 c^2)^4} \cdot \frac{E^4}{r^2} \tag{2.1}$$

Although the LHC's center of mass energy is about 60 times higher, the power loss caused by synchrotron radiation is about six orders of magnitude lower compared to LEP. The main limiting factor of the LHC, on the other hand, is the magnetic field, generated by the superconducting bending magnets that are necessary to keep the particles on their track along the ring. Nevertheless, with a maximum magnetic field of about 8.3 T, the LHC is still able to reach a center of mass energy of $\sqrt{s} = 14\,\text{TeV}$. However, due to limitations of the dipole magnets, the protons have to be pre-accelerated to an energy of 450 GeV before they can be injected into the LHC [EB08]. For that reason, the LHC is embedded in the CERN accelerator complex, which is shown in figure 2.1.

A list of the proton accelerators together with the corresponding maximum achievable kinetic energy of the particles is given in table 2.1.

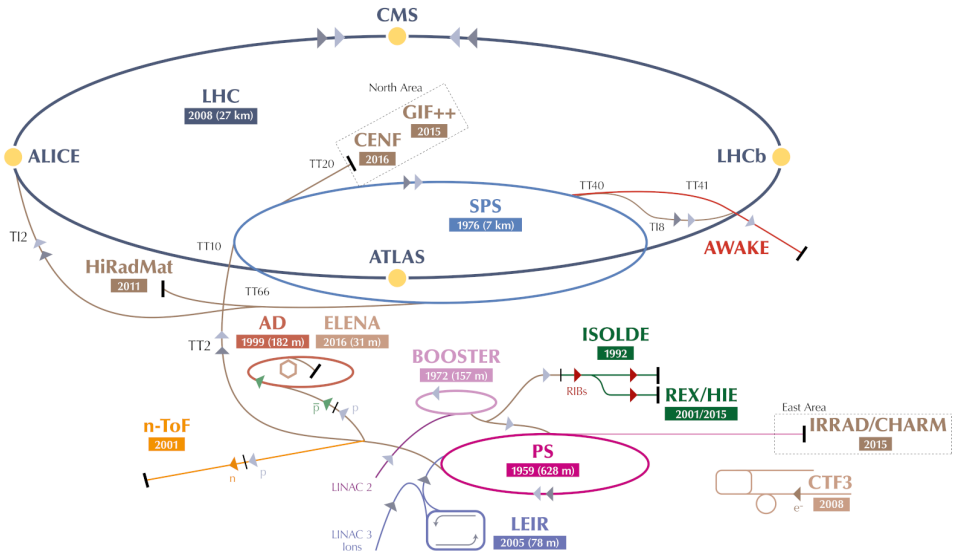


Figure 2.1.: The CERN accelerator complex. Protons are starting at the LINAC 2 accelerator and are injected into the Proton Synchrotron Booster (Booster) which pass the proton bunches to the Proton Synchrotron (PS). As soon as the protons reach an energy of 25 GeV they are injected into the Super Proton Synchrotron (SPS) where they get accelerated one more time to reach the LHC injection energy of 450 GeV. The LHC then accelerates the protons up to their final collision energy of 6.5 TeV [Mob16].

Table 2.1.: Proton accelerator chain together with the maximum kinetic energy of the particles in the corresponding accelerator [CER17].

Accelerator	Kinetic energy
Linear Accelerator (Linac) 2	0.05 MeV
Proton Synchrotron Booster (Booster)	1.4 GeV
Proton Synchrotron (PS)	25 GeV
Super Proton Synchrotron (PSP)	450 GeV
Large Hadron Collider (LHC)	6.5 TeV

The protons are accelerated in small packages called *bunches* that contain up to 1.2×10^{11} particles each. When the LHC is fully filled, each of the two proton beams is storing up to 2808 of these bunches. After acceleration, the proton bunches are brought into collision at four interaction points where the four main experiments are located. The bunch crossing rate at these points is 40 MHz. By focusing the beam, hence reducing the cross section A of the bunches right before they cross each other, the particle density and therefore the probability of a particle interaction increases. All these parameters lead to one of the most important quantities to express the accelerator performance besides the beam energy: the instantaneous luminosity $\mathcal{L}$, which is given by:

$$\mathcal{L} = \frac{n \cdot N_1 \cdot N_2 \cdot f}{A}, \tag{2.2}$$

where n is the number of bunches per beam, N_1 and N_2 the number of protons of the two colliding bunches respectively, f the revolution frequency of a single bunch and A the cross section of the particle beams [HM18]. The LHC is designed to reach an instantaneous luminosity of $\mathcal{L} = 1 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ which leads to an average of 1 billion proton-proton collisions per second or 25 collisions per bunch crossing [EB08]. Since May 2018 the LHC already doubled this value and was continuously running at a peak luminosity of $\mathcal{L} = 2 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ through 2018 [CER18a]. The reason why machine engineers are driving the luminosity to ever higher limits is the direct correlation between the luminosity and the number of events per second $\frac{dN}{dt}$ of a certain type of event:

$$\frac{dN}{dt} = \mathcal{L} \cdot \sigma_p \tag{2.3}$$

with the production cross section σ_p, a measure of the probability that a certain process p occurs. By integrating the event rate over the operation time, the total number of expected events can be calculated as

$$N_p = \int_0^T \mathcal{L}(t)\,\sigma_p\,\mathrm{d}t = \mathcal{L}_{\mathrm{int}}\ \sigma_p \tag{2.4}$$

which leads to the integrated luminosity $\mathcal{L}_{\mathrm{int}}$:

$$\mathcal{L}_{\mathrm{int}} = \int_0^T \mathcal{L}(t)\,\mathrm{d}t. \tag{2.5}$$

This means that a long operation time at a high instantaneous luminosity leads to a high number of collisions at the interaction points. The integrated luminosity can therefore be interpreted as the total amount of data which has been delivered by the accelerator. For that reason, the amount of data recorded by the experiments is usually expressed in units of the integrated luminosity (fb^{-1}) [HM18].

2.2. The Compact Muon Solenoid (CMS) experiment

The four main experiments that are located at the four interaction points of the LHC are: ATLAS[1] [ATL08], LHCb[2] [LHC08], ALICE[3] [ALI08] and the Compact Muon Solenoid (CMS) experiment. CMS, like the ATLAS experiment, is designed to serve as a general purpose detector that covers a wide range of physics objectives, including Higgs physics, the search for phenomena beyond the Standard Model (BSM), extra dimensions and many more [CMS08].

[1] A Toroidal LHC Apparatus
[2] LHC beauty
[3] A Large Ion Collider Experiment

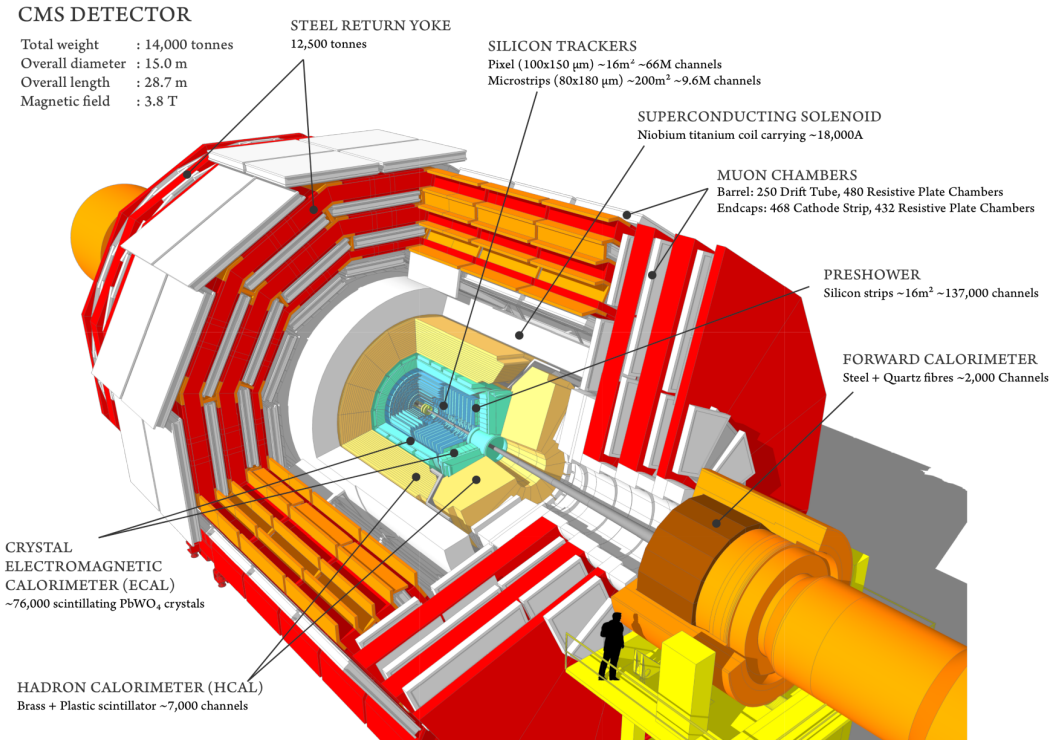


Figure 2.2.: Illustration of the Compact Muon Solenoid (CMS) detector. From the interaction point in the center to the outer layer in the barrel region: Silicon Tracker for track reconstruction of charged particles, Electromagnetic Calorimeter (ECAL) and Hadronic Calorimeter (HCAL) for energy reconstruction, superconducting solenoid to generate a magnetic field of 3.8 T and the Muon Chambers together with the iron return yoke. In the forward region the detector is complemented by the Preshower and the Forward Calorimeter [Tay11].

An illustration of the CMS detector is shown in figure 2.2. Over 5000 people employed by almost 200 different institutes located in 45 countries and regions around the world are involved in this experiment [CMS]. Their tasks include the development, construction and operation of the detector as well as the processing and analysis of the recorded data.

In 2012, all this finally led to the discovery of the long predicted and last missing piece of the Standard Model, the Higgs boson, by the CMS and ATLAS collaborations [CMS12b] [ATL12]. In order to perform such and similar high precision measurements, the detector has to fulfill several requirements [CMS08]:

- full spatial coverage of the interaction point,
- an excellent track reconstruction efficiency and momentum resolution of charged particles,
- efficient b- and τ-tagging capability with the help of a detector very close to the interaction points,
- high muon detection efficiency, momentum resolution and charge identification in the region $|\eta| < 2.5$[4],

[4] the pseudorapidity η is defined as $-\ln(\tan(\theta/2))$, where η describes the angle between the particle and the z axis which runs parallel to the beam.

- good energy resolution of charged leptons, hadrons and leptons in an electromagnetic and hadronic calorimeter with a large spatial coverage up to $|\eta| < 5$.

However, it is almost impossible for one single detector technology to meet all these requirements at once. Therefore, the CMS detector comprises several sub-detectors that are specialized in one or few of these required tasks:

Muon system

The muon system of the CMS detector is based on three different, but complementary, gaseous chamber technologies: **D**rift **T**ubes (DT) in the barrel region, **C**athode **S**trip **C**hambers (CSC) in the two endcaps and **R**esisitve **P**late **C**hambers (RPC) in both, the barrel and the endcap. All three subsystems are embedded in the iron return yoke of the solenoid magnet which acts as additional absorber material inside the muon system to reliably separate muons from all other particles. The muon system encloses all other sub-detectors as the outermost system of the CMS detector. More information about the CMS muon system can be found in [CMS97c].

Solenoid magnet and iron return yoke

The centerpiece of the CMS detector is the superconducting solenoid magnet, which is necessary to bend high energetic charged particles inside the comparably small detector volume and determine their momentum. The four-layer niobium-titanium (NbTi) coil conducts a total current of almost 20 kA and stores a total energy of up to 2.6 GJ. The resulting 3.8 T magnetic field is returned by the iron return yoke that runs through the muon system. With a mass of 12 500 t the iron return yoke is the main contributor of CMS' total mass [CMS08].

Hadronic calorimeter (HCAL)

The hadronic calorimeter (HCAL) is responsible for absorbing and measuring the energy of hadrons such as neutrons, protons, pions and kaons. The HCAL is a sampling calorimeter made out of plastic scintillators and brass absorber plates. This combination guarantees that all hadrons are stopped inside the brass plates by generating showers of secondary particles whose scintillation light are detected by photodiodes connected to the scintillator plates. More information about the Hadronic Calorimeter is summarized in [CMS97b].

Electromagnetic calorimeter (ECAL)

Electrons, positrons and photons, which mainly interact electromagnetically, are absorbed by the Electromagnetic Calorimeter (ECAL). The detector consists of over 76000 scintillating lead-tungstate crystals ($PbWO_4$) that enclose the silicon tracking detector completely. Due to the high density of $\rho = 8.28\,\mathrm{g\,cm^{-3}}$ and the short radiation length of $X_0 = 0.89\,\mathrm{cm}$, the ECAL can be operated without any additional absorber material. The scintillation light emitted by the crystals is detected by avalanche photodiodes and vacuum phototriodes that are mounted at the end of every crystal. More information about the ECAL is given in [CMS97a].

Silicon Tracker

The innermost subsystem close to the interaction point of the CMS detector is the all-silicon tracker, shown in figure 2.3.

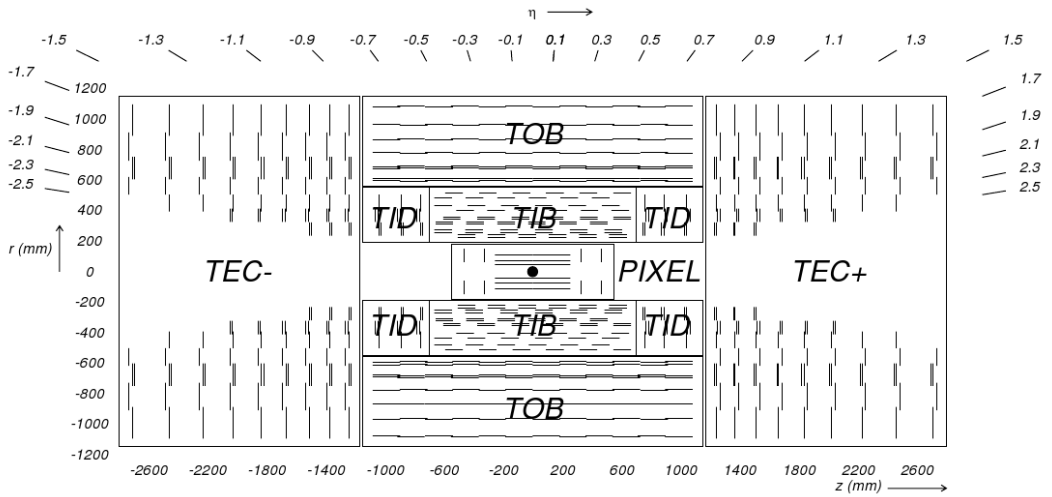


Figure 2.3.: Schematic cross section of the current CMS Tracker. The tracking system consists of pixel and strip sensor modules. The innermost layers, close to the interaction point, are covered by pixel modules. The Outer Tracker, which is composed of strip sensor modules, is divided into five different parts: Tracker Inner Barrel (TIB), Tracker Inner Disk (TID), Tracker Outer Barrel (TOB) and two Tracker End Caps (TEC- / TEC+). Since 2017, the pixel detector comprises four barrel layers and three disks per endcap instead of the three barrel layers and two end cap disks that are shown here [CMS08].

Overall, the CMS tracking system covers an active area of over $200\,\mathrm{m}^2$ which makes it the largest silicon tracking device ever built [Kar+97]. A dense arrangement of silicon sensors ensures that enough space points are provided for a reliable track reconstruction. However, only charged particles are able to generate a signal in the silicon sensors, making the detector blind for neutral particles that have to be detected by either the electromagnetic or the hadronic calorimeter. The Lorentz force guarantees that charged particles are deflected in the magnetic field and forces them onto a bent trajectory instead of a straight line. The transverse momentum p_T of the particle can then be determined by reconstructing the trajectory and the radius perpendicular to the proton beams:

$$p_T \left[\frac{\mathrm{GeV}}{\mathrm{c}}\right] = 0.3\, B[\mathrm{T}]\, R[\mathrm{m}] \tag{2.6}$$

with the magnetic field strength B in Tesla and the radius of the trajectory R in meters. As the curvature gets smaller with increasing energy of the particles, the reconstruction of the radius gets more inaccurate and hence the momentum resolution decreases.

The reconstructed tracks are also used to determine the vertices of the particles. This is essential to assign the particles to their corresponding point of origin, which is particularly challenging in the environment of the LHC. A collision rate of 40 MHz at the design luminosity of $1 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ can lead to 20–30 primary vertices resulting in over 1000 tracks in the detector volume during one single bunch-crossing. At a distance of approximately 4 cm from the beam pipe, this translates into a particle hit rate of about $1\,\mathrm{MHz/mm}^2$ and decreases to $3\,\mathrm{kHz/mm}^2$ at the edge of the tracker ($r = 115\,\mathrm{cm}$) [CMS08]. In order to still be able to reliably separate the tracks and interaction points from each other, the interaction region is enclosed by a high granularity pixel detector that is capable of separating vertices with an accuracy of 40 µm to 50 µm. The current pixel detector

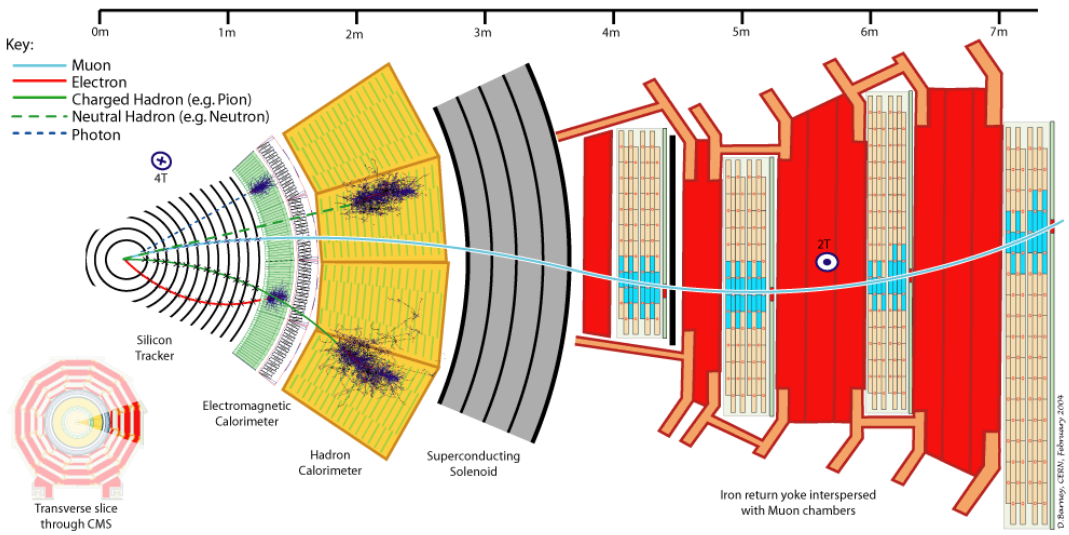


Figure 2.4.: Slice of the CMS detector. The interaction point on the left side is the point of origin of all particles. Neutral particles (dashed lines) like photons and neutral hadrons do not interact with the Tracker and will be absorbed in the electromagnetic and hadron calorimeter. Charged particles (solid lines) like electrons and charged hadrons are bent inside the magnetic field and interact with the silicon layers of the tracking system. Muons are the only particles that hardly interact with any subsystem and can reach the muon system outside the solenoid. The curvature of their trajectories changes, as the polarity of the magnetic field also changes at the solenoid [Dav16].

consists of four cylindrical layers in the barrel region and two endcaps with three layers of pixel modules each [CMS12a].

As the distance to the interaction point increases, the need for high granularity detectors becomes less important. Hence, the CMS collaboration decided to use more cost saving strip instead of pixelated sensors at $r > 200\,\text{mm}$, reducing the number of readout channels by a factor of twelve compared to the pixel detector, while covering 99 % of the total active area of the tracker. The strip tracker is divided into five different sections that are arranged around the pixel detector. The two innermost sections are the Tracker Inner Barrel (TIB) and the Tracker Inner Disk (TID) which form a similar geometry as the pixel detector. Both sections and the pixel detector are again surrounded by the Tracker Outer Barrel (TOB) and the two Tracker End Caps (TEC+ and TEC-). In total, the CMS strip tracker consists of more than 15 000 modules that cover a pseudorapidity range up to $|\eta| < 2.5$.

Overall, the CMS detector is 28.7 m long, 15 m in diameter and weighs about 14 000 t, making it the heaviest of the four main experiments at the LHC [Tay11].

2.2.1. Particle identification in the CMS detector

As it has already been indicated, all different subsystems of the detector are specialized to one or few tasks. Only the combination of all sub-detectors leads to a precise identification of the emerging particles. Figure 2.4 shows a small slice of CMS' cross section and illustrates how five exemplary particles are identified by the detector.

One of the simplest signatures is generated by photons. Without electric charge, they do not interact with the tracker and only produce showers in the electromagnetic calorimeter.

By reconstructing the shower shape, the point of origin is completely determined by the calorimeter. Neutral hadrons are also invisible for the silicon tracker but can easily pass the electromagnetic calorimeter without losing much of their initial energy. They are stopped in the hadron calorimeter and again, have to be assigned to their point of origin only by the calorimeter. Electrons, on the other hand, are electrically charged and thus can be detected by the tracking system. While they pass the tracking system, they generate Bremsstrahlung which is detected by the electromagnetic calorimeter and has to be taken into account during the energy reconstruction. Apart from that, electrons behave similar to photons and generate electromagnetic showers in the $PbWO_4$ crystals of the ECAL. The combined information of the calorimeter and the tracker leads to a very precise determination of their point of origin. Charged hadrons are detected by the tracker as well, but penetrate the ECAL and have to be stopped in the HCAL again. The only particles that are able to pass the hadronic calorimeter, and even the solenoid magnet and its return yoke, are muons. Therefore, signals that are detected in the muon system are most likely generated by passing muons. Since muons are either positively or negatively charged, the tracker will detect them as well. However, neutrinos, which barely interact with any kind of matter, cannot be detected by any of the subsystems at all. Fortunately, CMS can detect them indirectly by summing up all the transverse momenta of the remaining particles and determining a deficit, called missing transverse energy $\not{E}_T$, which can be associated with neutrinos or other weakly interacting particles. Instead of independently evaluating the information of the different systems, In order to identify and reconstruct all these particles more reliably, CMS uses a particle flow algorithm that combines the information from multiple sub-detectors instead of evaluating them independently [CMS17a].

2.2.2. The CMS trigger system

All the different sub-detectors that have been introduced in the previous section acquire data that has to be stored and analyzed. At the design luminosity of $1 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ and consequently 25 inelastic proton-proton interactions per bunch crossing, the total amount of data can easily add up to approximately 1 MByte per event [CMS08]. With the LHC bunch crossing rate of 40 MHz the data throughput would therefore equal 40 TB/s. CMS, the subsequent computer farm and data storage are not capable to read out, process and store the data at such high data rates. Therefore, CMS includes a two-stage trigger system that reduces the enormous amount of data by multiple orders of magnitude.

The first stage is the Level-1 (L1) trigger which is based on commercially available FPGAs[5] and custom made ASICs[6]. The hardware based system uses information from the calorimeters and the muon system to preselect events with predefined signatures within a timing window of 3.4 µs (L1 latency). Only these events are read out and stored in a readout buffer. This kind of preselection already reduces the read out rate of the whole CMS detector from 40 MHz down to 100 kHz [CMS17b].

To reduce the data rate even further down to a manageable and storable size, the preselected events in the readout buffer are passed to the second stage of the trigger system, the High Level Trigger (HLT). The HLT is a software based trigger system which runs on a computer cluster and therefore offers more flexibility concerning the selection criteria. Since it has access to information of all sub-detectors, the event selection can be adjusted to certain physics objectives, allowing the user to manually select more interesting events. The average data rate that has to be written to disk after the HLT is ultimately reduced to about 400 Hz [CMS17b].

[5] **F**ield **P**rogrammable **G**ate **A**rray
[6] **A**pplication **S**pecific **I**ntegrated **C**ircuit

3

The Phase-II Upgrade of the CMS Outer Tracker

Since its first light, the LHC has been improved regularly to reach ever higher energies and luminosities. Starting in 2010, the LHC began its operation at a center of mass energy of 7 TeV which was increased to 8 TeV two years later and reached 13 TeV after the first Long Shutdown (LS1) in 2015. Since then, the energy remained unchanged even after the Extended Year End Technical Stop (EYETS) at the beginning of 2017. Nevertheless, it is still planned to increase the energy one last time to LHC's design collision energy of $\sqrt{s} = 14\,\text{TeV}$ after the Long Shutdown 2 (LS2), which will be completed in 2021 [CER18d].

Similar to the center of mass energy, the instantaneous luminosity is following a ramp up sequence as well. It took the LHC almost five years to reach its design instantaneous luminosity of $\mathcal{L} = 1 \times 10^{34}\,\text{s}^{-1}\,\text{cm}^{-2}$ in 2015. During Run 2 the machine already doubled this value and pushed the current machine closer to its limits.

3.1. The High-Luminosity LHC (HL-LHC)

All accelerator based experiments rely on the amount of data that the underlying machine delivers during its runtime. In case of the LHC, the expected data for the experiments is about $300\,\text{fb}^{-1}$ until 2023. For many physics analysis, especially those that include heavy particles with masses in the order of TeV, this is not enough. Therefore, CERN decided to extend the lifetime of the LHC and the experiments until 2037 and beyond. However, in order to meet the high demand for large data sets, the LHC will be upgraded once more during the Long Shutdown 3 (LS3) between 2024 and 2026, which will increase the instantaneous luminosity by a factor of 5–7 of the nominal value and thus mark the beginning of the High-Luminosity LHC, or HL-LHC for short. The whole upgrade plan of the LHC, including the HL-LHC Phase, is shown in figure 3.1.

Assuming a runtime of approximately ten years, the HL-LHC would tenfold the data set recorded from 2011 till 2023. However, the higher luminosity is accompanied by an increased pile up and consequently higher particle density in the detectors. This will set new requirements on all the LHC experiments and their detector components.

3.2. The Phase-II Upgrade of the CMS tracker

The following sections are based on the Technical Design Report (TDR) of the Phase-II Upgrade of the CMS tracker [CMS18].

The present CMS tracker, including the pixel detector, will not be able to run for another ten years after the HL-LHC upgrade. One of the main reasons is the radiation damage that accumulates over the years and significantly impairs the performance of the silicon sensors and the associated readout electronics. However, instead of solely exchanging the tracker with a new identical one, the HL-LHC upgrade requires a number of design changes that are essential

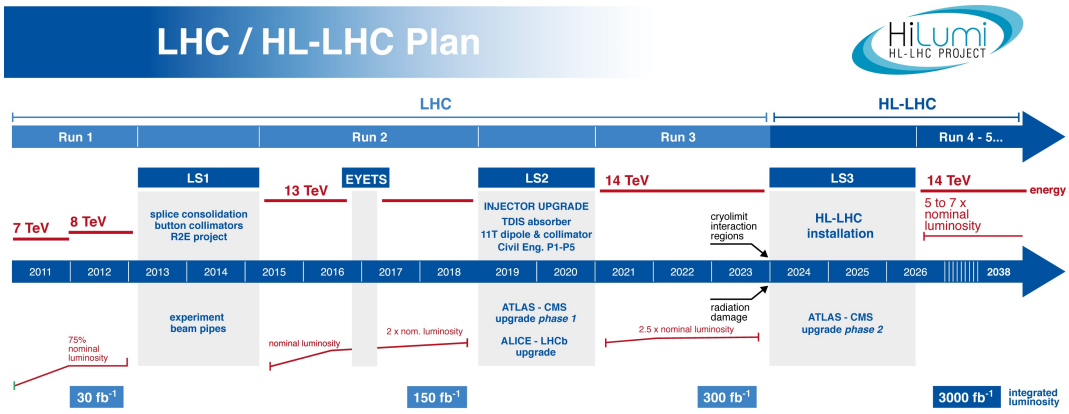


Figure 3.1.: Current upgrade plans of the LHC. The LHC already passed Long Shutdown 1 (LS1), the Extended Year End Technical Stop (EYETS) and is now in Long Shutdown 2 (LS2). The instantaneous luminosity has already been doubled compared to the nominal values and the center-of-mass energy reached 13 TeV. After LS2, the machine will run at the maximum center-of-mass energy of 14 TeV and an instantaneous luminosity of 2.5 times the nominal value. Finally, during Long Shutdown 3 (LS3), beginning in 2024, the LHC and some experiments will be upgraded once more and will enter the high luminosity phase of the LHC (HL-LHC) [CER18d].

to meet the demands set by the higher luminosity of the machine. First, the granularity of the tracker has to be increased to keep the occupancy of the readout channels below 3 % in the innermost layer of the Outer Tracker. This will ensure reliable track reconstruction even with the increased number of particle tracks in the detector volume. Second, since there is no plan to replace any parts of the Outer Tracker during the whole high luminosity phase, it is necessary that the new sensors and the readout chips are more radiation hard in order to withstand the higher particle fluences that are expected after ten years of operation. Finally, it is essential that the future CMS Outer Tracker contributes to the Level-1 trigger decision. The reason for this is based on the fact that the current selection algorithms become inefficient with increasing pile up, which can be improved by including track information in the L1 trigger decision. Together with the planned upgrade of the entire L1 trigger and DAQ system, this will keep the trigger rates below 750 kHz [CMS17c]. Although equipped with high-speed Gigabit links and high performance hardware, transferring and processing all hit information at the bunch crossing rate of LHC is simply not possible with the technology planned for the future Outer Tracker of CMS. The new Outer Tracker modules will therefore be able to select particles above a certain transverse momentum (p_T) threshold and only pass the most essential hit information to a hardware based track finding algorithm that will provide track information to the L1 trigger at the bunch crossing rate of 40 MHz. In CMS, this is realized by modules referred to as "p_T modules" that are composed of two closely-spaced silicon sensors each. More details about the p_T discrimination and the module concept will be described in the following sections.

3.2.1. The new CMS tracker layout

The most noticeable design change of the future CMS tracker is the extended tracking acceptance up to $|\eta| < 4$ compared to the present coverage of $|\eta| < 2.4$. This is achieved by an extension

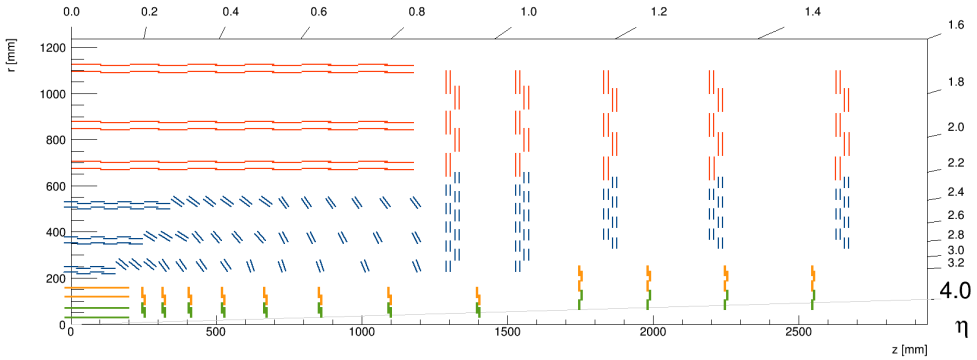


Figure 3.2.: Cross-section of one quarter of the Phase-II Outer and Inner Tracker of CMS. Each line represents a module in the detector volume. Pixel modules close to the beam pipe are marked in green (two readout chips per module) and yellow (four readout chips per module). Blue lines correspond to PS modules that are composed of a macro-pixel and strip sensor. The outer part of the tracker is covered by 2S modules (red lines) that consist of two strip sensors. The three barrel layers of the PS modules at $0.4 \leq \eta < 2.4$ are facing towards the interaction point to comply with the tilted layout proposed by the CMS collaboration [CMS18].

of the inner tracking system, by adding multiple additional discs in the very forward direction. The cross section of one quarter of the future CMS tracker is illustrated in figure 3.2.

The Inner Tracker will consist of four layers in the barrel section, two of which will include modules with two readout chips and another two layers which will consist of modules with four readout chips. Twelve additional endcap discs on each side will ensure the high spatial coverage in the forward direction. The Outer Tracker coverage, on the other hand, will remain the same after the upgrade. However, instead of relying on a combination of single- and double-sided strip modules, the Outer Tracker will consist of two different types of p_T modules. In the three outermost layers of the barrel and the outer part ($r > 700\,\text{mm}$) of the two tracker endcaps, modules with two silicon strip sensors are used, whereas the inner three layers of the barrel closer to the pixel detector as well as the inner part of the endcaps will be populated with modules composed of a macro-pixel and a strip sensor, giving them their names 2S (strip-strip) and PS (pixel-strip) modules, respectively. The strips of both sensors in the 2S modules are about 5 cm long, whereas the strips of the PS strip sensor are only about half the size of the 2S strips ($\sim 2.4\,\text{cm}$) which reduces the occupancy and increases the z resolution in those modules closer to the interaction point. The macro-pixels of the pixelated PS sensor are even shorter and are only about 1.5 mm long, which leads to an even better z resolution of the Outer Tracker. Monte Carlo simulations revealed that the initial flat barrel design[1] of the PS modules would lead to inefficiencies in the p_T discrimination due to badly overlapping modules at higher incident angles. In order to overcome this problem, the CMS collaboration decided to implement a tilted layout of the first three layers of the barrel part of the detector. This reduces the number of required PS modules in the tracker, and thus reduces its total mass and costs, and ensures that the modules are arranged in such a way that particles emerging from the interaction point traverse each module almost perpendicularly.

[1] In the flat barrel design, each module is aligned with the beam axis. Only the modules at $\eta = 0$ are simultaneously facing towards the interaction point

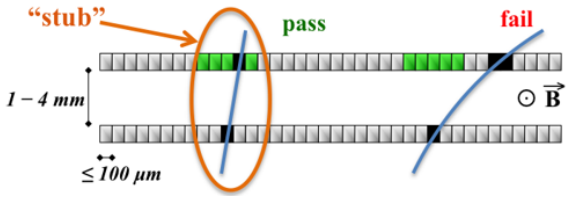


Figure 3.3.: The p_T trigger module concept. The sensor layers are arranged on top of each other at a distance of a few millimeters. Charged particles with high transverse momentum are less bent by the present magnetic field and are therefore more likely to hit the upper sensor in a small window above the hit in the lower sensor. All valid hit doublets inside this windows, called 'stubs', are sent to the Level-1 track finder at every bunch crossing to provide additional trigger information for the Level-1 Trigger [CMS18].

3.2.2. Concept of p_T trigger modules

Both types of p_T modules are based on the same p_T discrimination principle that is shown in figure 3.3.

The essential parts of each module are two closely-spaced silicon sensors that are connected to a common readout ASIC. The exact spacing between the two layers depends on the position of the module in the tracker. As a rule of thumb, the closer the modules are located to the interaction point the greater the distance between the two sensors. For the PS modules, spacings of 4.0 mm, 2.6 mm and 1.6 mm are foreseen, whereas 2S modules will only have two different spacings of 4.0 mm and 1.8 mm. When a particle traverses a module, it induces a signal in both sensor layers, resulting in two registered hits in the common readout electronics. The built-in correlation logic will then select hit pairs that pass a certain selection criteria which correlates with the transverse momentum of the particle.

The logic is based on the fact that charged particles are deflected in the 3.8 T magnetic field due to the Lorentz force (see equation 2.6). As soon as the correlation logic of the ASIC registers a hit in the inner sensor that is closer to the interaction point, it will search for a corresponding hit within a programmable correlation window in the outer sensor. Particles with high p_T have a larger radius of curvature and are therefore more likely to hit the outer sensor in the defined window. The window size is adjusted on a module by module level in such a way that only particles with $p_T > 2\,\mathrm{GeV/c}$ are able to generate such a valid hit pair. An additional programmable offset value that shifts the correlation window by several strips compensates for the fact that not all positions on the modules are oriented perfectly perpendicular to the interaction point. Up to five of these valid hit pairs per module, called "stubs", are sent to the L1 track finder at every bunch crossing. Further information about the event, including the full hit matrix, are stored in the pipeline of the chip and are only read out if a positive trigger signal is received (L1 accept). This data reduction on module level is essential to transfer only the most relevant data to the L1 track finder and ultimately include the resulting track information in the Level-1 trigger decision. The effect of p_T discrimination becomes more apparent by looking at the simulated p_T distribution of all particles per event that generate a hit in a sensor at a distance of 25 cm, which is shown in figure 3.4. By cutting on $p_T > 2\,\mathrm{GeV}/c_0$ the number of remaining hits that have to be transferred to the track finder can be reduced from $\mathcal{O}(10^5)$ down to a manageable amount of $\mathcal{O}(10^3)$.

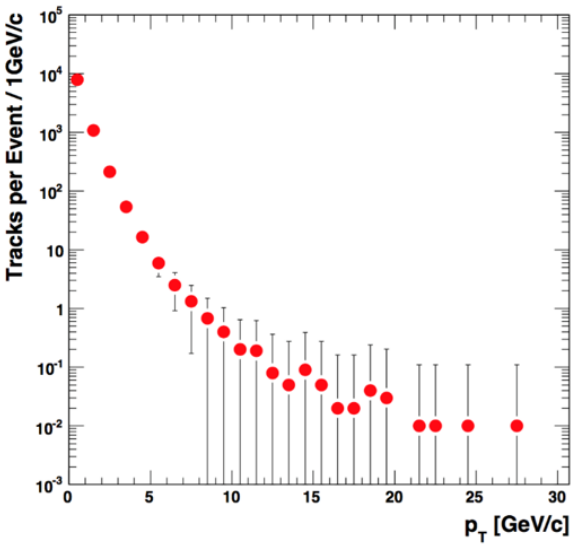


Figure 3.4.: Simulated number of tracks with a certain transverse momentum p_T per event. Only particles with $p_T > 2\,\mathrm{GeV}/c_0$ are able to generate stubs in the p_T modules. Only the stubs are sent to the Level-1 track finder, reducing the amount of data by many orders of magnitude [PH10].

3.2.3. The 2S module

The outer three layers of the barrel and the outer part of the endcap will be equipped with 2S (strip-strip) modules. A drawing of a 2S module with a 4 mm spacing between the sensors is shown in figure 3.5. The sensors of the 2S module have a size of approximately 10 cm × 10 cm whose strips are precisely aligned in parallel above each other. Even small rotations by 400 µrad between the strips of the sensor layers will cause the stub logic to fail at some points in the module and thus, making it unreliable for its trigger contribution purpose. Each sensor includes two rows of 1016 5 cm long strips with a *pitch* (distance between the center of two neighboring strips) of 90 µm. The strips are segmented in the middle of the sensor to increase the z granularity and therefore reduce the overall occupancy of the module and the tracker. All strips are read out by 16 CMS Binary Chip (CBC) ASICs [Uch+18] that are bump bonded to two flexible front-end hybrids. Each of the CBCs includes 254 readout channels that are alternately connected to the upper and lower sensor of the module. This is possible due to elongated routing lines of every second pad onto the backside of the flexible hybrid, which make them accessible for wire bonding of the lower sensor. An additional Concentrator Integrated Circuit (CIC) [Cap+18] on each front-end hybrid collects the data from eight CBCs and compresses, serializes and finally sends it to the optical converter stage on a connected service hybrid. This service hybrid includes the optical converter stage and the optical 5 Gbit link to the outside world, as well as several voltage regulators and band-pass filters to power the chips and the sensors. The Institute of Experimental Particle Physics (ETP) at KIT pledged to build 2000 of these 2S modules that will be used for one of the two endcaps of the detector. A lot of effort is put into setting up the production line and especially into the high precision equipment that is required during the alignment of the two sensors and the quality control.

3.2.4. The PS module

The complexity of the PS module is slightly larger compared to the 2S module, since it uses a macro-pixel instead of a second strip sensors. Thus, only three different sensors are used for the

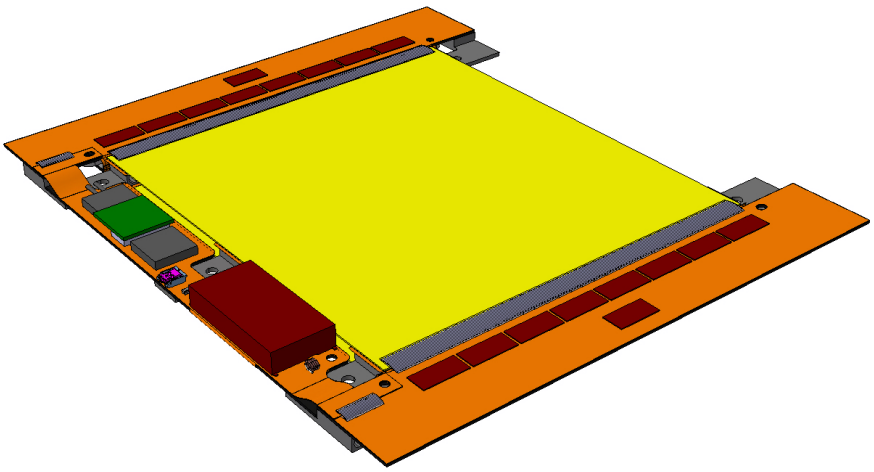


Figure 3.5.: Drawings of a 2S module with 4 mm spacing between the sensors. Every strip of the segmented sensors (yellow) is bonded to one channel of one out of 16 CMS Binary Chips (CBCs) that are placed on two front-end hybrids alongside the concentrator chip (CIC) (brown rectangles). Both front-end hybrids are connected to the service hybrid that provides all necessary voltage regulators and the optical transceiver stage to send (and receive) data to the external system [CER18b].

future Outer Tracker compared to the 15 differently shaped and sized sensors that are currently installed [CMS08]. To avoid confusion between the three different sensors for the Outer Tracker, the pixel and strip sensor of the PS module are called PS-p and PS-s, respectively. An exploded view of the PS module with a 1.6 mm spacing between the macro-pixel and the strip sensor is shown in figure 3.6.

Both sensors are about half the size ($\sim 5\,\text{cm} \times 10\,\text{cm}$) of a 2S strip sensor ($\sim 10\,\text{cm} \times 10\,\text{cm}$). A small difference of 600 µm between the length of the PS-s and the PS-p enables the possibility to use pattern recognition algorithms for the alignment of the two sensors during the assembly procedure. Similar to a 2S sensor, the PS-s consists of strips that are segmented in the middle of the sensor. Each of those 2×960 strips is about 2.4 cm long. The pitch between two neighboring strips is 100 µm and therefore slightly higher than in the 2S module (90 µm). One end of each strip is wire bonded to one of the 16 Short Strip ASICs (SSA) that are split between two front-end hybrids. The macro-pixel sensor of the PS module includes 30 208 pixels with a cell size of $100\,\mu\text{m} \times 1467\,\mu\text{m}$. The pixels are arranged in a 32×944 matrix from which 16 rows and 118 columns are connected to one readout chip, the Macro Pixel ASIC (MPA). This is done by flipping and placing the chip on top the sensor and connecting each pixel cell of the sensor to one front-end channel of the readout chip. This so-called *flip-chipping* process is the essential part of the *hybrid technology* that is used for this pixelated detector. The hybrid technology allows the chip and the sensor to be developed independently from each other in order to optimize their performance and, above all, their radiation tolerance. Small solder balls between the pixels and the corresponding front-end channel on the chip establish the conductive connection of the pixel cells. By heating up the *assembly* during this *bump bonding process*, the solder balls begin to melt and form a more stable interconnection between the sensor and the chip. In total, 16 MPAs have to be bump bonded to the sensor in order to read out one full PS-p and forming the Macro-Pixel Sub-Assembly (MaPSA).

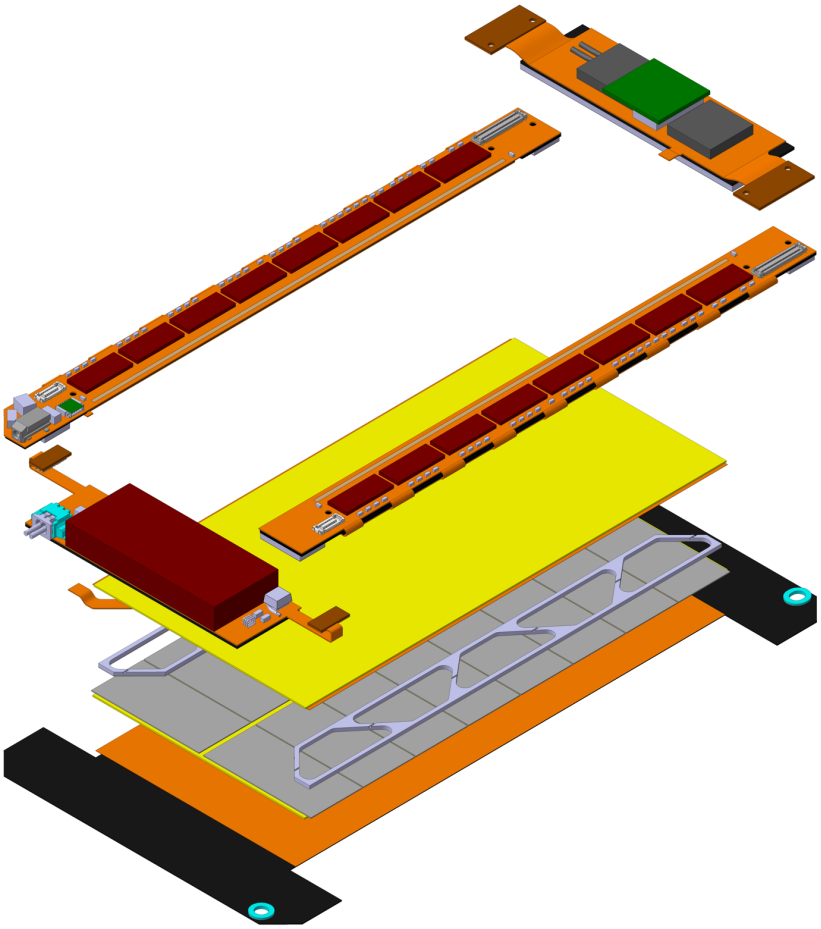


Figure 3.6.: Exploded view of a PS module with a spacing of 1.6 mm between the macro-pixel and the strip sensor. The Macro-Pixel Sub-Assembly (MaPSA), composed of a macro-pixel sensor (yellow) and 16 MPAs (gray) is placed on an aluminum carbon fiber (AL-CF) base plate (black) that is electrically insulated by a polyimide foil (orange). The MPA as well as the PS strip sensor are wire bonded to the front-end hybrids that include 8 SSAs (brown rectangles) and one CIC (on the backside). The PS service hybrid is split into a power distribution part (brown box) and a data transmission part (green box) [CER18b].

The MaPSA is the heart of the PS module which includes all important parts of the stub finding logic of the module. The SSA on the other hand does not include any stub finding logic at all. It only contains some front-end electronics, a comparator stage and a lateral communication system to exchange hit information with its neighboring chips. Thus, the hit information of the SSA has to be passed to the MPA to perform the stub finding routine. This is realized by a flexible hybrid the SSA is bump bonded onto and which is folded around a stiffener and finally wire bonded to the MPAs of the MaPSA. Similar to the front-end hybrid of the 2S module some lanes are elongated onto the backside of the hybrid to make them accessible for the MPA. However, instead of passing analog pulse signals of the sensor to the readout chip on the frontside, only digital information is transmitted between the SSA and the MPA, making the PS module less vulnerable to additional noise that can be picked up by the elongated routing lanes. Each of the two CICs receives data from eight MPAs and sends it to the optical transceiver that is placed on one of the two service hybrids. The second service hybrid houses several DC-DC converters that provide the necessary power for the readout chips and the connection for the sensor bias.

Although KIT is not involved in the production of the PS modules it is still contributing to the PS project as sensor qualification center (SQC) for all Outer Tracker sensors, including 2S and PS-s strip as well as PS-p pixel sensors. Furthermore, KIT even designed and tested several prototypes of the macro-pixel sensor whose last iteration is now defined as baseline design for the final sensor for the Outer Tracker of CMS. This thesis is dedicated to the development and validation of the PS-p sensor and covers possible improvements of its design to increase the overall efficiency of the detector.

3.2.5. The Macro Pixel ASIC (MPA) data paths

All readout chips of the future Outer Tracker, including the MPA, are designed for electron and binary readout only. As soon as a signal in the sensor exceeds an adjustable threshold in the readout chip, the output of the front-end goes to '1' or stays at '0' if not. Consequently, no information about the pulse height is stored, reducing the amount of data to a manageable size. The output of the binary readout is processed through two different data paths in the MPA: the stub and the Level-1 (L1) data path (illustrated in figure 3.7).

The stub data path is running at 40 MHz in order to provide stub information to the Level-1 track finder at every bunch crossing. The hit information of the pixel matrix is sent to a clustering circuit that bundles adjoining pixel hits and determines the center (centroid) of each pixel cluster. The resulting pixel centroid objects are passed to the stub finding logic where they get correlated with the strip centroids of the SSA. If the displacement between the strip and pixel centroid is within a user defined correlation window of up to seven strips, a stub is generated and sent to the Level-1 track finder.

At the same time, the L1 data path also receives the hit information of the binary readout and starts to process them. However, instead of passing it to the stub finding logic where most of the data gets rejected, the full event is stored in a dedicated row memory, waiting for the Level-1 accept. When a trigger is received, the data is sent to the chip periphery where it gets prepared to be sent to the CIC and the optical data transmitter on the service hybrid. The L1 data path of the MPA was chosen to be large enough to provide full event data at a maximum trigger frequency of 1 MHz and trigger latency of 12.8 µs.

3.3. Radiation environment

All parts of the CMS detector are exposed to an enormous particle flux that is linked to the high number of particle collisions resulting from the luminosity of the accelerator. In order

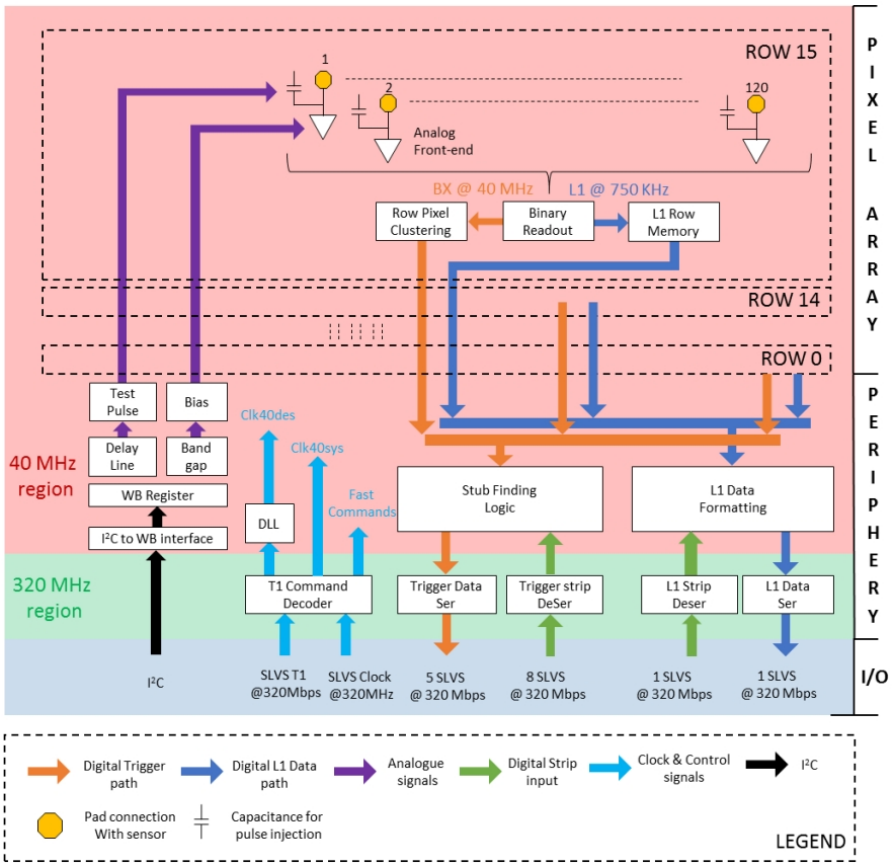


Figure 3.7.: The MPA data paths. Binary data that is acquired in each analog front-end is split into two different data paths. For the stub data (orange arrows) the hits are passed to a row clustering circuit before they will be sent to the stub finding logic in the periphery. If the strip data (green arrows) includes a cluster in the expected correlation window, a stub is generated and sent to the Level-1 track finder at the bunch crossing rate of 40 MHz. At the same time, the data is stored in the Level-1 row memory, waiting for a positive trigger decision (dark blue arrows). As soon as the data is requested, all row memories pass their information to the L1 data formatting circuit which will prepare the data for the final readout through one of the *scalable-low-voltage-signaling* (SLVS) connections [Cer+17].

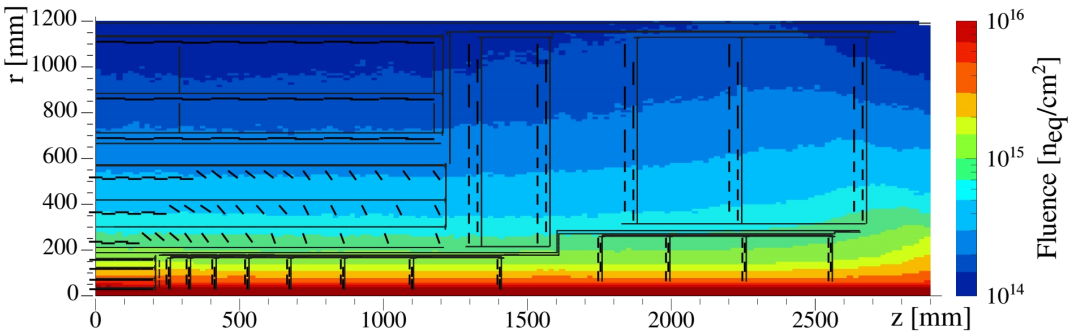


Figure 3.8.: FLUKA simulation of the expected fluence after 3000 fb^{-1} in one quarter of the CMS tracker volume. The highest fluence of about 2×10^{16} n_{eq}/cm^2 is expected in the innermost layer of the pixel detector. The PS and the 2S modules of the Outer Tracker have to withstand 1×10^{15} n_{eq}/cm^2 and 3×10^{14} n_{eq}/cm^2 in their respective innermost position in the outermost disc of the two endcaps [CMS18].

to estimate the expected particle fluence in the detector at the end of its lifetime, FLUKA[2] simulations for different scenarios of the high luminosity phase of the LHC are performed.

Figure 3.8 shows the expected fluence in the CMS tracker after ten years of operation and a total integrated luminosity of 3000 fb^{-1} at a center of mass energy of 14 TeV. The fluence is given in units of n_{eq}/cm^2, which means that the bulk damage in silicon sensors caused by various particles with different energies are normalized to the damage done by 1 MeV neutrons, using the NIEL hypothesis [Mol99]. The plot indicates that the radiation level decreases with increasing distance to the beam line. While the innermost layer of the CMS pixel detector will be exposed to a fluence of almost 2×10^{16} n_{eq}/cm^2 the outermost 2S modules will only be irradiated to a more moderate fluence of 1×10^{14} n_{eq}/cm^2. It is expected that the PS modules in the barrel region have to withstand a maximum fluence of 1×10^{15} n_{eq}/cm^2 and will collect a total ionizing dose (TID) of about 5×10^5 Gy at the end of the runtime of the HL-LHC.

For this reason, the CMS Outer Tracker community is working hard in the last few years to develop radiation hard readout chips and silicon sensors that can still be operated at the end of the HL-LHC runtime. In this context, KIT took a leading role during the sensor development phase by studying various different sensor materials and thicknesses as well as taking part in the sensor design optimization process of the PS-p sensor. Both, early prototypes as well as the current baseline sensors have been developed and investigated. The process and the results are presented in detailed in the following chapters.

[2] **FLU**ktuierende **KA**skade

4

Silicon as particle detector

Since the invention of the transistor in 1947 by Bardeen, Brattain and Shockley [BB48] and especially since the end of the 20th century, when personal computers became affordable for many people around the world, the demand for semiconductor materials is constantly increasing. As a consequence, a whole new semiconductor industry started to grow and reached its all-time highest sales revenue of 412.22 billion US-dollar in 2017 [Wor18]. Silicon as the most widely accessible semiconductor in the world quickly became the most requested semiconducting material with an annual production of over 7000 kt in the last few years [US 18].

Particle physics experiments are taking advantage of this trend. As a result of the technological progress, costs for ever better semiconductor materials are getting more and more affordable for large scale detectors like the Outer Tracker of CMS. The present Outer Tracker already covers an area of over 200 m^2 of active silicon, making it the largest silicon tracking device ever built [Kar+97]. Before the time of high-quality and affordable silicon, experiments relied on gas filled detectors in order to cover bigger volumes for tracking purposes. However, the advantages of silicon over gas filled detectors are manifold: a faster signal generation, increased readout rate and intrinsic energy resolution, to name just a few. The superior energy resolution is due to the fact that only 3.6 eV are required to create an electron–hole pair, whereas approximately 30 eV are necessary to ionize a gas molecule. On average every minimal ionizing particle that crosses the silicon bulk creates about 76 electron–hole pairs per micrometer that form the signal which is amplified and processed by the readout electronics [Har17].

This chapter provides a brief introduction to semiconductor physics and explains how the unique properties of the material are exploited to build particle detection devices. This also requires a short explanation of the energy deposition processes of different particles in silicon and matter in general. Finally, various types of radiation damage and their effects on the sensor performance are explained in detail.

4.1. Band model

In crystalline solids, atoms are arranged in a periodic lattice structure. In this configuration also the electrostatic potential, formed by the atomic nuclei gets periodical. Solving Schrödinger's equation for quasi-free electrons inside this potential leads to multiplets of energy states that are separated by gaps without any quantum mechanical states that are allowed to be occupied by the electrons. Since these states in each multiplet are very dense, they are usually regarded as independent energy *bands* without any forbidden states between them. The highest energetic band whose states are fully occupied by electrons is called the *valence band*. The next empty or partially filled energy band is known as the *conduction band*. Both bands are separated by the band gap E_g, which is different for every solid state material (see e.g. [Dem16]).

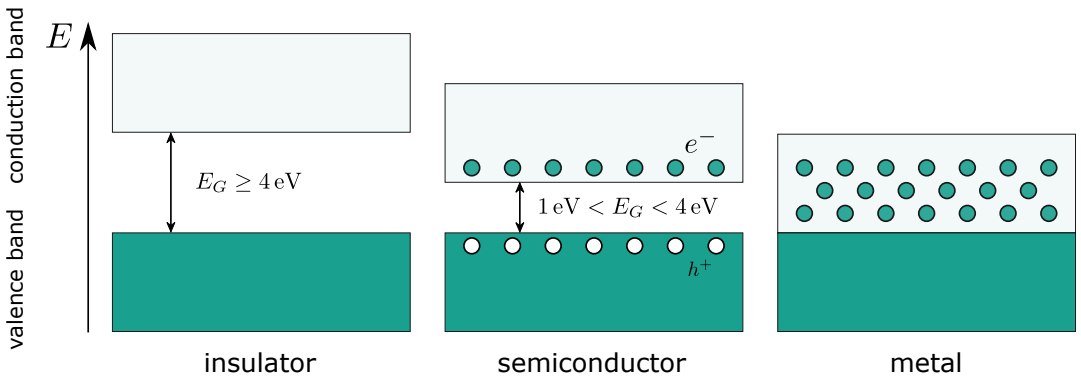


Figure 4.1.: Schematic of the energy band model and the resulting classification of solids into insulators, semiconductors and metals. Solids with a band gap bigger than 4 eV cannot generate free charge carriers by thermal excitation at room temperature and are therefore insulating. Semiconductors are partially conductive at room temperature due to some thermally excited electrons in the conduction band and the corresponding holes in the valence band. Metals, which are defined by a non-existing band gap, are always conductive due to the partially filled conduction band at every temperature. Modified from [Sch15].

The probability of an electron occupying an energy state with a certain energy E is described by the Fermi-Dirac distribution $f(E,T)$ which is valid for fermions and therefore also for electrons and is defined as (see e.g. [Har17])

$$f(E,T) = \frac{1}{\exp\left(\frac{E-\mu}{k_B T}\right) + 1} \tag{4.1}$$

with the chemical potential μ, the Boltzmann constant $k_B = 8.617 \times 10^{-5}\,\mathrm{eV/K}$ and the absolute temperature T of the solid. At $T = 0\,\mathrm{K}$ the chemical potential equals the *Fermi energy* $E_F = \mu(T = 0\,\mathrm{K})$, the highest possible energy that a fermion can have in its ground state. With the knowledge of the band gap and the position of the Fermi energy, solids can be categorized into three different groups of materials: metals, semiconductors and insulators (see figure 4.1).

Metals

If no band gap between the valence and the conduction band exists, the Fermi energy is located inside the conduction band. This means that electrons are able to occupy free states in the conduction band even without thermal excitation and therefore also at absolute zero ($T = 0\,\mathrm{K}$). Solids with such kind of band structure are always conductive and usually called *metals*.

Insulators

In intrinsic solids with a noticeable band gap, the Fermi energy is usually located close to the center between the valence and the conduction band. With a band gap higher than 4 eV [HNF07], electrons can only reach the conduction band at very high temperatures, which means that these materials are usually non-conductive and are therefore called *insulators*.

Semiconductors

A solid that is neither a metal nor an insulator is called a *semiconductor*. With a band gap of $0.1\,\mathrm{eV} < E_g < 4\,\mathrm{eV}$ [HNF07] the barrier is small enough to be overcome by thermal excitation at room temperature (or absorption of a photon), but keeps the solid insulating at low temperatures close to absolute zero. An electron which may be excited into the conduction band as well as the remaining hole in the valence band serve as free charge carriers and therefore improve the overall conductivity of the solid. The probability for an electron to occupy a state in the conduction band by thermal excitation is described by the already introduced Fermi-Dirac distribution (equation 4.1). In silicon about $1 \times 10^{11}\,\mathrm{cm}^{-3}$ of free charge carriers are generated by thermal excitation at room temperature [Spi05]. If the number of charge carriers is dominated by thermal excitation of the electrons and other sources like impurities in the bulk are negligible, the silicon is called *intrinsic*.

4.2. The effects of doping

Intrinsic silicon is hardly used for any kind of active element in silicon devices. Both, the semiconductor industry as well as particle physics experiments rather rely on silicon whose electrical properties are modified in a way that devices such as diodes and transistors can be produced from it. The idea is to introduce other elements into the silicon crystal lattice that either increase or decrease the overall number of free charge carriers of the solid, thus changing its electrical properties. This technical process is called *doping* and is one of the first main steps towards any complex device made out of silicon.

As part of the fourth main group of elements, silicon has four bound valence electrons that connect to four adjoining atoms to create the lattice structure. By introducing atoms with five valence electrons to the lattice, four of their bound electrons are used to create the lattice structure like silicon atoms do, while one excess electron is left that can move almost freely inside the crystal lattice, thus increasing the overall conductivity of the now n-doped silicon substrate. The same applies to silicon that is doped with atoms with only three valence electrons. However, instead of providing an additional electron to the lattice, elements like boron cannot bind four neighboring silicon atoms but will create a hole instead which can be filled by any other valence electron of the solid. In this p-doped silicon, valence electrons of neighboring atoms start to fill these voids, creating new holes at their former position that are filled by other valence electrons again. This process is equivalent to a *hole* that is moving in the opposite direction as the electrons do, which again increases the conductivity of the now p-doped silicon. The number of doping atoms and thus the increased conductivity after any doping process directly translates into a decreased *resistivity* of the material which can be calculated as

$$\rho = \frac{1}{e(\mu N)} \tag{4.2}$$

with the elementary charge e, the doping concentration N and the mobility μ of the introduced charge carriers. The resistivity is the primary parameter that influences the electrical properties of any complex device made from it and has to be chosen carefully to meet the requirements for its field of application.

It is important to mention that in both cases, n- and p-doping, the doping atoms are ionized and thus generate fixed space charge in the crystal lattice. Nevertheless, the amount of fixed space charge and the number of free charge carriers always add up to zero, thus keeping the solid electrically neutral. Both types of doping are illustrated in figure 4.2.

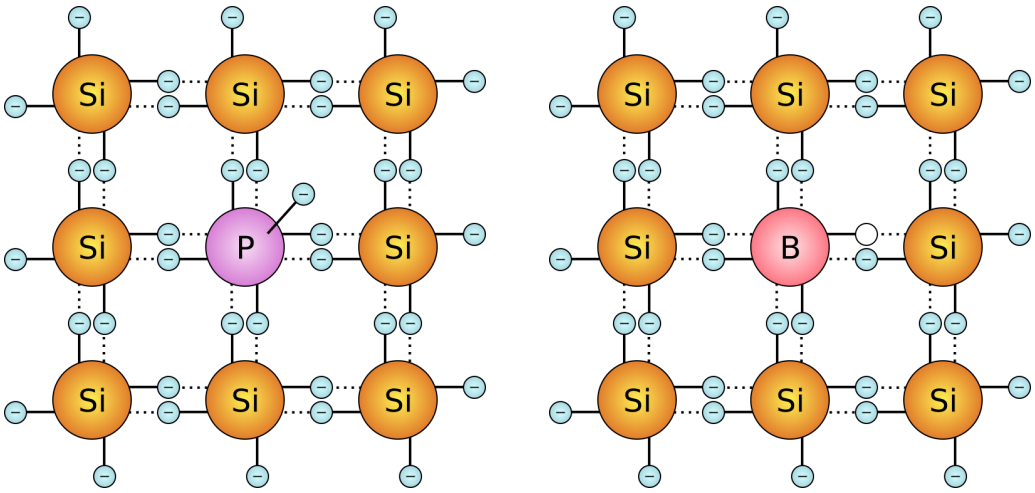


Figure 4.2.: *n*- and *p*-doping with phosphorus and boron in silicon. For *n*-type silicon phosphorus atoms are introduced to the silicon lattice (left picture [Hen06b]). Four out of five bound electrons of phosphorus are used to connect the surrounding silicon atoms, while the excess electron can move freely inside the lattice. In case of *p*-doping, boron atoms are added to the silicon lattice (right picture, adapted from [Hen06a]). Since one bound electron is missing to form the regular silicon lattice, a hole is created that can be filled by another bound electron.

All these effects can be explained by additional energy levels that are added inside the band gap of silicon. In case of *n*-doped silicon, new energy states close to the conduction band are introduced, which allow electrons that are occupying these states to easily reach the conduction band and become free charge carriers. These levels and the corresponding doping atoms with more than four valence electrons are called *donor levels* and *donors*, respectively. Atoms with fewer than four valence electrons on the other hand are called *acceptors*. The corresponding *acceptor levels* are located close to the valence band, offering free energy states that can be filled with electrons from the valence band, creating holes at their former position which act as free charge carriers as well.

4.3. The *pn*-junction

Intrinsic silicon and even a single piece of doped silicon is not suitable to be used as a particle detector. The reason for this is the huge number of thermally excited charge carriers inside the silicon bulk, which exceeds the number of charge carriers generated by incident particles by many orders of magnitude. A charged particle that penetrates a silicon sensor with a typical thickness of 320 µm generates only about 25 000 electron–hole pairs, compared to about 1×10^{11} electrons that are generated by thermal excitation per unit volume cm^{-3} at room temperature. The solution for this problem is to deplete the silicon bulk from as many free charge carriers as possible. This is achieved by creating an interface between *p*- and *n*-type silicon which is called a *pn*-junction. A silicon device that only consists of one of these *pn*-junctions is called a *diode*. As soon as the *n*- and *p*-region are brought into contact, the corresponding *majority charge carriers*, electrons in the *n*-doped and holes in the *p*-doped silicon, start to diffuse into the opposite region and recombine with their counterparts. This means that the excess electrons of the *n*-type silicon start to fill the holes in the *p*-type silicon close to the interface, forming a insulating zone without any mobile charge carriers which is called *space charge region* (SCR) or *depletion region*.

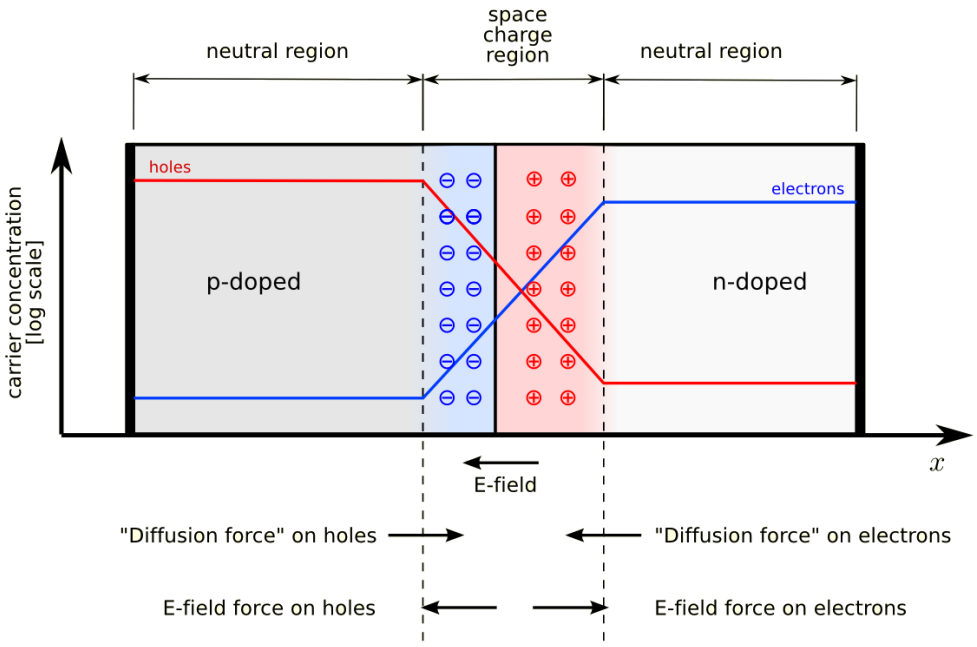


Figure 4.3.: *pn*-junction in equilibrium. The diffusion of majority charge carriers is compensated by an electric field that is generated by the recombination process of electrons and holes in the space charge region (SCR). The forces caused by the diffusion and the electric field are shown below the *pn*-junction. The corresponding electron and hole concentration are marked in red and blue, respectively [The07].

This process is slowed down by an electric field that arises from the remaining ionized nuclei in the SCR which counteracts the diffusion process and enhances the drift of the charge carriers in the opposite direction until both processes compensate each other. At this point equilibrium is reached and the space charge region reached its maximum intrinsic expansion. A schematic of the *pn*-junction, its corresponding carrier concentration and electric field constellation in equilibrium is shown in figure 4.3.

Starting with the Poisson equation for the electrostatic potential ϕ, the width w of the space charge region in equilibrium can be calculated as follows:

$$\frac{d^2\phi}{dx^2} = -\frac{\rho(x)}{\epsilon_0 \epsilon_{\mathrm{Si}}} \tag{4.3}$$

with the vacuum permittivity $\epsilon_0 = 8.854 \times 10^{-12}\,\mathrm{F\,m^{-1}}$ and the relative permittivity of silicon ϵ_{Si}. Assuming a discontinuous step at the junction, the charge density $\rho(x)$ is given as:

$$\rho(x) = \begin{cases} -qN_A & \text{for} \quad -x_p \leq x \leq 0 \\ qN_D & \text{for} \quad 0 < x \leq x_n \end{cases} \tag{4.4}$$

with the donor and acceptor concentration N_A and N_D in the bulk of the respective *p*- and *n*-region of the *pn*-junction. The expansion of the SCR into the two regions is defined as x_p and x_n.

The electrostatic potential in each region is determined by integrating the Poisson equation twice while taking the boundary conditions $E(x_n) = E(-x_p) = 0$ and $\phi(x = 0) = 0$ into account:

$$\phi_p(x) = \phi(x_p) - \frac{qN_A}{2\epsilon_0\epsilon_{\mathrm{Si}}}(x + x_p)^2; \qquad \phi_n(x) = \phi(x_n) + \frac{qN_D}{2\epsilon_0\epsilon_{\mathrm{Si}}}(x - x_n)^2. \tag{4.5}$$

The potential difference of the n- and the p-doped region across the SCR is known as the *built-in* or *diffusion voltage* V_0 and is defined as:

$$V_0 = \phi(x_n) - \phi(x_p) = \frac{qN_D}{2\epsilon_0\epsilon_{\mathrm{Si}}}x_n^2 + \frac{qN_A}{2\epsilon_0\epsilon_{\mathrm{Si}}}x_p^2 \tag{4.6}$$

Since both regions are electrically neutral before the charge carriers start to diffuse, conservation of charge adds an additional boundary condition to the equation

$$N_D x_n = N_A x_p, \tag{4.7}$$

which then leads to the width w of the depletion region:

$$w = x_p + x_n = \sqrt{\frac{2\epsilon_0\epsilon_{\mathrm{Si}}}{q}V_0\frac{1}{|N_{\mathrm{eff}}|}} \tag{4.8}$$

and yields the *effective doping concentration* $|N_{\mathrm{eff}}|$:

$$|N_{\mathrm{eff}}| = \frac{N_A N_D}{N_A + N_D}. \tag{4.9}$$

Assuming that the doping concentration of either the n- or p-region is several orders of magnitude higher than the other one, only the concentration of the lower doped region is of importance and defines the size of the space charge region. However, the expansion of the SCR in equilibrium is usually limited to a very small fraction of the whole device. In order to extend the SCR beyond its built-in size, an additional external bias voltage V_{bias} has to be applied to the *pn*-junction

$$w = \sqrt{\frac{2\epsilon_0\epsilon_{\mathrm{Si}}}{q}(V_0 + V_{\mathrm{bias}})\frac{1}{|N_{\mathrm{eff}}|}}. \tag{4.10}$$

However, only if the applied external bias voltage has the same polarity as the electric field in the SCR, the depletion region is growing. Otherwise the external voltage would counteract the depletion process and the SCR would vanish. The whole device would then become conductive and insensitive for incoming particles. Therefore, the device has to be operated in *reverse bias*, which means that the positive terminal (anode) is connected to the n-implant and the negative terminal (cathode) to the p-implant. The bias voltage V_{bias} at which the lower doped part of the semiconductor is fully covered by the SCR is called *full depletion voltage* V_{dep} [Har17]

$$V_{\mathrm{dep}} = \frac{q}{2\epsilon_0\epsilon_{\mathrm{Si}}}|N_{\mathrm{eff}}|\,d^2 \qquad \text{with} \qquad V_{\mathrm{dep}} \gg V_0. \tag{4.11}$$

At this point the whole device is almost completely free of mobile charge carriers, which solves the problem of having too many thermally excited electrons inside the intrinsic semiconductor.

Increasing the bias voltage beyond the full depletion voltage is known as *overdepletion*, which provides a certain level of safety margin to ensure proper depletion of the silicon device. However, an increased bias voltage is also accompanied by a higher potential difference across and an increased electric field inside the SCR. If the field strength exceeds a value of approximately $3 \times 10^5\,\mathrm{V\,cm^{-1}}$ the insulating SCR becomes conductive, causing the electric field and thus the

SCR to collapse. This *breakdown* of the SCR is a non-destructive and reversible process which depends on the material as well as the geometry of the device. Determining the *breakdown voltage* V_{break} at which the SCR collapses is an important measurement during the qualification of silicon sensors.

4.3.1. Capacitance of the space charge region

According to equation 4.6, the space charge region isolates two electrical potentials from each other and thus resembles a parallel-plate capacitor whose capacitance is given as

$$C_{\text{bulk}} = \epsilon_0 \epsilon_{\text{Si}} \frac{A}{w} \tag{4.12}$$

where A stands for the area and w for the width of the space charge region. Therefore, by determining the capacitance of a fully depleted silicon device, the ratio between the area and the thickness of the SCR can be obtained. By inserting equation 4.10 into the parallel-plate capacitor approach, the ratio between the bulk capacitance C_{bulk} and the area A of the SCR can be expressed as

$$\frac{C_{\text{bulk}}}{A} = \begin{cases} \sqrt{\frac{\epsilon_0 \epsilon_{\text{Si}} |N_{\text{eff}}|}{2(V_0 + V_{\text{bias}})}} & V_{\text{bias}} \leq V_{\text{dep}} \\ \epsilon_0 \epsilon_{\text{Si}} \frac{1}{d} = const. & V_{\text{bias}} > V_{\text{dep}}. \end{cases} \tag{4.13}$$

As long as the device is not fully depleted, $1/\text{C}^2$ grows linearly with the bias voltage until the SCR reaches the backside of the semiconductor and then becomes constant. The kink between the linear growth and the constant value of $1/\text{C}^2$ marks the point of full depletion and thus defines the full depletion voltage V_{dep} of the device.

The simplified model of a parallel-plate capacitor does not apply perfectly to silicon sensors that are used in particle physics experiments. Further information about this topic and the necessary correction terms to the equations above can be found in [Bra00]. Nevertheless, the approximation is good enough to extract the capacitance and the full depletion voltage of a device with acceptable accuracy.

4.3.2. Leakage current

The space charge region can never be completely depleted from mobile charge carriers at room temperature. According to the Fermi-Dirac distribution, given in equation 4.1, new electron–hole pairs are constantly generated in the SCR by thermal excitation. By applying an external bias voltage to the device, a measurable current in the depletion region, called *volume generated current* or *leakage current* is generated. Additional charge carriers that diffuse from non-depleted regions into the SCR are negligible at this point. This means that the leakage current is increasing with the size of the SCR and therefore depends on the square root of the bias voltage V_{bias} (see equation 4.10). The volume generated current density is then given as

$$J_{\text{leak}} \approx -e \frac{n_i}{\tau_g} w = -e \frac{n_i}{\tau_g} \sqrt{\frac{2\epsilon_0 \epsilon_{\text{Si}}}{e\,|N_{\text{eff}}|}(V_0 + V_{\text{bias}})} \tag{4.14}$$

with the intrinsic carrier concentration n_i, the effective doping concentration $|N_{\text{eff}}|$, the carrier generation lifetime τ_g as well as the width w of the SCR [Ros+06]. The vacuum permittivity ϵ_0, the relative permittivity of silicon ϵ_{Si} and the elementary charge e are already given in section 4.3. The leakage current through the SCR depends on the temperature. Again, this can be explained by the Fermi-Dirac distribution, which states that the probability to lift an electron from the valence into conduction band increases with higher temperature. The

temperature dependent volume generated current density is best describe by the Shockley diode equation [Sho49], which states that

$$J_{\text{leak}} \propto T^2 \exp\left(\frac{-E_A(T)}{2k_B T}\right) \tag{4.15}$$

with the activation energy E_A of silicon and the Boltzmann constant k_B. The increasing current is also accompanied by a higher power consumption ($P = U \cdot I$) of the device. The excessive heat that is generated by the higher power consumption has to be cooled by a dedicated cooling system or the surrounding air. If the additional heat exceeds the cooling power of the system the device starts to heat up and the leakage current will increase further. This in turn will increase the power consumption again and the device will end up in a *thermal runaway* of the leakage current [Mol99].

4.4. Interaction between particles and matter

Now that the silicon device is depleted from mobile charge carriers, it became sensitive to the energy deposition of incident particles inside the SCR. The amount of energy that is deposited by the incident particle depends on the type and energy of particle as well as the absorber material. In the following, the energy deposition of heavy charged particles, electrons and photons are introduced.

4.4.1. Charged particles – the Bethe equation

The energy loss of heavy charged particles can be well described by inelastic coulomb interactions between the incident particle and multiple shell electrons of the matter.

The average energy loss of the traversing particle per unit length, also known as *stopping power*, is described by the Bethe equation, see e.g. [Par18]

$$-\left\langle \frac{dE}{dx} \right\rangle = 4\pi N_A r_e^2 m_e c^2 z^2 \frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\left(\frac{2m_e c^2 \beta^2 \gamma^2 T_{\max}}{I^2}\right) - \beta^2 - \frac{\partial(\beta\gamma)}{2}\right]. \tag{4.16}$$

The parameters of the equation are listed below:

N_A	Avogadro constant
r_e	Classical electron radius
m_e	Mass of the electron
c	Speed of light
z	Charge of the incident particle
Z	Atomic number of the traversing material
A	Mass number of the traversing material
β	Ratio of velocity to the speed of light
γ	Lorentz factor
$T_{\max}$	Maximum kinetic energy that can be transferred in a single collision
I	Mean excitation energy

The Bethe equation already contains smaller correction terms that account for effects other than inelastic scattering with the shell electrons. Nevertheless, the Bethe equation, even with the correction terms, is only valid for particles within an energy range of $0.1 \leq \beta\gamma \leq 1000$. For particles with lower energy, nuclear losses become more relevant and start to limit the overall

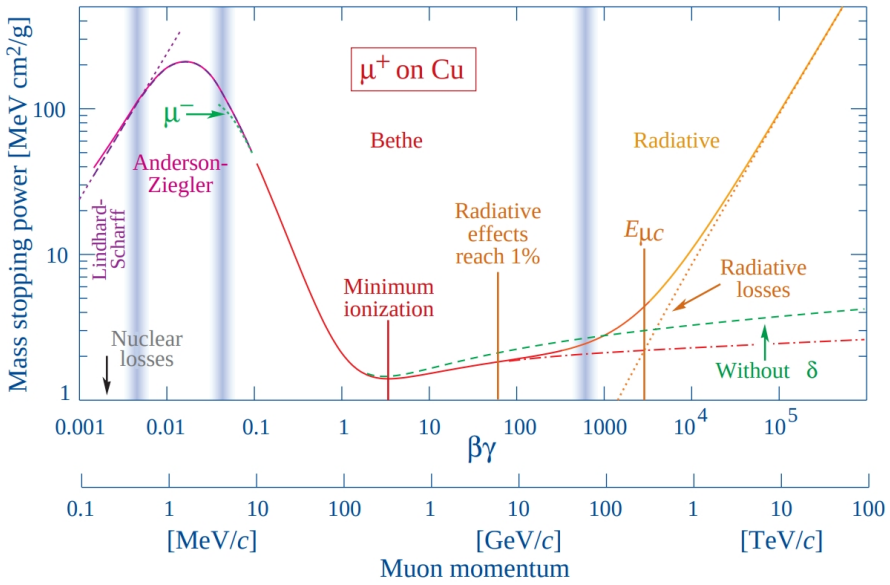


Figure 4.4.: Mass stopping power for positively charged muons over the muon momentum range of $0.1\,\mathrm{MeV/c} \leq p_{\mu^+} \leq 100\,\mathrm{TeV/c}$ in copper. The Bethe equation is only valid for a window at moderately relativistic muon momenta. In that region around $\beta\gamma \approx 3 - 4$ the stopping power gets minimal and the muon is called a minimal ionizing particle (MIP). While at lower energies the stopping power is mainly affected by nuclear losses, at higher energies the energy loss of muons is dominated by radiative losses [Par18].

energy loss that is predicted by the Bethe equation. At higher energies, radiative losses start to set in and dominate the energy loss of the particle. Figure 4.4 shows the stopping power of a positively charge muon μ^+ in copper for all mentioned energy ranges.

Particles with an energy of $\beta\gamma \approx 3 - 4$ are called minimum ionizing particles or MIPs for short. Within that particular range, the stopping power passes a minimum which implies that the particle traverses the matter with the minimal energy loss possible for that specific material. If not stated otherwise, particles that are mentioned in this thesis are usually considered to be minimum ionizing particles.

4.4.2. Electrons

The assumption of a heavy particle interacting with shell electrons is no longer valid if the incident particle is an electron as well. This means that the Bethe equation does not apply for electrons and positrons due to their identical interaction partner. Instead, their energy loss is dominated by elastic scattering (ionization, Møller and Bhabha scattering) at lower and bremsstrahlung at higher energies. Nevertheless, signal generation in silicon is predominantly caused by the ionization processes and an energy transfer in the order of the energy loss of heavy MIP particles. The reason for this is the very thin silicon layer of about 200 µm that corresponds to 0.2 % of the radiation length of silicon [Par18].

4.4.3. Photons

For massless photons three different interaction processes are possible: absorption of the photon by the photoelectric effect, Compton scatting and electron–positron pair production. The

cross-section of each of those processes depends strongly on the photon energy and the atomic number of the absorber material. At lower energies the photoelectric effect is the dominant mechanism. It describes the complete inelastic scattering of the photon by transferring all its energy to one of the shell electrons of the absorber material. At intermediate energies, Compton scattering sets in and starts to contribute to the total cross-section of the photon interaction. During this process, the photon transfers only a fraction of its energy to the electron which in turn leaves the atom and can contribute to further energy losses in the absorber material (see previous section). At energies above the threshold of 1.022 MeV and the proximity of an atomic nucleus for momentum conservation, the photon can be converted into an electron–positron pair. While the resulting electron can lose some of its energy via elastic scattering or bremsstrahlung, the positron will annihilate with a present electron, emitting two 511 keV photons that eventually start to lose some of their energy by one of the mentioned processes again [Par18].

4.5. Signal generation

Most of the energy which is deposited in the material is used to transfer electrons from the valence into the conduction band. About 3.6 eV are necessary to generate such an electron–hole pair, which is considerably larger than the band gap of silicon of 1.12 eV at room temperature. The reason for this behavior is the band structure of silicon. Silicon is an indirect semiconductor which means that the closest transition between the valence and the conduction band requires additional excitation of the silicon lattice to ensure momentum conservation. These excitations are usually regarded as quasiparticles that are referred to as *phonons*. However, the consequent three body process between the photon from the energy transfer, the electron and the phonon is less probable to take place than a two body process in case of a direct transition without lattice excitation. Therefore, the electron is more likely to undergo a direct transition into the conduction band, whose energy threshold is about 3.6 eV, see e.g. [GM12].

When particles are completely absorbed by the detection material, almost all their kinetic energy is converted into electron–hole pairs. In this case, the number of generated charge carriers is well described by a Gaussian distribution. In thin materials on the other hand only a small amount of the initial particle energy is deposited according to the Bethe equation. Statistical fluctuations of the ionization process can lead to an additional energy deposition and the generation of highly energetic secondary electrons. Similar to the primary particle, these knock-on or δ electrons can ionize surrounding silicon atoms and increase the overall yield of charge. This leads to an asymmetric energy loss towards higher energies which is approximately described by a Landau distribution [Lan44]. Figure 4.5 shows several normalized Landau shaped energy loss distributions of 500 MeV pions inside silicon of various different thicknesses.

The thicker the material, the more likely it gets for particles to deposit a large amount of their initial energy due to the statistical fluctuations. As a result, the distribution gets shifted towards higher energy losses per micrometer. In contrast to a Gaussian distribution, the mean and the **M**ost **P**robable **V**alue (MPV) are not the same due to the asymmetry towards higher energies. For a Landau distribution the MPV is about one third lower than its mean value. If not stated otherwise, talking about energy deposition or signal height is usually referred to the MPV and not the mean value of the energy deposition.

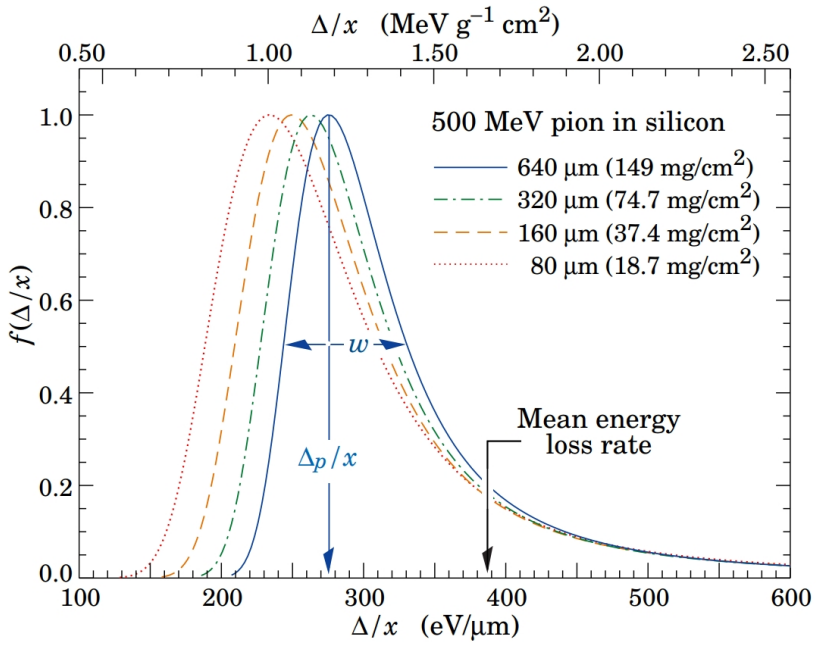


Figure 4.5.: Normalized energy deposition per µm of a 500 MeV muon in silicon with various thicknesses. The energy deposition follows the Landau distribution with an asymmetry tail towards higher energies [Par18].

4.6. Signal detection

As soon as charge is generated in the SCR the charge carriers start to drift inside the electric field that is generated by the external bias voltage until they reach their respective terminal. In case of a reversely biased diode the holes are drifting to the cathode that is connected to the p-doped silicon while the electrons are consequently drifting towards the n-implant which is attached to the anode of the external voltage supply. The charge is then collected and processed by dedicated readout electronics.

4.6.1. Shockley-Ramo Theorem and the Weighting field

The signal formation at the electrodes already starts as the charge carriers start to drift along the electric field lines of the SCR. The reason for this are *signal induced currents* at the electrodes, whose creation process is well described by the Shockley-Ramo theorem [Ram39] [Sho38]. The generated charge in the detector is then determined by integrating the induced current over the drift time of the respective charge (electron or hole). The principle of signal induced current is not limited to semiconductors with a space charge region, but is also valid for any kind of device with a system of electrodes. The theorem states that the induced current at an electrode j is proportional to the charge q and velocity $\vec{v}$ of the moving particle as well as the *weighting field* $\vec{E}_W$ in the device for that particular electrode

$$i_j = -q\,\vec{v}\,\vec{E}_{W_j}\,. \tag{4.17}$$

The weighting field for each electrode $\vec{E}_{W_j}$ solely depends on the geometry of the device and is obtained by applying unit potential to electrode j and ground to all others [Spi05].

In a heavily over-depleted diode with thickness d and two electrodes to which a bias voltage V_{bias} is applied, the system approaches and resembles a parallel plate capacitor with a uniform electric field. Therefore, the electric field and the weighting field simply read

$$E = \frac{V_{\text{bias}}}{d}; \qquad E_W = \frac{1}{d}\,. \tag{4.18}$$

Assuming a constant carrier velocity v

$$v = \mu E; \qquad t_{\text{drift}} = \frac{d}{v} \tag{4.19}$$

the Shockley-Ramo theorem (equation 4.17) yields the total amount of charge induced in the electrode

$$Q = i\, t_{\text{drift}} = -q\mu \frac{V_{\text{bias}}}{d^2} \frac{d^2}{\mu V_{\text{bias}}} = -q\,. \tag{4.20}$$

Since electrons and holes are moving in opposite directions it is important to point out that both induce current of the same polarity at a given electrode [Spi05]. However, the sum of both currents at one electrode still adds up to q, which complies with the simple picture of collected charge at the terminal. The calculation also reveals that if the integration time of the readout electronics does not exceed the drift time of the charge carriers, only a small fraction of the generated signal is read out which could impair the performance of the detector.

For devices without any space charge, like the parallel plate capacitor example shown above, the electric field and the weighting field are always of the same shape. More complex devices like strip and pixel detectors show significant differences between the two fields which have to be taken into account during the calculation of the signal induced current at the electrodes. More information about the Shockley-Ramo theorem and the weighting field can be found in [Har17].

4.7. Position sensitive silicon sensors

A depleted diode is already sensitive to incoming particles and can be seen as the most simple silicon particle detector. However, the position information a diode can provide is limited to the size of the diode itself. In order to gain additional information about the impact point of the particle, the sensor has to be segmented into multiple smaller *pn*-junctions. In case of a one dimensional segmentation, the diode becomes a *strip sensor*, the most widely used type of silicon sensor in large scale particle physics experiments like CMS or ATLAS. Its main advantage is the comparatively simple connection to an adjoining readout chip. The connection is usually realized by thin aluminum wires, called *wire bonds*, that connect one end of each strip to one channel of the amplification stage of the readout electronics. The situation gets more complicated if the silicon sensor is segmented in two dimensions which leads to small isolated islands, called *pixels*. In that case, the front-end electronics cannot be easily attached to each individual pixel by wire bonds anymore. Instead, the readout chip is placed on top of the sensor, which is called *flip-chip bonding*. Small solder balls between the sensor and the readout chip ensure a conductive connection between the pixel cells of the sensors and the pixelated front-end electronics. A precise alignment and the fact that the chip still has to be wire bonded to a peripheral circuit, makes this *hybrid technology* comparably complicated and expensive. It should be mentioned that *monolithic* approaches with combined sensor and readout electronics exist [Mou+18] which, however, will not be discussed in the context of this thesis. Nevertheless, the advantage of the hybrid technology lies in the independent development of the pixel sensor

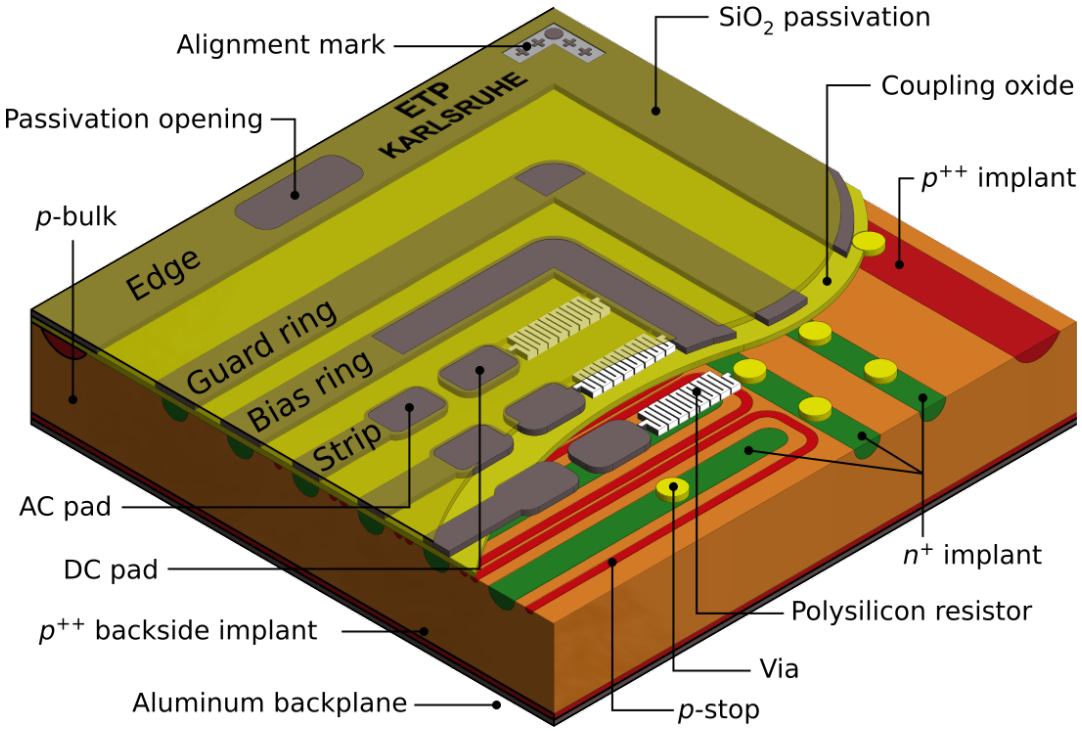


Figure 4.6.: Illustration of an n-in-p type strip sensor. n-doped and p-doped silicon are marked green and red, respectively. Each strip implant is isolated by a *p-stop* ring and is read out capacitively via its aluminum strip that runs on top of the silicon dioxide. All strips are enclosed by and connected to the grounded *bias ring* through *vias* and *poly resistors*. The surrounding and floating *guard ring* protects the bias ring and the connected strips against excessive potential differences between ground and high voltage at the *edge*. Modified from [Har17].

and the readout chip. In this way, both parts can be optimized to their respective requirements and be produced in the best suited technology.

4.7.1. A silicon strip sensor

A silicon sensor does not only consist of a certain number of pn-junctions, but also includes peripheral structures, different strip or pixel isolation techniques and several passivation layers to ensure testing possibilities and stable operation during the production and measurement phase. Figure 4.6 shows a detailed schematic of one corner of an AC coupled strip sensor that includes all relevant structures of a modern silicon sensor.

The base material is a p- or n-doped silicon bulk with a highly doped[1] backside of the same doping polarity. The latter is necessary to ensure an ohmic contact to the backside metallization. Since all silicon sensors for the future CMS Tracker are based on the n-in-p technology[2] [CMS18], only p-bulk silicon with a p^{++} backside implant will be explained in the following. The highly doped n^+ strip implants are located on the frontside of the sensor and establish the actual pn-junctions between each implant and the bulk. The strips and all other necessary implants are covered by a thin SiO_2 layer that acts as isolation between the implants and a conductive metal layer on top of it. The desired AC readout is realized by placing

[1] Highly/Low doped silicon is marked by additional +/- signs next to the letter of the doping type. The more signs are added, the higher/lower the doping concentration compared to the base material

[2] **n** doped implants **in** a **p**-doped bulk

aluminum strips above each strip implant on top of the oxide layer. Multiple bigger areas, called *AC pads* at one or both ends of these aluminum strips facilitate the placement of wire bonds for the connection between the strip and the readout electronics. The AC readout has the advantage that the leakage current is not drained by the readout chip and only the signal is processed by the analog front-end of the chip. However, in order to deplete the bulk, hence expand the SCR to the backside of the sensor, a bias voltage between the bulk and the strip implants has to be applied. The backside of the sensor is completely covered by a metal layer that already acts as one of the terminals for the bias voltage. In case of the strips, additional peripheral structures are necessary to connect the buried n^+-implants to the bias potential. For strip sensors, meander-shaped polysilicon resistors are commonly used that run on top of the silicon dioxide and connect each strip with an all surrounding *bias ring*, which acts as second terminal for the bias voltage. In order to contact the strip implants below the oxide, holes are etched into the insulation layer that are subsequently filled with aluminum to form the conductive connection (also called *via*). Applying negative high voltage on the backside and ground on the bias ring leads to the depletion of the sensor. In this configuration, holes are drifting towards the backside contact while electrons are collected by the strip implants.

The existing potential gradient also leads to the removal of highly mobile electrons in the silicon dioxide resulting in a slightly polarized oxide layers. This additional potential attracts electrons, which accumulate at the Si–SiO_2 interface and generate a conductive channel between the strips. That situation would lead to short circuits between the channels and would impair the position resolution of the penetrating particles. To avoid these short circuits, additional p^+-implants are added between the strips that ensure a proper strip isolation. Depending on the concentration and the implementation technique, this strip isolation is either called *p-stop* or *p-spray*. With p-spray isolation, the entire frontside of the wafer is implanted with a comparatively low-doped p-type silicon layer, which covers the entire space between the strips and therefore isolate them. In either case, electrons are captured by the additional acceptor levels of the p-type silicon and thus generate a small negative space charge at the boron implant. Electrons are repelled by this negative space charge, causing the accumulation layer to be interrupted and the strips to be isolated from each other, see e.g. [Pri16].

All the strips, together with their p-stop isolation, are surrounded by the bias ring, one or multiple guard rings and a sensor edge. The sensor edge is based on a p^{++}-implant that establishes a conductive p^{++}–p–p^{++} sandwich between the frontside edge, the bulk and the backside contact and thereby sets the edge on the same potential as the backside. The all-surrounding edge metal on top of the oxide is used to display several labels, strip numbers and alignment marks. The peripheral bias and guard rings consist of ring-shaped aluminum contacts on top and a DC connected n+-implant below the oxide layer. Both are necessary to protect the strips in the center of the sensor from the high voltage on the sensor edge. While the bias ring is connected to ground potential and thus effectively shields the strips from any current originating from the edge, the guard ring is not connected to any potential (*floating*) which helps to form a more continuous potential drop between the edge and the bias ring and thereby reduce the risk of an early breakdown of the sensor.

The whole sensor is covered by another silicon dioxide layer that serves as passivation layer to protect the sensor from external damage while handling it. Openings at the pads and several positions along the bias and guard ring as well as the edge ensure that the strips and the periphery can still be contacted during testing and operation.

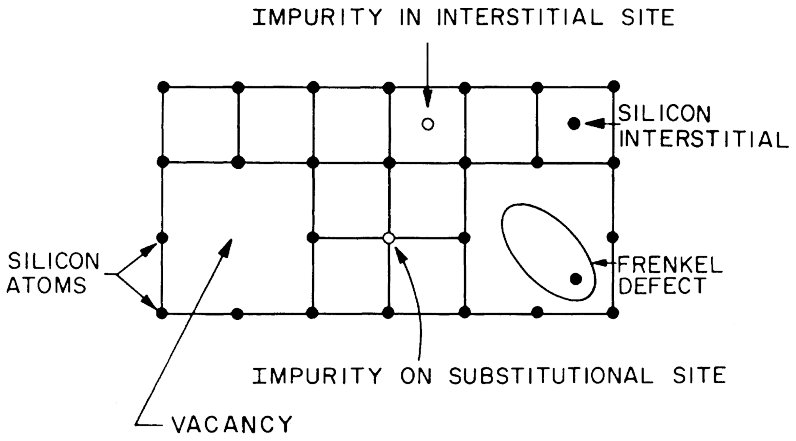


Figure 4.7.: Possible bulk defects in a crystal lattice. Atoms can be knocked out of their lattice sites and thus create *vacancies* at their former positions. The released atom can then occupy one of the surrounding *interstitial* sites an create a double defect called *Frenkel pair* [Lut07].

4.8. Radiation damage

Silicon that is used in an environment like the Inner or Outer Tracker of the CMS experiment is constantly exposed to radiation of particles that emerge from the proton collisions at the interaction point. While these particles traverse the silicon detector, they deposit energy according to the processes introduced in section 4.4. Additional non-ionizing energy losses of these particles can cause severe damage of the silicon lattice and permanent deterioration of the sensor performance, also called *radiation damage*. Depending on the location where the lattice is distorted, radiation damage can be divided into *bulk* and *surface damage*. Bulk damage is responsible for an increased leakage current, lower charge collection efficiency and higher depletion voltage of the sensor. Surface damage, on the other hand, can influence the electric field distribution, strip isolation and causes undesired surface currents, all of which could lead to a reduced breakdown voltage and could impair the sensor performance in general.

4.8.1. Bulk damage

Traversing particles do not solely interact with shell electrons but also with the nuclei of the atoms via elastic scattering. If the energy transfer to one of the nuclei exceeds 25 eV it is able to leave the silicon lattice, creating a *vacancy* at that position. The released nucleus, also called *primary knock-on atom* (PKA) then might occupy one of the nearby *interstitial* sites of the lattice which would lead to a double defect called a *Frenkel pair* [Lin+80]. An overview of the different bulk defects is shown figure 4.7.

The PKA can also traverse the lattice and start to affect other atoms on its path. As it passes other lattice atoms it will ionize them and eventually displace the nucleus, hence generating additional defects along its track. As soon as the PKA lost almost all its energy, it will deposit its remaining energy by creating a defect cluster at the end of its track [Mol99].

NIEL hypothesis

It is easy to understand that damage caused by light particles such as electrons differs from damage caused by heavy hadrons like neutrons and protons of the same energy. But the same also applies for charged and neutral particles. While protons for instance interact with the whole atom primarily by the Coulomb interaction, neutrons can only interact with the nucleus

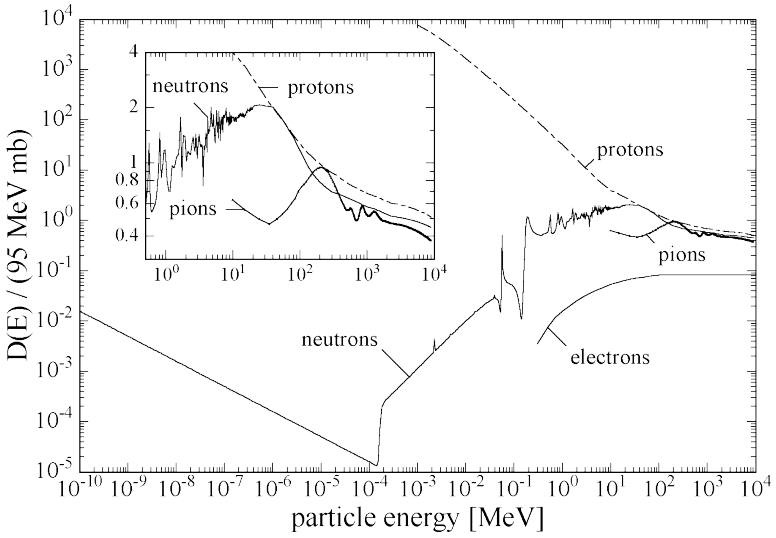


Figure 4.8.: Displacement damage functions D(E) normalized to 95 MeV mb for neutrons, protons, pions and electrons over an energy range of 10^{-10} MeV to 10^{4} MeV [Mol99].

of a lattice atom. Hence, neutrons do not lose as much of their initial energy as protons do. In order to compare radiation damage induced by different particles with different energies the *Non Ionizing Energy Loss hypothesis* (NIEL) is postulated. The NIEL hypothesis assumes that any displacement-damage induced change in the material scales linearly with the transferred energy during the collisions [Mol99]. Figure 4.8 shows the resulting displacement damage function normalized to 95 MeV mb for several particles as a function of their energy.

While there is a big difference between the displacement damage functions of protons and neutrons at energies smaller than a few MeV, both start to converge at energies above 100 MeV and also merge with the damage function of pions.

By introducing a hardness factor κ for the integrated displacement damage function over the energy spectrum of the radiation source the *equivalent* 1 MeV *neutron fluence* Φ_{eq} normalized to the damage induced by 1 MeV neutrons of the same fluence, can be expressed as [Mol99]

$$\Phi_{eq} = \kappa\,\Phi = \kappa \int \Phi(E)\,dE\,. \tag{4.21}$$

All fluences Φ_{eq} that are mentioned in this thesis are given in 1 MeV neutron equivalent per square centimeter ($\mathrm{n_{eq}/cm^2}$).

Effects of bulk damage

All bulk defects described in section 4.8.1 have a major impact on various sensor parameters and impair the performance of the detector during operation. The origin for these effects are additional energy levels inside the band gap that are introduced by the radiation damage. Depending on their position in the band gap, these energy levels can be categorized into three different groups which can be linked to different effects in the silicon sensor.

- Energy levels close to the valence and the conduction band are called *shallow levels*. They are ionized at room temperature and quite similar to energy levels introduced by doping atoms. As a consequence, the effective doping concentration N_{eff} is changing with increasing radiation fluence and therefore affects the depletion voltage V_{dep} of the device. The ratio between additional acceptors and donors, thus increase or decrease of N_{eff}, depends on the particle type and its energy. Former studies showed that usually

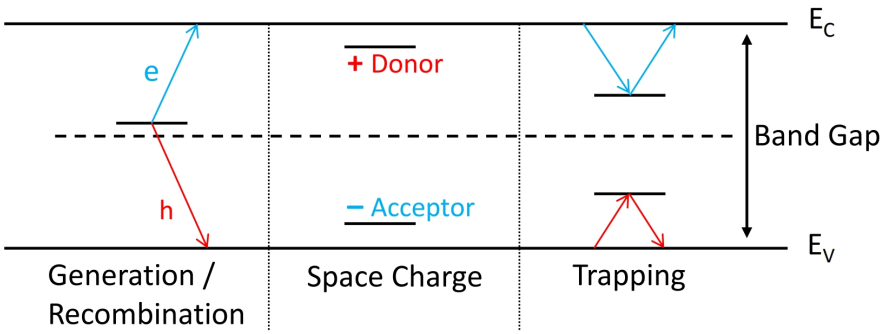


Figure 4.9.: Effects of bulk damage in silicon. Defects in the middle of the band gap serve as generation and recombination center for free charge carriers, increasing the overall leakage current of the sensor (left). Shallow levels close to the valence and conduction band trap charge and mainly affect the effective doping concentration $|N_{\text{eff}}|$ of the solid (middle). Charge can also be trapped by any defect for a certain period of time and is therefore lost for the signal readout (right) [Ebe13].

more acceptor like defects are generated than donator like ones [Jun11]. This means that in case of n-in-p type material the depletion voltage increases with the runtime of the detector.

- Defects that introduce *deep levels* in the middle of the band gap are responsible for an increased leakage current of the sensor. The almost equidistant position between valence and conduction band turn them into generation and recombination centers for electrons and holes at the same time. Hence, electrons can either jump from the valence band into the deep level and from there either reach the conduction band or recombine with a present hole. The higher the fluence the more deep levels are generated and thus more leakage current is generated in the sensor. It was found that the increase of leakage current ΔI per unit volume V after a certain absorbed fluence Φ_{eq} increases linearly with the fluence

$$\frac{\Delta I}{V} = \alpha \, \Phi_{eq}. \tag{4.22}$$

  The slope α is called *current related damage rate* [Mol99].

- Bulk defects can capture drifting charge carriers that are generated by traversing particles. This *trapped* charge then either recombines with its respective counterpart or the defect releases it after a certain period of time. Since the integration time of the readout electronics is usually many orders of magnitude smaller then the detrapping time of the charge, these charge carriers cannot contribute to the signal generation of that particular readout cycle. Thus, both phenomena, recombination and the time-delayed release of the charge carriers, lead to an undesirable signal loss that reduces the charge collection efficiency (CCE) of the sensor.

A summary of these effects is shown in figure 4.9.

To address these problems, experiments need to provide powerful service equipment that keep the sensors operational throughout their entire lifetime. In case of the future Outer Tracker of CMS, high-performance power supplies, capable of providing up to 800 V, are in place in order to adapt the bias voltage to the depletion voltage of the sensor. By replacing the current

water cooling of the Outer Tracker with a powerful CO_2 cooling system, the leakage current of the sensor will be kept as low as possible (see equation 4.15, thus ensuring that excessive heat, caused by the increasing power consumption ($P = U \cdot I$) of the sensor, is dissipated and that the sensor is not driven into thermal runaway. Finally, custom made low-noise readout electronics ensure a high signal to noise ratio (SNR) and thus a distinct separation of the signal from the background noise [CMS18].

4.8.2. Surface damage

Radiation damage is not limited to defects in the silicon bulk. Also the surface and the silicon dioxide in particular are affected by the absorbed radiation dose and have a large influence on the performance of the device. Surface damage, however, is not only caused by radiation damage, but is already introduced during the production process of the sensor. Dangling bonds at the Si-SiO_2 interface, caused by the different lattice structure of silicon and silicon dioxide, lead to additional energy levels in the middle of the band gap. These *interface traps* predominantly contribute to the surface generation current and are already present after production. The different lattice structures also leads to a thin layer of highly disordered atoms in the silicon dioxide which act as hole trapping defects at the interface. Charge that gets trapped by these defects is known as *fixed oxide charge*.

During operation, traversing particles and the resulting electron–hole pairs in the oxide contribute to the surface damage as well. While the highly mobile electrons are attracted and collected by the strip electrode on top of the oxide, the holes start to drift in the opposite direction and get trapped at the Si-SiO_2 interface, which is known as *oxide trapped charge* [Har17]. All this leads to a positively charged oxide layer that acts as an additional potential which attracts electrons in the bulk. As soon as the electrons reach the Si-SiO_2 interface, they start to accumulate and form a conductive channel between the implants. Therefore, further precautions have to be taken in order to protect the implants from short circuits as described in section 4.7.1.

4.8.3. Annealing

Defects in silicon sensors are not permanent and can evolve over time. With increasing temperature, displaced atoms are able to leave their current position and start to move through the crystal lattice. By doing so, defects can either be cured or enhanced as they start to build clusters with other point defects in the lattice. Both phenomena are called *annealing* and have a strong influence on the sensor properties.

One positive effect of annealing is the decrease of leakage current I_{leak} and thus the current related damage rate α. The higher the temperature and the longer the sensor is stored or operated at this temperature, the stronger the effect. The time and temperature dependence of α is shown in figure 4.10. Since the current is always decreasing over time this kind of annealing is usually referred to as *beneficial annealing*. The parameterization of α over time for different temperatures also allows the conversion of any combination of time and temperature into another. This is used to define a common reference point which is expressed in the effective annealing of the leakage current at room temperature (T = 21 °C).

The fact that annealing can repair and enhance bulk defects in the sensor implies that the effective doping concentration $|N_{\text{eff}}|$ is affected by annealing, as well. In contrast to the annealing of the leakage current, $|N_{\text{eff}}|$ is not only affected by beneficial annealing but also by the detrimental *reverse annealing* which can be parameterized by the *Hamburg Model* [Mol99], illustrated in figure 4.11.

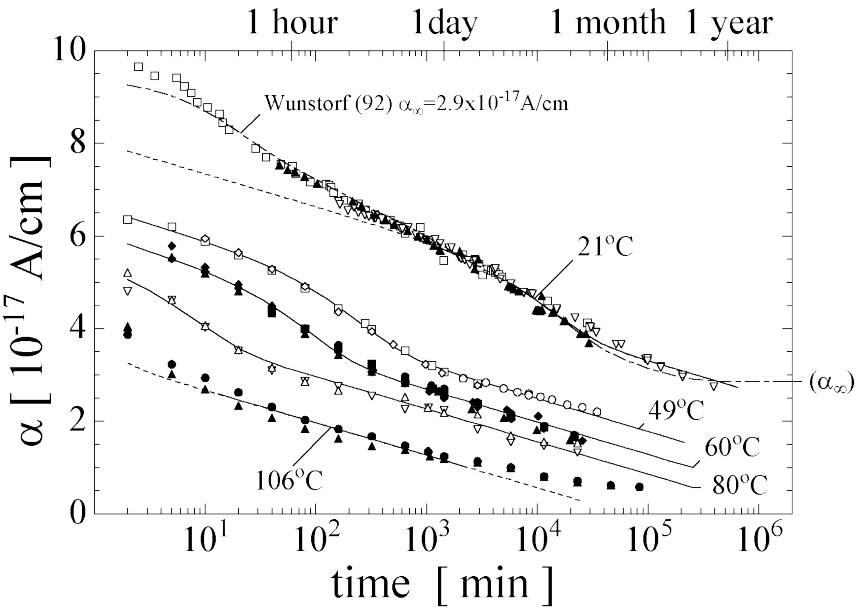


Figure 4.10.: Annealing of the current related damage rate α over time at different temperatures. α decreases continuously over time at every temperature shown in the plot. The higher the temperature, the lower α in general [Mol99].

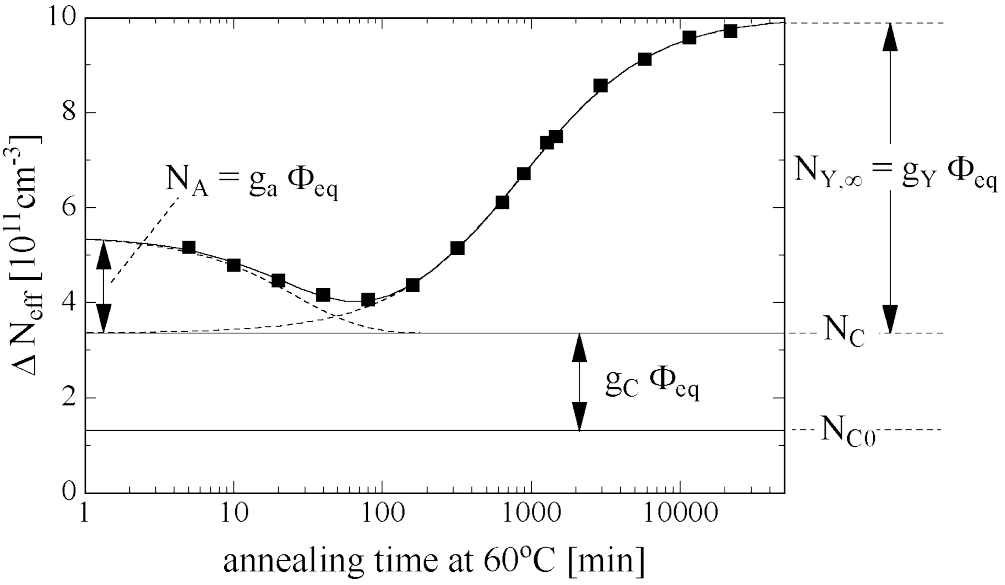


Figure 4.11.: Annealing of the effective doping concentration N_{eff}. First, the irradiation induced change in the effective doping concentration ΔN_{eff} is reduced due to the short term beneficial annealing. After 60 to 70 minutes at 60 °C, which corresponds to about 10 days at room temperature, ΔN_{eff} starts to increases again and even surpasses the initial value before annealing (reverse annealing). The constant offset remains unaffected by the annealing [Mol99].

The evolution of irradiation induced change in the effective doping concentration before and after irradiation ΔN_{eff} consists of three components: the short term or beneficial annealing, the long term or reverse annealing and a constant change. In the initial phase after the defects are created, many of the bulk defects recombine and ΔN_{eff} is reduced. As a result, the full depletion voltage decreases and the charge collection efficiency at a given bias voltage increases. At some point around 10 days at room temperature, the long term annealing takes over and dominates the annealing behavior of the device. Any additional annealing from now on leads to an increase of the effective doping concentration and thus higher depletion voltages. The constant term remains unaffected by annealing and defines the minimum irradiation induced change in the effective doping concentration ΔN_{eff}. The annealing process can be suppressed by storing and operating the sensors at low temperatures around $-20\,^{\circ}\text{C}$ and below, which reduces the movement of the defects and thus the annealing to a minimum.

Part II.

The PS-p light

5

Requirements, design and characterization of the PS-p light prototype

The main objective of this thesis is the development of the macro-pixel sensor of the PS modules for the future Outer Tracker of CMS: the PS-p. All information presented in the previous section is taken into account to make this sensor as radiation hard as possible. However, there are still many free parameters that have to be optimized and adjusted either by simulations or experimental studies. Some of these sensor parameters have already been investigated by several institutes and collaborations in the past. In order to avoid any unexpected problems in advance, it is not very surprising that all these results have been consulted during the development of the pixelated sensor of the PS module.The Institute for Experimental Particle Physics (ETP) played a leading role in providing several wafer layouts and performing detailed qualification studies of non-irradiated as well as irradiated macro-pixel sensor prototypes. The first of these macro-pixel prototypes is the PS-p light whose development process and measurement results are presented in the following.

5.1. Choosing the right sensor material

One of the first decisions that has to be taken during the sensor development is the choice of the right base material. Depending on the requirements, bulk materials with different doping flavors, concentrations and thicknesses are considered. In case of the experiments at the LHC, including CMS, the main driving aspect is the radiation hardness of the material. In order to find a material suitable for use at the HL-LHC, CERN founded a research and development group, the RD50 Collaboration "Radiation hard semiconductor devices for high luminosity colliders" [CER18e], to exchange experience between the various experiments and support their joint effort. Since 2002, the collaboration has been successfully coordinating the development of new radiation hard silicon detectors for the individual experiments. This includes detailed studies of n-in-p instead of the more common p-in-n technology during that time and the accurate characterization of radiation induced damage of the silicon lattice. For more details about the history and the future plans of RD50 see [CM18].

Inspired by the work of RD50 and the promising results, the CMS Outer Tracker collaboration conducted a large-scale sensor development campaign to find the best material for the Phase-II Upgrade of its silicon tracking system. In this context, a 6-inch silicon wafer was designed that contains several strip and pixel sensors of different geometries as well as a variety of test structures to collect as much information about the underlying material as possible. The wafers for this project have been produced and delivered by Hamamatsu Photonics K.K. (HPK) in Japan. This is the reason why this research project is usually referred to as the *Hamamatsu* or *HPK campaign* [Hof13]. All structures on these wafers are based on the single-sided[1] n-in-p or p-in-n technology, implemented on wafers that have been sliced out of a silicon ingot either grown with the Magnetic Czochralski (MCz) [Czo18] or Float Zone (FZ) [Pfa58] process. In

[1] In contrast to the double-sided process, only one side of the wafer contains any microstructures.

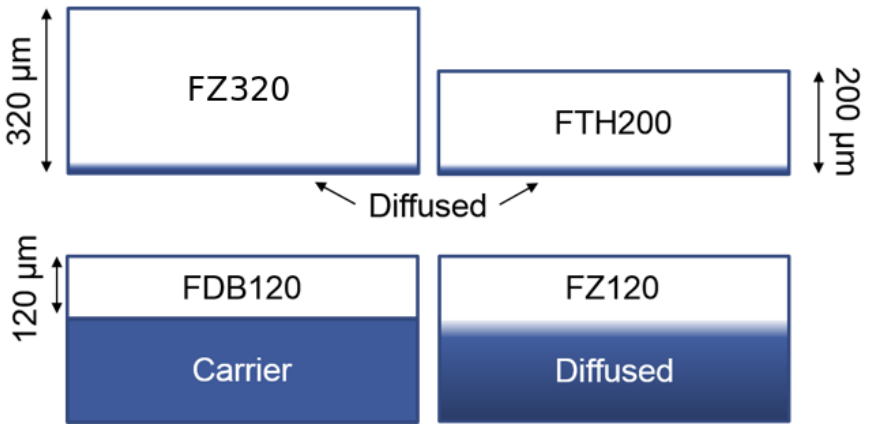


Figure 5.1.: Schematics of silicon substrates of various physical and active thickness. The base material is a 320 µm thick silicon wafer with a thin backside implant. To reduce the the active thickness, the wafer can either be thinned down (TH) directly or after it is bonded onto a carrier wafer. A third option is a deep diffused backside implant which is offered exclusively by Hamamatsu Photonics K.K.

addition, either p-stop or p-spray isolation has been added to the n-in-p wafers to properly isolate the pixels and the strips. Finally, various active thicknesses between 320 and 50 µm were chosen, which have been achieved either by epitaxial growth (Epi), physical thinning (TH) of the wafer, deep diffusion (DD) of the backside implantation or direct bonding (DB) of the thinned wafer onto a support wafer. The different processes except the epitaxial growth are summarized in figure 5.1.

If not stated otherwise, the measurements and results presented in this work are limited to Float Zone material whose active thickness, if changed at all, has been reduced by the deep diffusion process or has been thinned physically.

5.1.1. n-type vs p-type bulk

In the context of the Hamamatsu campaign a total number of 144 wafers have been produced and distributed among the institutes of the CMS tracker community. After meticulous testing and the electrical characterization of the sensors, some of them have been irradiated to various fluences up to about $1 \times 10^{16}\,\mathrm{n_{eq}/cm^2}$, which is close to the expected fluence in the innermost layer of the future CMS pixel detector after 10 years of operation at the HL-LHC [CMS18]. The suitability of the material is determined by repeating the same measurements as before [Hof13] and comparing it with the requirements that are set by the Outer Tracker community. One of the most significant parameters is the charge collection efficiency (CCE) of a sensor. It is defined as the fraction of the collected charge to the amount of charge that is generated by a penetrating particle. Radioactive sources with an activity in the order of MBq or higher, which emit particles with energies in the order of MeV are well suited for that kind of laboratory measurement. In segmented sensors, the generated charge is usually divided among several adjacent channels, resulting in a signal *cluster*. The highest signal on one channel within each of these clusters is called the *seed signal*. A summary of the measured seed signal in irradiated 300 µm thick n-in-p and p-in-n strip sensors is shown in figure 5.2.

All measurements were performed at −20 °C in order to minimize leakage current and prevent the sensor from thermal runaway (see Section 4.3.2). The bias voltage was set to 600 V which corresponds to the target operating voltage of the sensors after 10 years of operation. The type of particle the sensors have been irradiated with is indicated next to the data points, where n

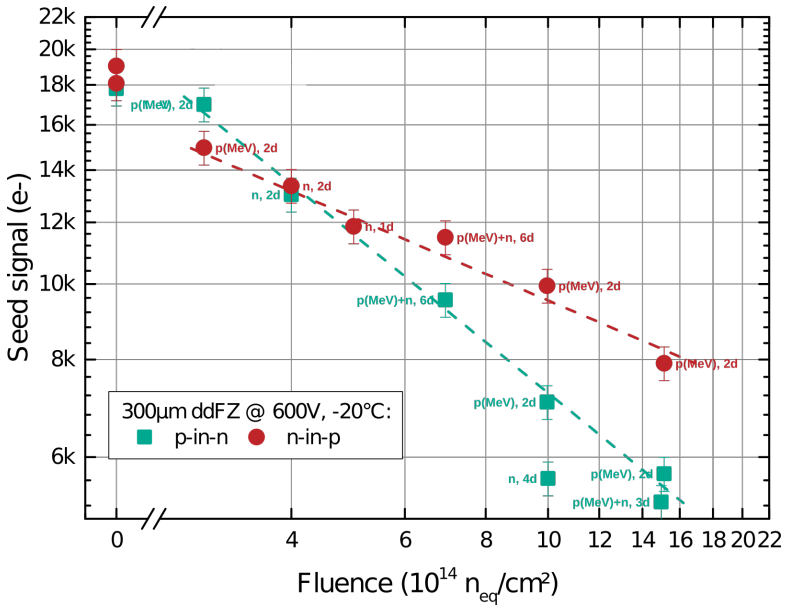


Figure 5.2.: Seed signal of n-in-p (red) and p-in-n (green) substrates over the fluence. The sensors have either been irradiated with 23 MeV protons (p(MeV)), reactor neutrons (n) or both (p(MeV)+n). The annealing time is given in days at room temperature (d). Dashed lines are added to guide the eye. After a fluence of approximately $\Phi_{eq} = 5 \times 10^{14}\,n_{eq}/cm^2$, the p-type material outperforms its counterpart in terms of charge collection and stays in advantage from then on (modified from [Ada+17]).

stands for neutron and p for proton irradiation. Mixed irradiation, like p+n were performed as well. The annealing time of each sensor is given in days (d) at room temperature and is mentioned at the end of each measurement point. The results show that the seed signal in p-in-n material is higher at lower fluences, while p-type substrates show better results at higher fluences of $7 \times 10^{14}\,n_{eq}/cm^2$ and above. The fact that the expected fluence in the innermost layer of the Outer Tracker is in the order of $1 \times 10^{15}\,n_{eq}/cm^2$ and even reaches $2 \times 10^{16}\,n_{eq}/cm^2$ in the pixel detector makes the choice in favor of the p-type substrate inevitable.

5.1.2. Thickness of the sensor

Not only the sensor material, but also its thickness has a big impact on the sensor and detector performance. Thin substrates have the advantage of a lower material budget and thus less energy deposition and multiple scattering of heavy particles, which leads to an increased momentum resolution of the tracking detector. In addition, photons are less likely to be converted into electron–positron pairs, which facilitates their identification during reconstruction. Smaller active volumes also lead to lower leakage currents and thus lower heat dissipation in the powered sensor (see section 4.3.2). However, since approximately 110 electron–hole pairs are created per micrometer of silicon [Har17], smaller signals are generated in thin sensors compared to thicker ones. While this applies for non-irradiated sensors, the situation changes after irradiation of the sensors, which is shown in figure 5.3.

The plot shows the seed signal of various irradiated p-type strip sensors with an active thickness of 200 µm, 240 µm and 300 µm at increasing bias voltages. Looking at the target operating voltage of 600 V, it becomes apparent that substrates with a thickness below 300 µm generate higher seed signals than the thick substrate. This is caused by the fact that thicker

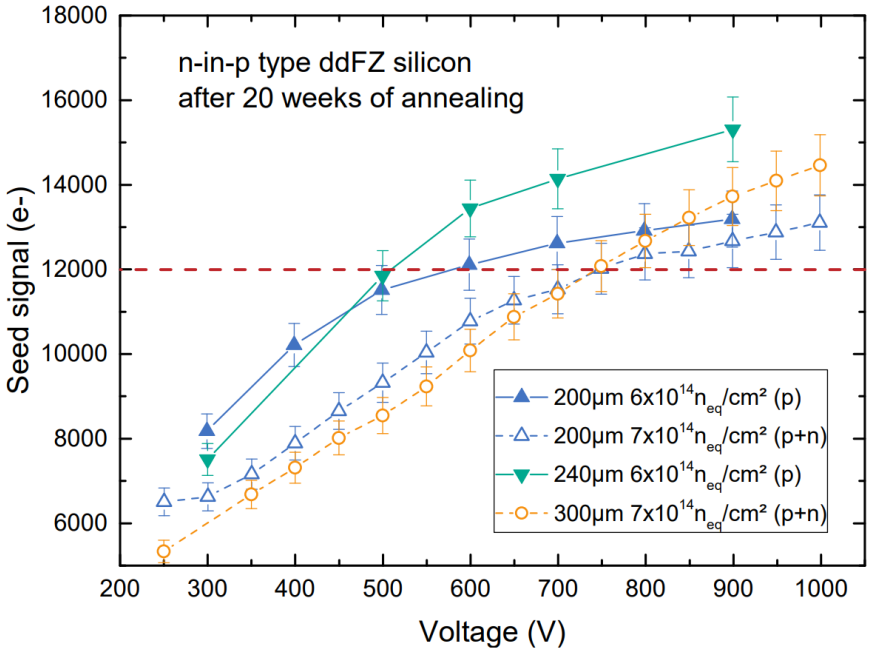


Figure 5.3.: Seed signal after 20 weeks of annealing over the bias voltage of irradiated strip sensors of various thicknesses. The red line indicates the minimal seed signal for sensors read out by the CBC. While generally less charge is generated in thin materials around 200 µm, thick sensors with an active thickness of 300 µm typically suffer from a partially depleted bulk at voltages around the target value of 600 V. Sensors with an active thickness of 240 µm seem to be well-balanced between these two effects [CMS18].

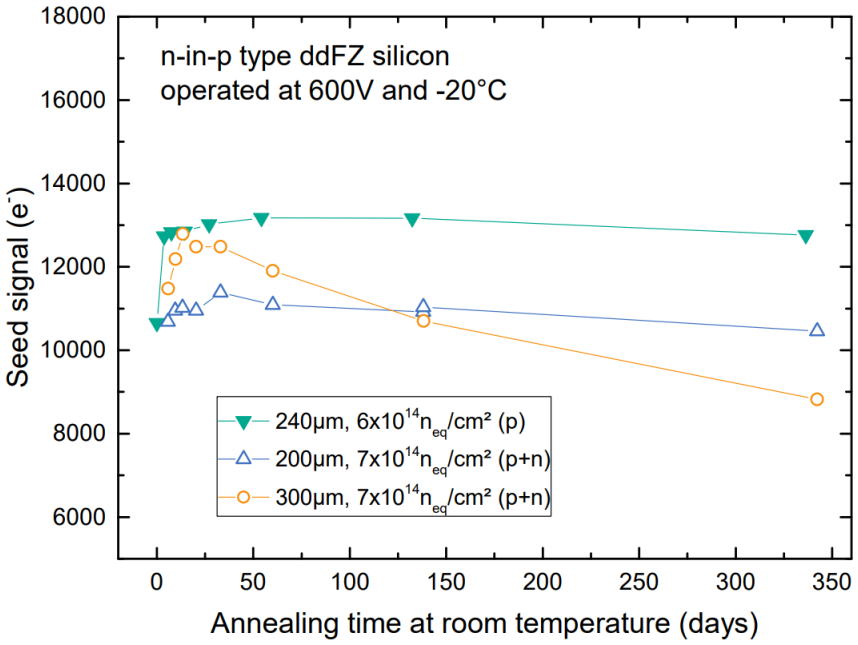


Figure 5.4.: Annealing behavior of sensors with three different thicknesses after an irradiation to $6 \times 10^{14}\,\mathrm{n_{eq}/cm^2}$ and $7 \times 10^{14}\,\mathrm{n_{eq}/cm^2}$. The material with an active thickness of 300 µm shows a pronounced annealing behavior with significant reverse annealing after approximately 20 days at room temperature. Seed signals which are generated in thinner material on the other hand stay more or less constant over long period of time [CMS18].

sensors do not get fully depleted at 600 V at such high fluences. Increasing the bias voltage to 900 V recovers most of the missing charge, but also increases the total power consumption of the device. Furthermore, thin sensors also show slightly higher electric field strengths in the bulk. This leads to higher drift velocities of the charge carriers and makes them less susceptible to trapping.

Another aspect that has to be considered is the annealing behavior of the material. Figure 5.4 shows the annealing of the seed signal of three sensors with different active thicknesses over an annealing period of almost one year at room temperature.

Thick sensors tend to suffer more from reverse annealing than thin sensors, where the seed signal is more or less constant over the whole annealing period. This is particularly advantageous when unexpected maintenance work during operation is required, for which the detector must be heated up to room temperature. All in all, it appears that substrates with an active thickness of less then 300 µm outperform thicker wafer materials after irradiation and are therefore the preferred choice for the future Outer Tracker of the CMS detector.

However, the final decision also depends on the readout chip of the respective silicon sensor and its front-end noise. As a general rule of thumb, the chip threshold should be set to four times its front-end noise and the most probable seed signal in the sensor should be three times higher than the threshold value. This is especially important for chips with binary readout where a hit is only detected when at least the seed signal exceeds the threshold of the chip. In case of the CBC and 9 pF strips attached to it, an electronic noise of about 1000 electrons is expected. This means that the most probable seed signal of the sensor therefore has to exceed at least 12 000 electrons (red line in figure 5.3).

The situation is more relaxed for the PS-p, which is read out by the MPA. With a noise of about 150 electrons [Cer+17], even the worst of the tested substrates has a comfortable margin to the minimal required seed signal of about 2000 electrons [CMS18]. However, physically thinned material is usually harder to handle and also more expensive due to additional processing steps. Therefore, the advantages and disadvantages of thin and thick material must be well balanced before the decision for the mass production is made.

5.2. A Macro-Pixel sensor

The PS module combines two different sensor technologies into one common module: an AC-coupled strip (PS-s) as well as a DC-coupled macro-pixel (PS-p) sensor. Both have a size of roughly 5 mm × 10 mm and are read out by their dedicated readout ASICs. In case of the PS-s, 16 Strip Sensor ASICs (SSAs) are wire-bonded to the individual strips of the sensor while the PS-p is read out by 16 Macro-Pixel ASICs (MPAs) that are bump bonded onto the sensor in order to connect every pixel with its corresponding analog front-end in the chip. The use of pixels instead of strips, and the fact that each channel of the chip is designed for DC readout, lead to some changes in the sensor layout that is shown in Section 4.7.1.

5.2.1. DC-coupled Macro-Pixel sensors

The most notable difference are additional vias between the metal contact and the implant of the pixels. This makes DC coupling much more tolerant to the quality of the coupling oxide and thus more cost-effective compared to AC-coupled sensors which rely on a well-processed, very homogeneous oxide layer to obtain a well-defined coupling between the aluminum and the strip implant. Due to the conductive connection, the implant can also be biased by the virtual ground potential[2] of the individual front-ends of the readout chip, making additional biasing circuits, e.g. the bias ring and polysilicon resistors, obsolete during operation. However, most DC-coupled sensors still feature a global biasing scheme for several reasons. First, the pixel matrix is still surrounded by a grounded bias ring, which protects it from the high voltage at the sensor edge and helps to shape the electric field, reducing the risk of early breakdowns significantly. The ground potential is provided by the chip periphery, which is connected to the bias ring by some additional *bias bumps* that are placed along the ring. Second, by connecting the pixels to the bias ring, high currents will be redirected from the pixels to the common ground of the chip, protecting the front-end electronics and the chip in general. Finally, having a global biasing scheme enables the possibility to test the sensor before assembly with a readout chip. For this purpose ground potential is applied to the bias ring which will be distributed to the individual pixels. In case of the PS-p **P**unch **T**hrough **S**tructures (PTS) are used instead of polysilicon bias resistors to connected the pixel implant with the global biasing scheme. The design and working principle of a PTS is described in the following.

5.2.2. The Punch-Through Structure

Apart from polysilicon bias resistors, punch through structures (PTS) are the most common approaches to connect each individual implant of a segmented silicon sensor to the global bias ring. Applying ground potential to the bias ring without any of these connections between the individual implants and the bias ring would result in an inhomogeneous depletion of the bulk and thus affect all measurements performed during the test procedure. An illustration of one possible design of a PTS is shown in figure 5.5.

[2] A virtual ground is not directly connected to the common ground potential of the chip and is generated by a amplifier circuits and a feedback loop.

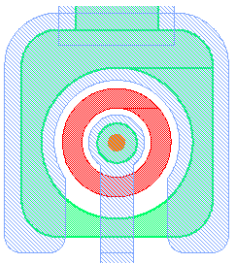


Figure 5.5.: A possible implementation of the punch-through structure (PTS). A hole in the pixel implant (green) is used to house the necessary PTS elements. The bias dot (green circle), which acts as seed for the growing depletion region, is conductively connected (orange) to an aluminum rail (blue) which is connected to the global bias grid. An additional p-stop ring (red) isolates the pixel implant and prevents the pixels from short circuits to the bias dot.

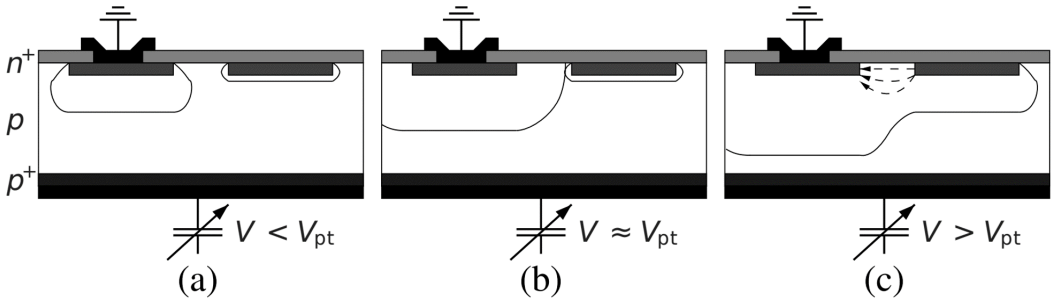


Figure 5.6.: An illustration of the punch-through effect (PTE). As soon as the growing depletion region of the connected implant (a) reaches the SCR of the floating implant (b), excess charge carriers are removed and the two depletion regions are getting merged (c) [Ros+06].

The starting point of a PTS is a hole in the pixel implant (green rounded square) into which an additional implant, the so-called *bias dot* (green circle), is introduced. This bias dot is connected to an aluminum rail (blue) by an aluminum via (orange) through the oxide layer. The aluminum rail is connected to the bias ring and therefore set on ground potential. In order to avoid shorts between the pixel and the bias dot, a p-stop ring (red) is added to the PTS which will break the electron accumulation layer and therefore isolate the pixel properly (see section 4.7.1). The principle behind the PTS is the punch-through effect (PTE), which is illustrated in figure 5.6. The drawings show two implants of an n-in-p silicon sensor, where one is set to ground potential while the other one is kept floating. Even without an external bias voltage, a small space charge region is formed around both implants. By applying reverse bias to the backside of the sensor, the SCR of the connected implant starts to grow into the bulk and approaches the floating implant laterally. As soon as the growing SCR reaches the SCR of the floating implant, the punch-through effect sets in. Excess charge carriers of the floating implant are removed by the connected implant and its potential is adjusted to the connected one. At this point, a common SCR is formed and the depletion of the bulk continues from both implants simultaneously.

The punch-through effect is not limited to the PTS and its biasing purposes. As already mentioned in the previous section, PTS are also used to protect the front-end electronics of the readout chip from unsustainable currents caused by an increased amount of drifting charge carriers in the silicon bulk. The origin of such high currents could be of different nature. One

Table 5.1.: List of isolation variants used for the PS-p prototype wafers, produced at CiS, Germany

Isolation variant	Peak concentration [cm^{-3}]	Implantation depth [µm]
1	1×10^{16}	1.5
2	1×10^{16}	2.5
3	1×10^{17}	2.5
4 (p-spray)	2×10^{15}	0.5

possible reason is an unexpected *beam loss* event, where the proton beam of the LHC leaves its trajectory and interacts with the beam pipe or the collimators, thereby generating large numbers of particle showers that will flood the tracker with ionizing particles. More information about beam losses at the LHC and the associated risks for the silicon tracker can be found in [Fah06].

To summarize, although DC-coupled sensors do not necessarily rely on any kind of biasing scheme, the advantages of PTS are manifold. Especially the testability before assembly is one of the main reasons why the PTS were already implemented on many DC-coupled sensors so far. However, like any other additional structure on a silicon sensor, they also take up valuable space in the pixel cell, which could otherwise be covered by the charge-collecting pixel implant, resulting in a reduced detection efficiency in the detector.

5.3. The PS-p light prototype at CiS

While macro-pixel sensors have already been extensively studied during the HPK campaign [Ber15], the development of the first dedicated PS-p prototypes only started a few years later with the design of the PS-p light prototype wafer, which has been evaluated and produced by CiS [CiS19]. This R&D[3] project was carried out in close cooperation with the chip developers at CERN. This ensured that certain parameters of the sensor and the chip were adjusted to each other in order to be able to produce fully functional detector prototypes at the end. The Institute of Elementary Particle Physics at KIT was heavily involved in the design and qualification process of these first prototype sensors [Pri16]. Similar to other projects in the past, various design variations and sensor materials have been chosen to find an optimized parameter set that will maximize the performance of the final macro-pixel sensors.

5.3.1. Wafer material

The PS-p light prototypes are based on the DC-coupled n-in-p technology and are implemented on a 4-inch p-type float zone wafer. A bulk resistivity of $4\,k\Omega\,cm$ to $8\,k\Omega\,cm$ together with an active and physical thickness of $200\,\mu m$ ensures a full-depletion voltage V_{dep} of less than $100\,V$. Both, p-stop with varying implantation depths and concentrations as well as p-spray isolation with a fixed parameter set have been used, resulting in four different wafer variants which are summarized in table 5.1.

5.3.2. Wafer layout

Every PS-p light prototype wafer includes 30 macro-pixel sensors (PS-p lights), 11 strip sensors, several diodes and various other test structures that are necessary to characterize the wafer

[3] Research and Development

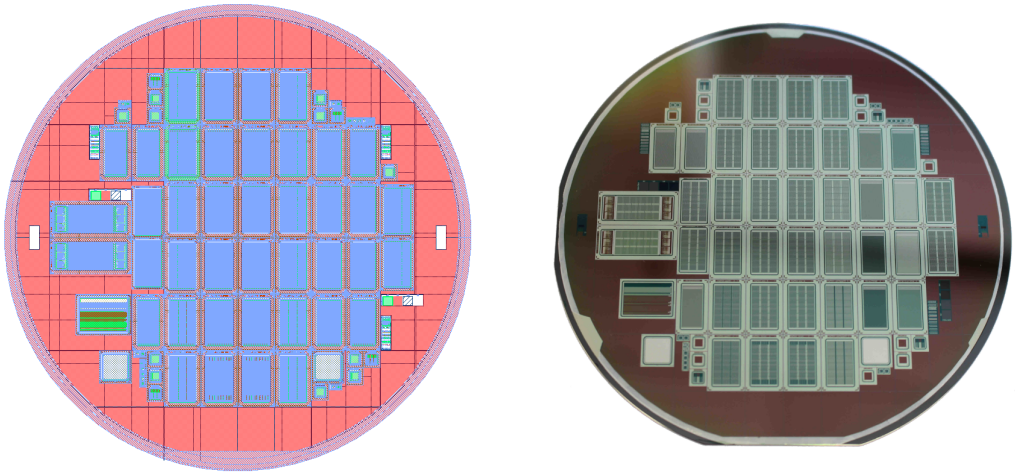


Figure 5.7.: The PS-p light prototype wafer. On the left: output of the design file that is used to save the structures during the design phase. On the right: final wafer produced at CiS.

material and the process quality. The biasing of the strip sensors and the macro-pixels has been achieved by punch-through structures (PTS) with one out of two different geometries (PT v1, PT v2). Sensors with various implantation widths and p-stop geometries have been implemented to understand how the strip isolation is affected by these parameters. Detailed information about the design variations of the sensors together with the corresponding test results are presented in [Pri16].

5.3.3. The PS-p light

The macro-pixel sensors on the PS-p light prototype wafer consist of only 48×6 pixels which already makes it evident why the sensor is called the *light* variant of the final PS-p. While the full-size PS-p sensor which is used for the Outer Tracker PS modules comprises over 30 000 pixels in its matrix, the PS-p light only covers about 2 % of the active area of the full-size PS-p. The advantage of using such small prototypes is the opportunity to accommodate a wider range of design variations onto one single wafer, expanding the R&D project quite extensively. To put this into figures, the 30 macro-pixel sensors placed on a single prototype wafer already contain 11 different design and technology variants, which in turn can be supplemented by one out of four different pixel isolation techniques. One of these PS-p light prototype wafers together with its mask design is shown in figure 5.7.

The 48×6 pixel matrix is subdivided into 6 fields with 16 columns and 3 rows each, which matches the bump bond pattern of one single readout chip. This means that one sensor is read out by a total of six readout chips. Depending on their position on the sensor, the pixels can have one out of four different geometries. The standard geometry which is used for most pixels in the matrix is $100\,\mu m \times 1446\,\mu m$. Pixels in the first and last row are elongated by 300 µm towards the edge of the sensor to cover as much area below the periphery of the bump bonded readout chip as possible. Additional *gap pixels* that are read out by an edge channel of the readout chip are twice as wide than the standard pixels (200 µm) in order to cover the space between two adjoining readout chips. Gap pixels that are located in the first and last row of the sensor are both, widened and elongated compared to the standard pixels, which gives the total number of four different pixel geometries. Both approaches, widening and elongating the pixels, aim to maximize the active area of the sensor and thus the efficiency of the assembly. However, the pitch between the pixel cells, more precisely the bump bond pads, remains the

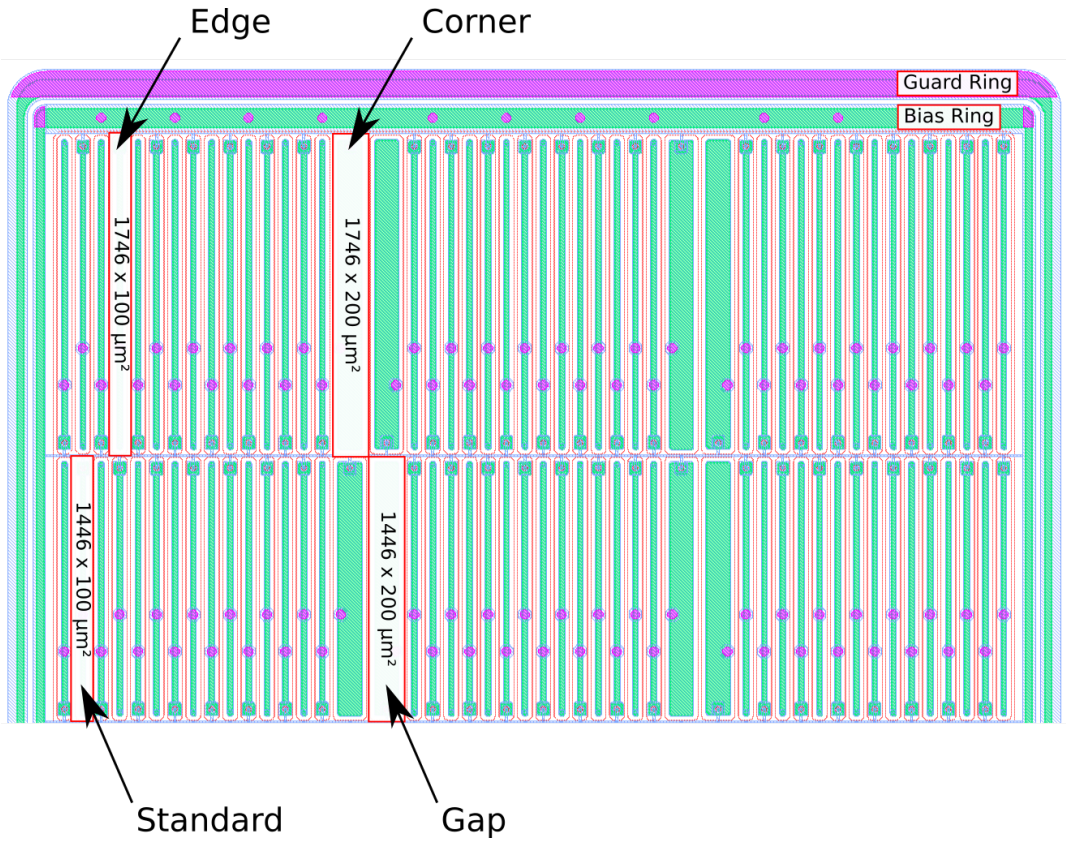


Figure 5.8.: Two rows of the PS-p light standard layout. Pixels in the first and last row are 300 µm longer than all the other pixels on the sensor. Four columns of gap pixels are widened to cover the space between two adjoining readout chips. The whole pixel matrix is surrounded by a bias and guard ring and enclosed by the sensor edge (not shown).

same as with the standard geometry. Two rows of the final PS-p layout, including all four pixel geometries are shown in figure 5.8.

The standard pixel implant within the 100 µm wide pixel cell has a width of 25 µm, which leads to a width to pitch ratio of $w/p = 0.25$. This ratio is considered as the default value for all Outer Tracker sensors, including the PS-s and 2S strip sensors. Only the gap pixels that are twice as wide as the standard pixels include wider pixel implants of 125 µm. In both cases the remaining 75 µm are used to add an individual p-stop ring to the pixel cell in order to properly isolate the pixels from each other.

Each of those pixels in the matrix contains its own punch-through structure that is connected to the bias ring or an aluminum bias rail that runs between two adjacent pixel rows and the bias ring. As a result, all pixels can be biased simultaneously by simply applying ground potential to the global bias ring. The bias ring is complemented by a single guard ring and the sensor edge, forming the sensor periphery that is based on the well-established sensor periphery used for the sensors of the HPK campaign.

The standard layout is the starting point of all other design variation that have been implemented on the PS-p light prototype wafer. A comprehensive list of all design variations and their main differences is given in table 5.2.

The large number of design variations allows to perform detailed studies of individual parameters and their influence on the sensor performance. However, the results presented in

Table 5.2.: List of all PS-p light design variants on the PS-p light prototype wafer, produced at CiS.

Name	Pixel width	Gap pixel width	Edge width	Comments
Std (wp025)	25 µm	125 µm	850 µm	Standard layout
wp03	30 µm	125 µm	850 µm	Wider pixel implant
wp04	40 µm	125 µm	850 µm	Wider pixel implant
wp04gap40	40 µm	40 µm	850 µm	Smaller gap pixels
wp025gap50	25 µm	50 µm	850 µm	Smaller gap pixels
edge350	25 µm	125 µm	350 µm	Smaller sensor edge
edge500	25 µm	125 µm	500 µm	Smaller sensor edge
Open p-stop	25 µm	125 µm	850 µm	Open p-stop ring for biasing
Inverted	25 µm	125 µm	850 µm	Additional routing
Spark	25 µm	125 µm	850 µm	n-type edge
Brick	25 µm	125 µm	850 µm	Bricked/Staggered layout

the following are confined to only few of these parameters and design variants. Further studies and a more detailed description of all the sensors on the PS-p light prototype wafer, including the strip sensors, can be found in [Pri16].

5.4. Sensor Qualification

Every single component of the Outer Tracker modules has to meet certain requirements in order to be accepted for further use in the assembly process. For this reason, dedicated test setups have been developed to qualify the individual parts and reject single units that do not meet the specifications. All specifications for the future Outer Tracker can be found in the Technical Design Report (TDR) of the Phase-2 Upgrade of the CMS Tracker [CMS18].

For silicon sensors the most important part is the electrical characterization of the sensor material as well as the validation of the implemented design. This is achieved by performing a number of test procedures on dedicated test pads that are distributed across the sensor surface. In the R&D phase of the detector development, good sensors are subsequently connected to one or several readout chips to determine the signal height and charge collection efficiency of the underlying sensor material. Ultimately, the performance of the system is evaluated in a beam test, where the efficiency of the sensor and the whole readout chain is determined. The different setups that have been used to characterize several PS-p prototypes throughout this thesis are presented in the following.

5.4.1. The ETP probe stations

The Institute for Experimental Particle Physics at KIT owns two custom needle setups that are used to contact the small test pads on the sensor and perform the electrical measurements. One of the two ETP *probe stations* is shown in figure 5.9.

The setup includes a darkened shielding box to protect the sensor from light induced current that could impair the test results during the measurement. Inside the box, the sensor is placed on a movable and coolable vacuum chuck that keeps the sensor in place and cools it down to approximately $-20\,°C$ if required. In order to avoid condensation on the chuck the box is constantly flushed with dry air, which keeps the dew point in the box below the set temperature on the sensor. A microscope and a camera are added to the setup to guide the user during

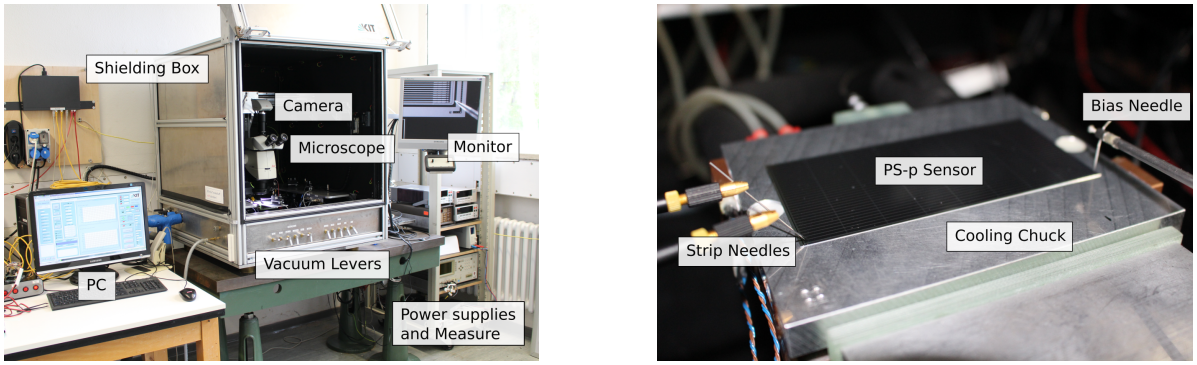


Figure 5.9.: Pictures of one out of two probe station setups at ETP. The movable and coolable vacuum chuck is placed in a darkened shielding box which is constantly flushed with dry air. The chuck is surrounded by up to four needles that are used to contact the test pads on the sensors. The power supplies, measuring devices and all other test equipment is controlled by LabVIEW or Python based software package.

the needle placement. The needles are mounted on high precision needle holders which again are connected to various different power supplies and measuring devices that are necessary to perform the desired qualification measurement. Up to four needles can be used in the setup in order to characterize a sensor completely. Almost all of these measurements require the sensor to be depleted. This is achieved by setting the chuck and thus the backside of the sensor on high voltage, while one of the needles, the *bias needle*, is placed on the bias ring and provides the necessary ground potential to it. All other needles are used for contacting individual or neighboring pixels and determining their corresponding pixel and inter-pixel properties. Three movable stages (x, y, z) on which the chuck is mounted, make it possible to contact all pixels consecutively without having to reposition the needles manually.

The whole setup is controlled by a LabVIEW[4] or Python based software package which is used to select, record and store user defined measurements and finally upload them into a common database.

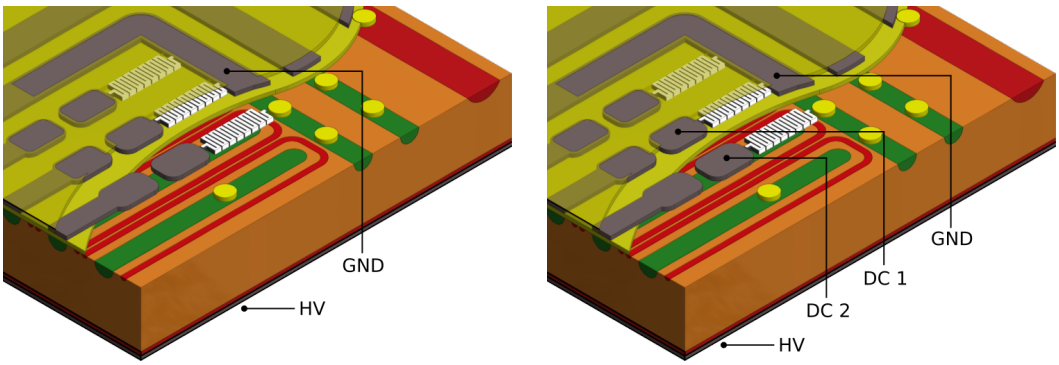
5.4.2. Probe station measurements

Depending on the needle positioning on the sensor and the devices connected to them, different properties of the sensor can be determined. Figure 5.10 shows the two most common needle configurations to acquire all necessary properties of a DC-coupled sensor. Global parameters can be obtained by solely placing the bias needle onto the bias ring and applying high voltage to the backside. To obtain the individual strip or pixel parameters, up to four additional needles are required, which have to be placed on several pads along the strips or pixels. Since this work is concentrating on DC-coupled macro-pixel sensors without any AC-coupled contacts, measurements including those are omitted.

5.4.3. I(V) and C(V) measurements

The two most basic measurements of all position sensitive silicon sensors and even diodes are the current-voltage I(V) and capacitance-voltage C(V) characteristics. Both measurements only require the bias needle to be connected to the bias ring and high voltage applied to the backside of the sensor. The I(V) characteristic is obtained by applying an increasing bias voltage to

[4] **Lab**oratory **V**irtual **I**nstrumentation **E**ngineering **W**orkbench developed by National Instruments™



(a) (b)

Figure 5.10.: Needle configurations for PS-p measurements. For I(V) and C(V) (a) measurements only one needle has to be placed onto the bias ring and set to ground potential, while the backside of the sensor is set to high voltage. For pixel and inter-pixel measurements (b) up to two additional needles have to be placed onto two adjoining DC (bump bond) pads.

the backside of the sensor while measuring the current through the bias needle. If the sensor includes any kind of biasing scheme, all strips or pixels are connected to the grounded bias ring and the I(V) measurement provides valuable information about the total current of the entire sensor and its high voltage stability. In case of the sensors for the CMS Outer Tracker, a leakage current of less than $2\,\mathrm{nA\,mm^{-2}}$ and a breakdown voltage above 700 V is required to declare the sensor good.

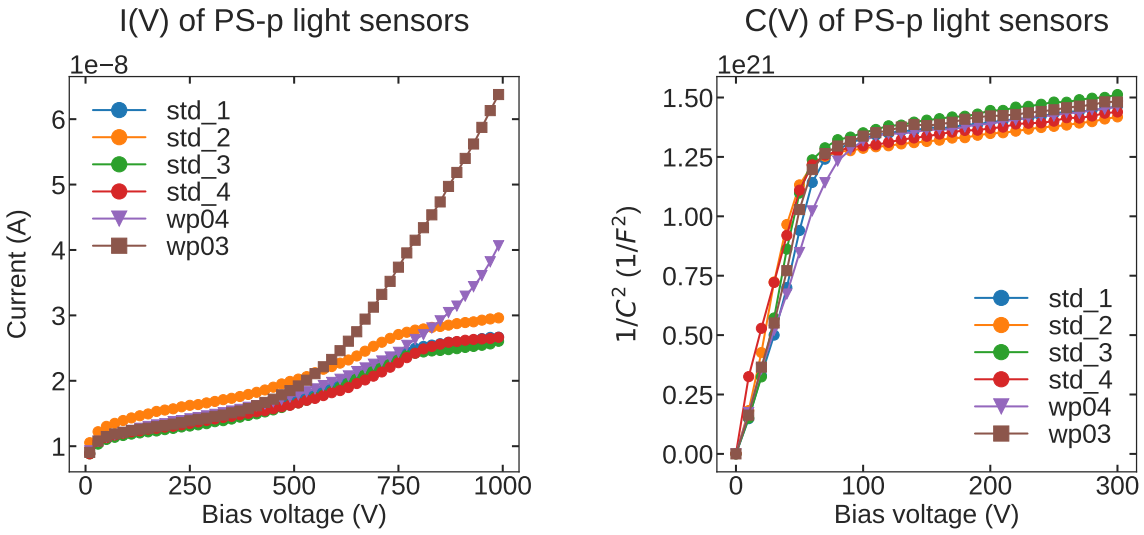
The capacitance-voltage C(V) characteristic of a silicon sensor is obtained by measuring the capacitance with a connected LCR meter while performing the same bias sweep as before. For all C(V) measurements a frequency of 1 kHz is chosen. The resulting C(V) characteristic is then used to determine the depletion voltage of the device according to equation 4.13.

5.4.4. I_{leak}, R_{int} and C_{int} measurements

Pixel and inter-pixel measurements on DC-coupled pixel sensors are confined to three measurements: the leakage current I_{leak} of an individual pixel, the resistance R_{int} and the capacitance C_{int} between two neighboring ones. Since there are usually no dedicated test pads for pixels on a sensor, the bump bond pads are used, which are equivalent to DC pads in that case.

The pixel leakage current I_{leak} corresponds to the current that is conducted by a single grounded pixel in the matrix. For this purpose, one additional needle (indicated in figure 5.10 as DC 1 or DC 2) is placed on the bump bond pad of a pixel and connected to ground potential. The specifications of the Outer Tracker sensor community state that one pixel should not drain more than 300 pA in order to avoid any damage to the front-end electronics of the readout chip [CMS18]. In addition, the sum of the individual pixel currents should approximately equal the total leakage current of the sensor.

For the inter-pixel measurements, R_{int} and C_{int}, two needles have to be placed onto the bump bond pads of two neighboring pixels. The inter-pixel resistance R_{int} is determined by connecting an additional low-voltage power supply to the DC needles and applying a voltage ramp from 0 V to 2 V to them. By measuring the current in the low-voltage circuit and using Ohm's law, the inter-pixel resistance R_{int} can be calculated. In case of DC-coupled sensors like the PS-p light, R_{int} has to exceed at least the input impedance of the readout chip to ensure a proper pixel insulation. Only then, the charge is collected by the seed pixel and is not distributed among the surrounding pixels. In case of the readout chip of the PS-p light, a



(a) **(b)**

Figure 5.11.: I(V) (a) and C(V) (b) characteristics of six PS-p light sensors. All four PS-p sensors with the standard layout show no evidence of any failure up to a bias voltage of 1000 V. The two sensors with an increased width to pitch ratio of 0.3 and 0.4 on the other hand indicate a soft breakdown which is still within the exclusion limit set by the Outer Tracker community. All six sensors, regardless of their design are fully depleted at a bias voltage of about 80 V.

maximum input impedance of 4 kΩ is expected [Cer17]. Thus, an inter-pixel resistance in the order of 10 kΩ is required. Nevertheless, the CMS Outer Tracker community has specified that an inter-pixel resistance of $R_{\text{int}} \geq 6.6\,\text{G}\Omega$ must be achieved on each pixel to declare the pixel insulation of the sensor good [CMS18].

The last parameter, the inter-pixel capacitance C_{int}, determines the crosstalk between two neighboring pixels and makes a significant contribution to the overall pixel capacitance. Both effects have a big influence on the performance of the final assembly and should be as small as possible. Crosstalk describes the effect of capacitively induced signals in adjacent pixel cells, which considerably reduces the seed signal and impairs the resolution of the final detector. A high pixel capacitance on the other hand leads to higher noise in the front-end channels and thus affects the signal to noise ratio (S/N) and the minimal threshold that can be set by the readout chip. However, only the capacitance to one adjacent pixel can be determined with the present probe station setup and the C_{int} measurement. In order to determine the total capacitance of a pixel, the remaining seven pixels as well as the backside of the sensor should be taken into account. In the end, an input capacitance of 500 fF per channel [Cer15] is expected by the readout chip developers. Further information about the total pixel capacitance and a more detailed view on this topic can be found in [CE97].

5.5. Measurements of the PS-p light

Figure 5.11a shows the I(V) characteristics of six PS-p light sensors. Four of these sensors are based on the standard layout and two with slightly wider pixel implants of 30 µm ($w/p = 0.3$) and 40 µm ($w/p = 0.4$).

All four sensors with the standard layout show no evidence of a faulty behavior up to the required bias voltage of 700 V. The two more aggressive designs on the other hand show first indications of a *soft breakdown* that describes the exponential increase in current at higher bias voltages instead of a sharp breakdown that is normally expected. Nevertheless, the current specifications only require that the current at 700 V must not exceed more than three times the current that is conducted at 500 V [CMS18]. Even with this additional exclusion criterion, all sensors shown in figure 5.11a are still within the specification.

The C(V) characteristics of the same six PS-p light sensors are shown in figure 5.11b. It is immediately apparent that the C(V) characteristics of all six sensors, regardless of their design, are identical. The reason for this is that all sensors are based on the same silicon substrate, which determines the course of the C(V) measurement. The pronounced kink at about 80 V marks the point of the full depletion voltage V_{dep} and lies well below the upper limit of $V_{\text{dep}} < 150\,\text{V}$ for silicon substrates with a thickness of 200 µm set by the Outer Tracker community [CMS18]. All subsequent measurements are performed at a bias voltage well above the depletion voltage and below the breakdown voltage. This ensures that the SCR in the device is maximized and that the sensor is operated properly.

The inter-pixel measurements of one PS-p light with the standard geometry are summarized in figure 5.12. The first two-dimensional pixel map in figure 5.12a shows the result of the I_{leak} measurement of every second pixel on one PS-p light. On average, each pixel is draining about 50 pA which fits well into the specifications and matches the fraction a single pixel should drain compared to the total current of about 12 nA. Elongated pixels in the two outermost rows and wider pixels between the individual sections connected to one readout chip drain higher currents due to their increased pixel implant size. Two pixels in the first row show an increased leakage current that could be caused by a simple pixel defect or mechanical damage of the sensor in that particular region.

Figure 5.12b shows the result of the measurement of the inter-pixel resistance R_{int} of the same pixels on that particular sensor. With a pixel length of almost 1.5 mm, the inter-pixel resistance should exceed at least 6.6 GΩ in order to declare the sensor good. The two-dimensional pixel map illustrates that all measured pixels except the defective one in the first row easily reach the required inter-pixel resistance and even exceed 1 TΩ in some cases.

Inter-pixel capacitance measurements of the macro-pixel sensors are not required during the sensor qualification process. Nevertheless, by comparing the measurements with the specifications of a strip sensor at least a feeling for the quality of the measurement and the material can be obtained. Thus, a maximum inter-strip capacitance of $C_{\text{int}} = 1\,\text{pF}\,\text{cm}^{-1}$ would be the limit at which the sensors would still be used for the final modules [CMS18]. Figure 5.12c shows the result of the inter-pixel capacitance measurement of every second pair of pixels on the PS-p light with the standard geometry. Two pixels with very low capacitances are immediately noticeable that are either defective or have had poor contact with the needles during the measurement. The latter is not unlikely, considering the very small and fragile bump-bond pads that have to be contacted during these measurements. While the inner four pixel rows show an average inter-pixel capacitance of about 0.08 pF, the outer two pixel rows show slightly higher values which originate from the elongated pixels and consequently higher capacitances to one of their neighboring channels. However, by normalizing the inter-pixel capacitance to the length of each individual pixel a global average of about $C_{\text{int}} \approx 0.6\,\text{pF}\,\text{cm}^{-1}$ is achieved. Due to the fact that strip sensors of the same material are expecting similar values the results seem to be plausible.

In summary, it can be said that the electrical properties of the PS-p light are well in agreement with the specifications defined by the Outer Tracker Sensor community and that the wafer material as well as the sensor design would be suitable for the final PS-p sensor.

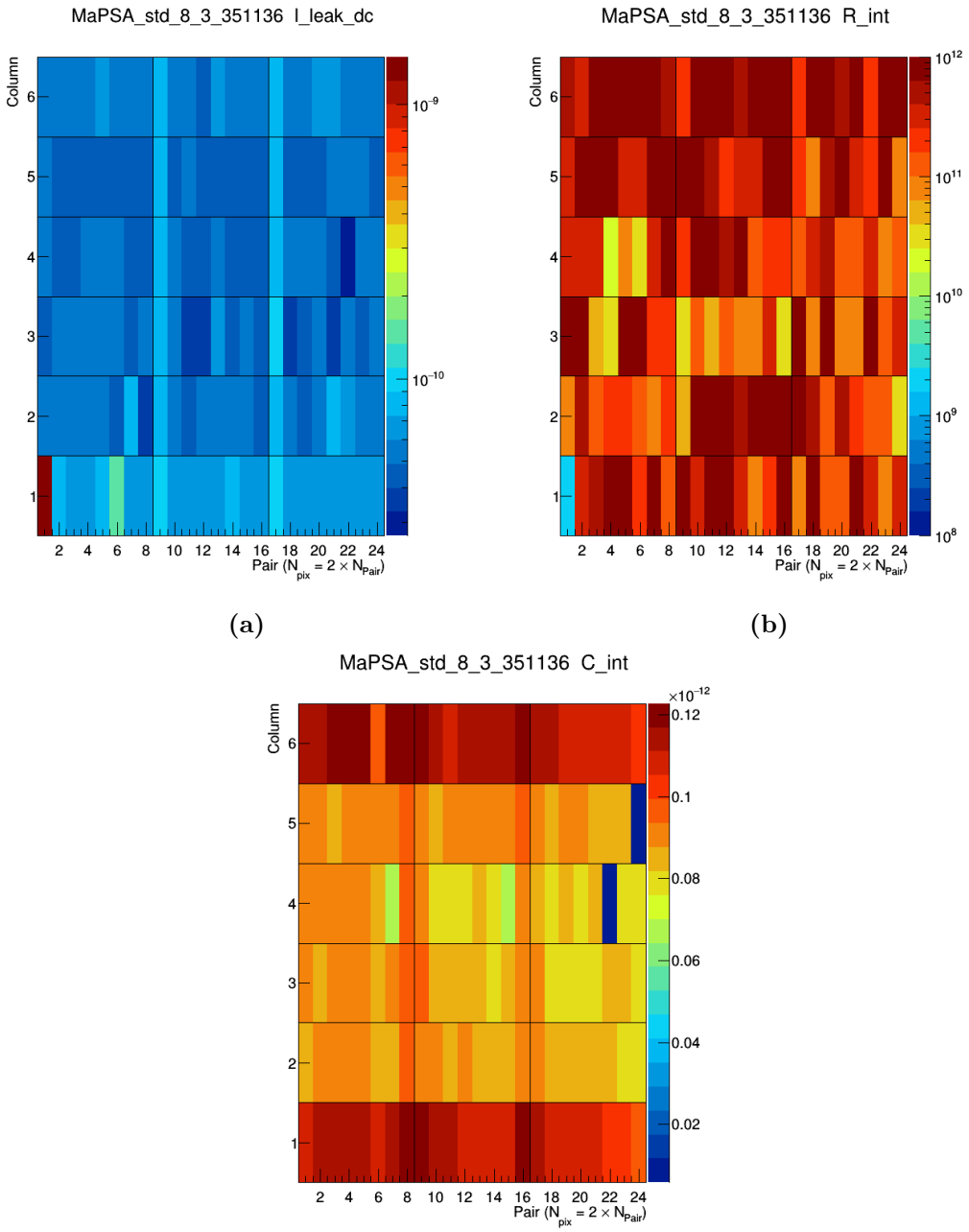


Figure 5.12.: Inter-pixel measurements of the PS-p light. Only every second pixel pair is measured to avoid reallocation of the needles. The pixel leakage current I_{leak} (a) is measured on one of the two pixels only. Inter-pixel resistance R_{int} (b) and inter-pixel capacitance C_{int} (c) are measured within one pair. The increased current and low resistance, measured on the first pixel in the first row can be caused by a pixel defect or mechanical damage in general. Pixels in the first and sixth row show higher capacitances due to their longer pixel implants.

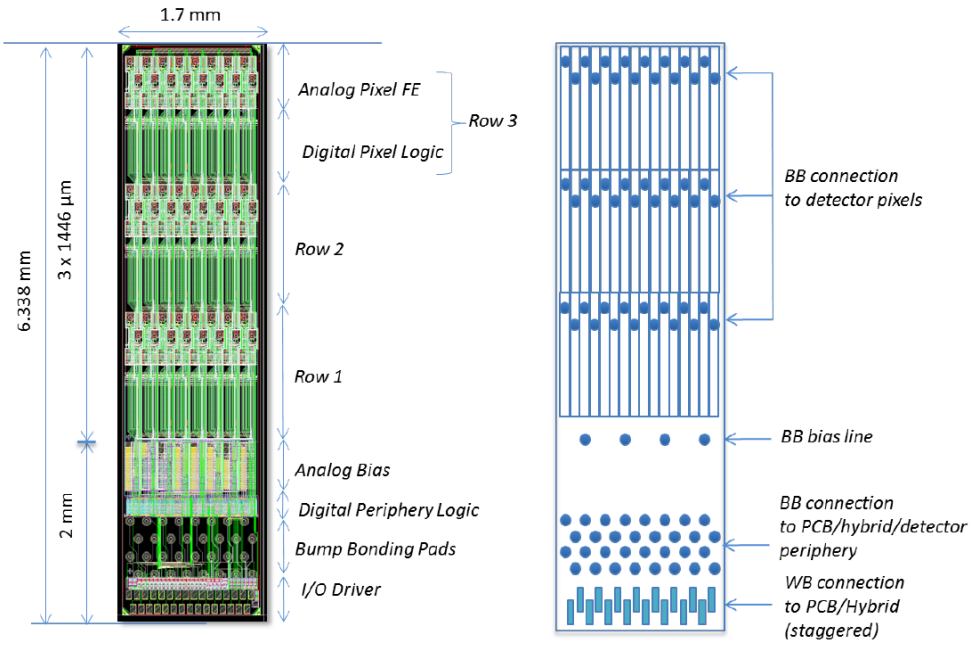


Figure 5.13.: Schematics of the MPA-Light. On the left: final design and description of the MPA-Light and its individual sections. On the right: all electrical connections of the chip, including the bump bond pads of the analog front-ends, the ground pads of bias circuit as well as the bump bond and wire bond pads for the external connection [Cer15].

5.6. The MaPSA light

All sensors that show good electrical properties during the probe station measurements are qualified to be connected to their corresponding readout ASIC. By doing so, further analysis and qualification steps can be performed that provide additional information about the sensor performance. This includes signal height, signal to noise ratio, crosstalk and most importantly the charge collection efficiency (CCE). In case of the PS-p light, whose results have been shown and discussed in the previous section, up to 6 MPA-Light readout chips are bump bonded to the sensor, forming the light version of the Macro-Pixel SubAssembly or *MaPSA light* for short. The MaPSA light is then glued and wire bonded to a PCB that acts as a carrier board for the individual assemblies. A dedicated readout system with the corresponding mounting for the carrier board is then used to calibrate and read out the final assembly. The MPA-Light, the assembly procedure and the necessary readout system are introduced in the following.

5.6.1. The MPA-Light

The dedicated readout chip for the PS-p sensor is called Macro-Pixel ASIC (MPA). Similar to the PS-p, the chip designers decided to develop their first prototype as a smaller variant of the final chip which has been scaled up to the final size later on. A schematic of the MPA-Light together with its bump bond pattern is shown in figure 5.13.

The light version of the MPA has a total size of about $6.3\,\mathrm{mm}^2 \times 1.7\,\mathrm{mm}^2$ and comprises 48 pixel front-ends divided into an array of 3 rows and 16 columns. Four additional bias bumps below the pixel matrix are used to connect the bias ring of the sensor with the ground potential of the analog bias circuit on the chip. Multiple staggered wire bond pads at the end of the

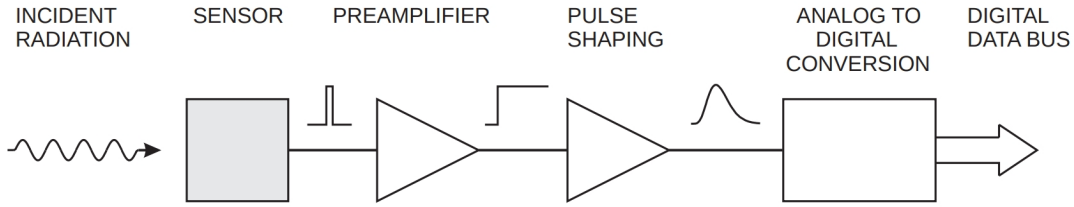


Figure 5.14.: Signal processing of a readout chip. The short pulse that is generated inside the sensor is passed to the preamplifier which integrates and amplifies the incoming signal and passes it to the pulse shaping circuit. There the signal gets differentiated again and smoothed by a low-pass filter. The final shaper output is then digitized and fed into the digital bus of the chip [Spi05].

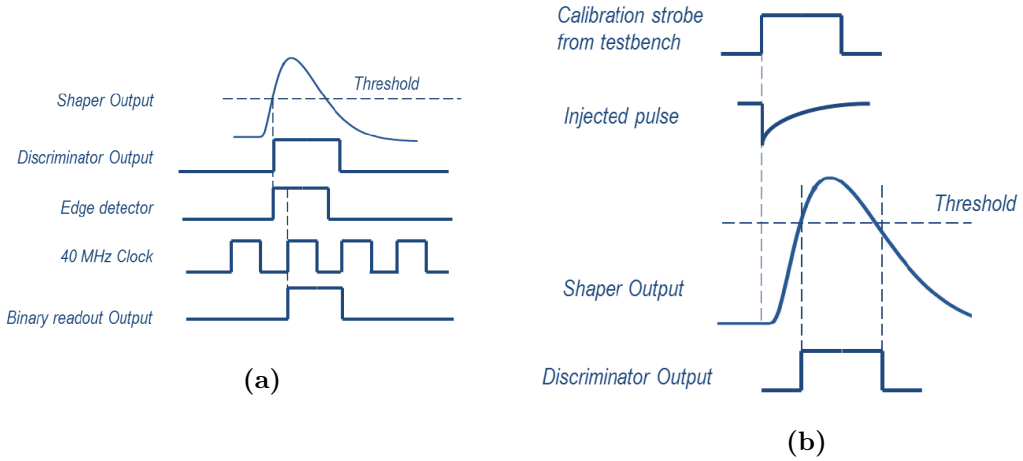


Figure 5.15.: The MPA-Light acquisition modes. In synchronous acquisition (a) the discriminator output is passed to an edge detector that generates a signal of exactly one clock cycle which is subsequently sampled by the global 40 MHz clock. The asynchronous acquisition (b) only detects the positive edge of the discriminator output and increases a 16-bit ripple counter that is implemented in every pixel cell [Cer15].

chip serve as interface to the outside world and are used to connect the chip with a carrier board. The MPA-Light also offers the possibility to use bump bonds instead of wire bonds for the external connection of the chip. The idea here is to implement the wire bond pads and necessary routing lines on the sensor side and thereby flipping the whole assembly by 180° in the final module. The corresponding sensor for such kind of approach is the *inverted* PS-p light that exists twice on each PS-p light prototype wafer. The inverted approach may have various advantages, which are not discussed further in this thesis.

Each front-end channel of the MPA-light, or any readout chip in general, consists of multiple stages to digitize the analog signal of the sensor, which are shown in figure 5.14. The first stage, the preamplifier, integrates and amplifies the incoming pulse of the sensor and passes it the pulse shaper. There the signal gets differentiated again and is passed through a low-pass filter which leads to a typical shaper output that has to be digitized. This final analog-to-digital conversion can be very different among different readout chips, but also between various acquisition modes of a single chip. The MPA-Light contains two of these acquisition modes that can be used simultaneously: asynchronous and synchronous acquisition. Both concepts are illustrated in figure 5.15. The synchrony in this case refers to the global 40 MHz clock that

samples the discriminator output of the analog front-end of the pixels. In both cases the data acquisition is initiated by opening a global shutter on the chip. As soon as the shaper output exceeds the adjustable threshold of the discriminator, a pulse is generated that persists until the shaper output drops below the threshold again. In synchronous acquisition, the output of the discriminator stage is passed to an edge detector that generates a signal of exactly one clock cycle in length, no matter how long the output of the discriminator actually is. This pulse is then synchronized with the 40 MHz clock and subsequently sent to the memory in the chip periphery. The memory stores up to 96 full events that include at least one hit in the whole pixel matrix (*zero-suppression*) along with a time stamp which counts the number of clock cycles from the begin of the acquisition. Before the memory exceeds its capacity, the chip has to be read out by an FPGA to free up the space of the memory for further data acquisition. It should be noted that the MPA-Light offers additional other synchronous acquisition modes, like the centroid extraction mode, that will not be discussed any further.

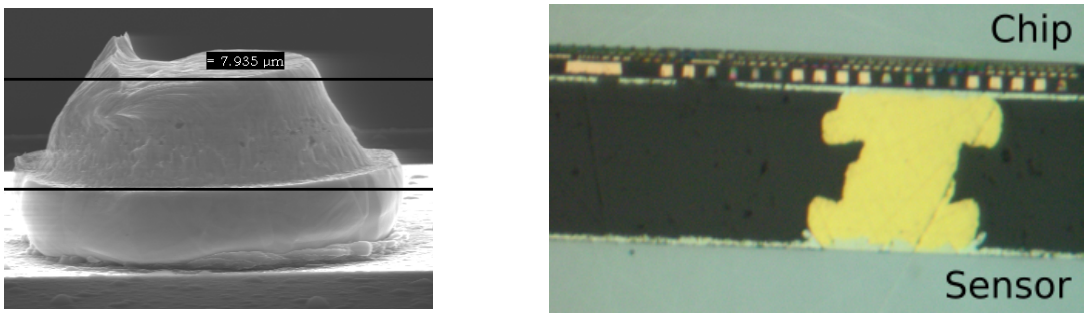
The asynchronous acquisition on the other hand operates independently of the global 40 MHz clock. Instead, it uses a 16-bit ripple counter that is implemented in every pixel cell, which counts the number hits since the beginning of the acquisition cycle. Every time a positive edge of the discriminator output is detected, the ripple counter of the corresponding pixel is increased by one. At the end of the acquisition, all values are concatenated into one long byte string which is then passed to the readout system. Once the transaction is complete, all ripple counters are cleared, preparing the chip for the next acquisition cycle [Cer15].

Both readout modes are used for various different tasks during the chip testing and the readout of the assembly later on. However, this work is mainly focusing on the asynchronous acquisition mode which is more than sufficient for all use cases concerning the sensor qualification procedure.

5.6.2. Assembly process using gold-stud bump bonding

Silicon wafers are usually coated by a comprehensive passivation layer to protect the underlying structures from scratches and other external impacts. The only possibility to contact the buried structures are small passivation openings that are placed above the dedicated aluminum pads. However, in order to establish a reliable connection through the passivation, these openings have to be filled with a conductive material and connected to a solder pad that is placed on top of the passivation layer. For that reason, silicon wafers including pixel sensors are usually post processed and equipped with under bump metallization (UBM) that serves as conductive material in the openings as well as solder pad (bump bond pad) for the final interconnection. The actual connection between the sensor and the readout chip is established by small solder bumps that are placed on either of the two. These small balls are often made out of indium (In) or a tin-lead alloy (SnPb), which makes them quite soft and fusible at comparably low temperatures. When the chip is placed on top of the sensor, or vice versa, the assembly is heated up to the melting point of these solder balls which then form a quite robust connection between the two opposite UBM pads. However, both processes, creating the under bump metallization as well as placing the solder bumps onto them, require additional processing steps which are only practical on wafer level. The reason for this is that both processes include additional lithographic steps which require high precision mask alignment that can only be assured on wafer level.

However, smaller R&D projects like the PS-p light and the MPA-Light project, often sacrifice some, if not all, of their wafers that will not be post-processed at all and thus cannot be used for standard assembly later on. These wafers are immediately cut into single *dice* by the manufacturer or the institutes, which are sent to the developers for their testing procedures.



(a) (b)

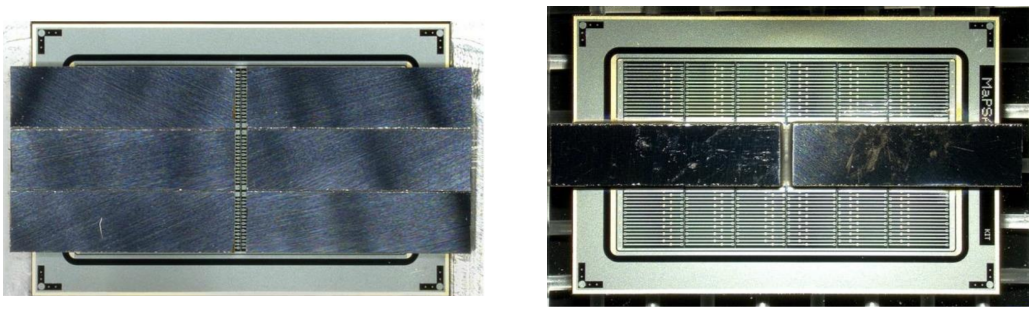
Figure 5.16.: Scanning electron microscope image of a gold-stud (a). The plateau at the bottom of the stud indicates the edge of the capillary. The small remnant at the top left of the stud is created when the capillary shears of the wire from the stud [Jun14]. Cross section of a bump-bonded assembly (b). The gold-studs are well aligned to each other and form a strong interconnection.

In order to still be able to use the diced material for assemblies later on, the Institute for Data processing and Electronics (IPE) at KIT developed the alternative gold-stud bump placing process, which requires no lithographic steps and even works with single dice [Kud14]. The gold-stud bumping process utilizes a ball bonding machine that is equipped with a very thin gold wire, typically about 20 µm to 30 µm in diameter, which is guided through a small ceramic capillary. The whole process is initiated by an electrical discharge between an electrical contact and the gold wire at the end of the capillary. This discharge, also called the electrical flame off (EFO) melts the gold wire and thereby creates a small spherical free air ball (FAB) at its end. The FAB is then pressed onto one passivation opening of the pre-heated silicon die. By applying ultra-sonic power to the system, the FAB gets welded onto the aluminum pad below the passivation opening. After the FAB is placed, the capillary moves a bit upwards and then sideways to shear off the wire from the remaining gold-stud bump. A scanning electron microscope picture of the final gold-stud is shown in figure 5.16. This process is repeated until all bump bond pads of the die are covered by these gold-studs. More information about the gold-stud bump bonding technique can be found in [Kud14].

The next step in the whole assembly procedure is the actual flip-chipping process. For this purpose, the sensor is placed on a heated chuck with its bumps facing upwards. The machine then uses a pick-up tool to pick up one MPA-light at a time and places it on its dedicated position on the sensor. The machine uses pattern recognition algorithms to find the optimal position of the chip and aligns the two parts accordingly. As soon as the chip and sensor are brought into contact, high forces of up to 400 N are applied to the sandwich while it is simultaneously heated up to temperatures around 200 °C. This deforms the studs and form a strong interconnection between them. For the MaPSA light this procedure is repeated up to six times until the sensor is fully equipped. However, due to dicing issues at the manufacturer, most of the MPA-Lights are slightly wider than expected and thus, placing two of them next to each other was often not possible. For that reason most assemblies produced at KIT are only equipped with two instead of six MPA-Lights. Figure 5.17 shows two of the final MaPSA light assemblies, one with six and one with only two MPA lights bonded vis-à-vis.

5.6.3. Spark protection with underfill

One problem that arises from the flip-chipping process is the risk of destroying the assembly by electrical discharges between the sensor and the grounded readout chip. As already mentioned



(a) **(b)**

Figure 5.17.: Two MaPSA light assemblies. In order to read out all macro-pixels, the PS-p light is supposed to be equipped with six MPA-Lights (a). However, due to unexpected dicing issues, most assemblies produced at KIT only contain two readout chips (b).

in section 4.7.1, the p^{++} edge, the p^{+} bulk and the p^{++} backside form a conductive channel which sets the sensor edge at the front-side on the same potential as the backside. The now bump bonded and grounded readout chip crosses the sensor edge at least once where its wire bond pads are located. The arising potential difference in the overlapping region could then lead to an electrical discharge which would destroy the readout chip and consequently the whole assembly. The risk of sparking mainly depends on the distance between the two dice and the insulation material in between. In case of gold-stud bump bonding, the distance is solely defined by the size of the gold-studs and their deformation during the bonding process. Typical distances for this kind of bump bonding technique are in the order of 50 µm to 80 µm. Assuming the gap is filled with nothing but the surrounding air which can withstand up to $3\,\mathrm{V\,\mu m^{-1}}$ (see e.g. [TM14]) the maximum bias voltage that can be applied to the sensor without sparking is 240 V. For non-irradiated sensors with a typical depletion voltage of $V_{\mathrm{Bias}} \leq 150\,\mathrm{V}$ this is more than enough to operate the sensor even slightly over-depleted. However, the situation changes for irradiated assemblies which often require bias voltages above 600 V to deplete the bulk and reach maximum efficiency. These assemblies in particular demand further pre-cautions to protect the edge from sparking. The most common and easiest solution is the application of *underfill*, a mostly silicone based elastomer with very low viscosity and high dielectric strength. The low viscosity is necessary to allow the material to creep into the very thin gap and completely fill the area at the edge. Various different elastomeres have been tested in the last few years before and after irradiation and all of them seemed to be suitable for this specific kind of application. In case of the MaPSA light and all future macro-pixel prototypes, EPO-TEK ® 301-2 with a dielectric strength of $20\,\mathrm{V\,\mu m^{-1}}$ [Kre18] and a shelf life of about one year at room temperature [Epo18] was used and has become the preferred underfill of choice.

5.7. The MaPSA light readout system

All assemblies are finally glued and wire-bonded to a PCB carrier board which is necessary to connect the assemblies with their dedicated readout system. One of these carrier boards including a fully wire bonded MaPSA light is shown in figure 5.18.

The PCB carrier is equipped with two high speed, high density quad row SMT[5] connectors on its backside that provide enough connections to address all six MPA-Lights at once. For further use, the carrier board is covered by a 3D-printed enclosure that protects the assembly

[5]acronym: **S**urface-**M**ount **T**echnology

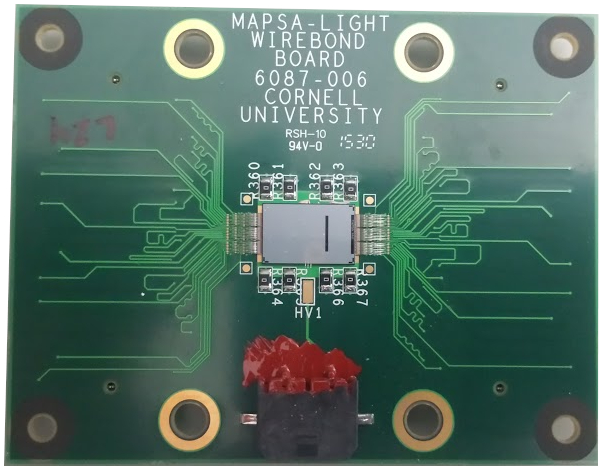


Figure 5.18.: Fully equipped MaPSA light wire bonded to its carrier board. The two high pin count connectors on the backside are only indicated by two guiding holes on the left and on the right end of the PCB. Three MPA-Lights are routed to one of these two connectors. The black terminal at the bottom serves as high voltage connection for the sensor, whose upward facing backside is wire bonded to the connected high voltage pad (HV 1) next to the assembly.

from damage, electromagnetic radiation and light induced current in the sensor. The whole package can then be plugged onto a custom made daughter board, developed by the Rutgers University in the United States of America, which houses all necessary routing lines and voltage regulators to operate the MaPSA light. A high pin count FMC to FMC cable finally connects the daughter board with an FPGA-based evaluation board that controls the MaPSA light and also serves as readout system during the data acquisition. In case of the MaPSA light, the CERN-internal Gigabyte Link Interface Board (GLIB) is used. The GLIB is based on Xilinx' Virtex-6 FPGA series which serves two high pin count FMC slots with 80 differential I/O pairs each. An on-board Ethernet port and separate power connection allows easy bench-top operation and avoids the use of any additional hardware except a PC the setup is connected to and controlled from [Vic+10]. The whole setup is presented in figure 5.19.

A small JTAG[6] programmer is used to upload custom firmware to the FPGA and adapt the board to the needs of the user. The ability to upload dedicated user firmware makes the board extremely versatile and therefore suitable for a wide variety of user applications. The user firmware for the MaPSA light was developed by Rutgers University and provides all necessary functionality to test, calibrate and operate the assembly. However, some modifications were necessary to prepare the setup for test beam operation other than at Fermilab, which will be explained in more detail in the next chapter.

[6]acronym: **J**oint **T**est **A**ction **G**roup

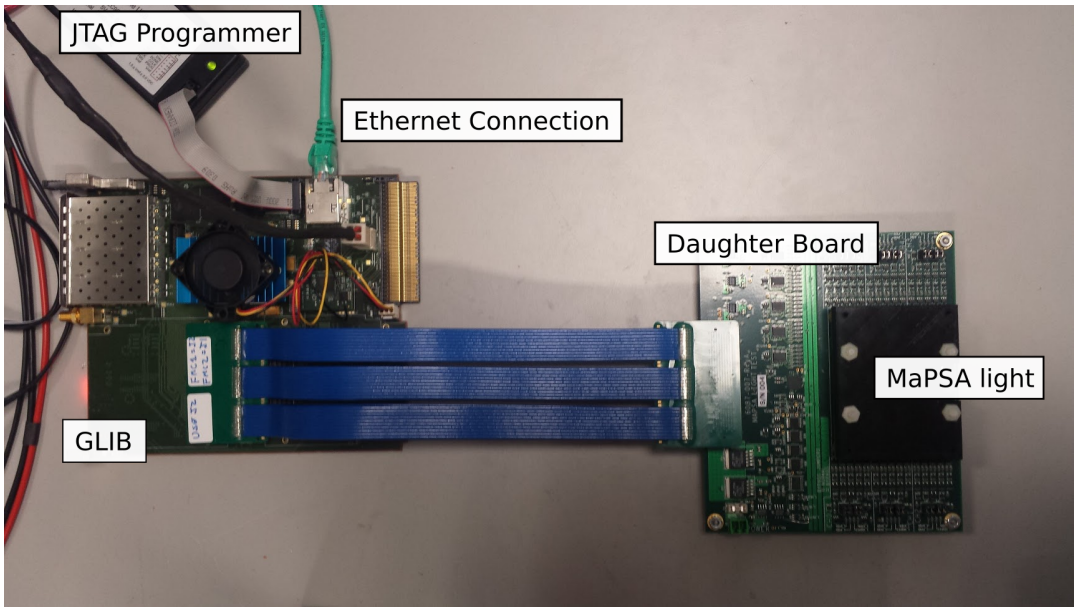


Figure 5.19.: The MaPSA light readout system. The MaPSA light carrier board is covered by a 3D-printed enclosure and is connected to the custom made daughter board. A high pin count FMC to FMC cable (blue) connects the daughter board with the FPGA based Gigabyte Link Interface Board (GLIB), which is controlled by a PC through an ordinary Ethernet connection. A JTAG connector provides the necessary interface to upload custom firmware to the board and adapt the FPGA to the user's needs.

6
Test beam measurements

The previously presented measurements are essential to qualify the sensor material and to determine its electrical properties. These measurements, however, do not provide any information about the performance and especially the efficiency of the sensor and assembly under realistic conditions. Therefore, additional measurements are necessary to fully characterize the small prototype detector and to make a statement about its usability in the CMS detector. Probably the most realistic environments for detector developers are test beam facilities at a particle accelerator. One of these test beam facilities is operated by the Deutsches Elektronen-Synchrotron (DESY) in Hamburg, Germany, which will be presented in the following. The overview of the test beam setup and the description of the analysis also serve as a reference for the beam test of the new PS-p prototype, which will be presented in the Chapter 10 of this thesis.

6.1. The DESY-II Test Beam facility at DESY

The DESY test beam facility operates three beam lines which receive their particles from the DESY-II accelerator, which mainly acts as injector for PETRA-III, a synchrotron radiation source further down the accelerator chain. However, as long as PETRA-III does not require any additional particles (*top-up*), DESY-II is providing beam to the test beam facility closely attached to the storage ring. Since the revolution frequency of DESY-II is fixed to 1 MHz, an almost continuous particle beam is expected in the beam area. The beam generation for the three beam lines is illustrated in figure 6.1.

DESY-II accelerates and decelerates only one bunch of electrons or positrons at a time. The particles are injected at an energy of 450 MeV and subsequently accelerated up to 7 GeV. The bunch is then extracted to PETRA-III, dumped or decelerated down to 450 MeV again. At this point, a new bunch is injected or the remaining bunch gets filled with new particles again to compensate for the losses during the acceleration process. A thin carbon fiber target in the middle of the beam pipe causes some of the electrons or positrons in the bunch to generate bremsstrahlung, which is emitted tangentially to the beam and leaves the beam pipe shortly after. By hitting a second converter target outside the synchrotron, the photons are converted back into electron-positron pairs due to the pair production process. A dipole magnet after the converter target deflects these secondary particles and generates a fan of particles which are sorted by their charge and energy. A collimator cuts-out the desired sign of charge and energy of the particles which then enter the beam area. By adjusting the current of the magnet, the user can choose what kind of particles (electrons or positrons) and with which energy they are passed into the beam area. The maximum particle energy that these secondary particles can achieve is limited to about 6 GeV. The rate at this energy is usually in the order of a few hertz. In order to receive particles at a more reasonable rate of at least several hundred hertz, the particle energy is usually set to 5.6 GeV and below. The drawback of low-energy particles, however, is the fact that the trajectory of these particles tend to be more affected by multiple scattering, which makes analysis more difficult and more importantly, reduces the maximum

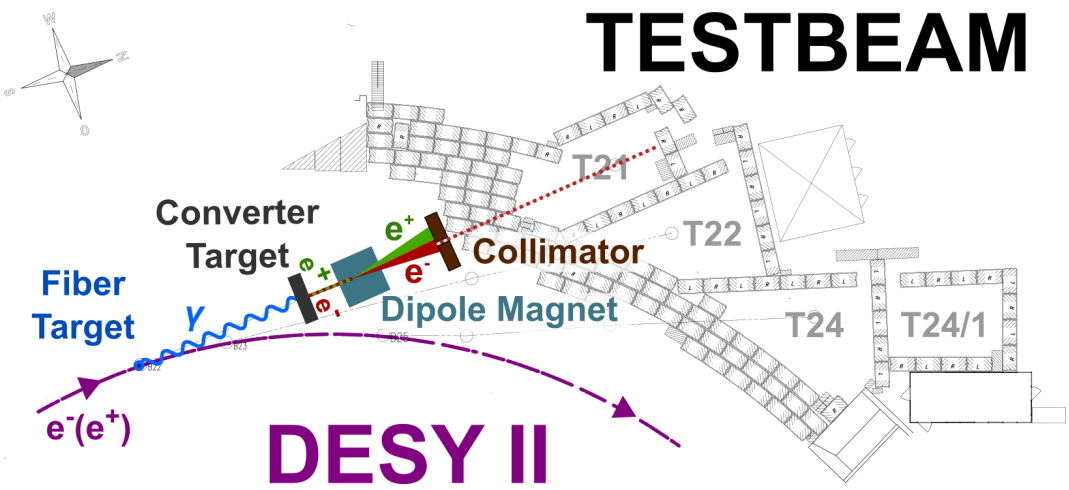


Figure 6.1.: Beam generation at the DESY-II test beam facility. The DESY-II accelerator stores one bunch of electrons (positrons) that passes a carbon fiber target at every revolution. Electrons (positrons) that hit the carbon fiber target generate bremsstrahlung which is converted into electron-positron pairs at a converter target outside the synchrotron. A dipole magnet fans out the resulting particles while a collimator in front of the beam area cuts out the desired particle with a certain energy [Deu18].

achievable resolution of the particle tracks [Deu18]. In the end, a particle energy of 5.6 GeV has turned out to be the optimal sweet spot between a very good track pointing resolution and a decent particle rate.

6.1.1. The EUDET telescope

Precise track reconstruction is essential to determine the performance of the prototype in a test beam environment. Therefore, almost all test beam areas in the world are equipped with a permanently installed tracking device, called a *telescope*, that is offered to the users. At DESY, two out of three beam lines are equipped with a telescope which consists of six identical pixel detectors that are mounted on two movable arms with three planes each. The first three layers, that are mounted on the arm closer to the accelerator, are called *upstream* planes while the planes on the second arm are called *downstream* planes. The prototype, or the **D**evice **U**nder **T**est (DUT), is placed in between these two arms which ensures a good track resolution and simplifies the interpolation of the track impact point during the analysis. Both telescopes are EUDET type telescopes, called DATURA[1] and DURANTA [DES19]. The former is shown in figure 6.2.

EUDET was a project supported by the European Union to promote the research activities of over 30 European institutes towards the next large particle physics project, the **I**nternational **L**inear **C**ollider (ILC). In this context several EUDET-like telescopes, the Data Acquisition software (*EUDAQ*) and the offline analysis framework *EUTelescope* have been developed.

All EUDET telescopes are equipped with six fine-pitch MIMOSA 26 sensors with a size of 21.2 mm × 10.6 mm and a physical thickness of about 50 µm. Each sensor consists of 663 552

[1] **D**ESY **A**dvanced **T**elescope **U**sing **R**eadout **A**cceleration

Figure 6.2.: The DATURA telescope at the DESY test beam. The telescope consists of two arms with three MIMOSA 26 sensor planes each. The three planes closer to the accelerator (right side of the picture) are called upstream planes and the three remaining ones are called downstream planes, respectively [Deu18].

pixels with a size of 18.4 µm × 18.4 µm that are organized in an array of 576 rows and 1152 columns. The very small pixel size and thus excellent intrinsic binary resolution

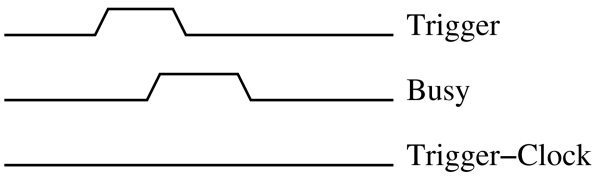
$$\sigma_{\text{binary}} = \frac{d}{\sqrt{12}} \tag{6.1}$$

of 5.3 µm is the most outstanding advantage of the EUDET telescopes which leads to a remarkable track resolution later in the analysis. However, the main drawback of the MIMOSA 26 is its comparably long integration time during one readout cycle. The MIMOSA 26 is read out by a rolling-shutter mechanism, which needs 16 clock cycles of an 80 MHz clock to acquire the data of each individual row of the sensor. This leads to a total integration time of about 115.2 µs per readout cycle. Compared to the detectors used at the LHC, which run at the bunch-crossing rate of 40 MHz, the MIMOSA 26 takes more than 4600 times as long to be read out, making it unsuitable for high rate tests of these systems.

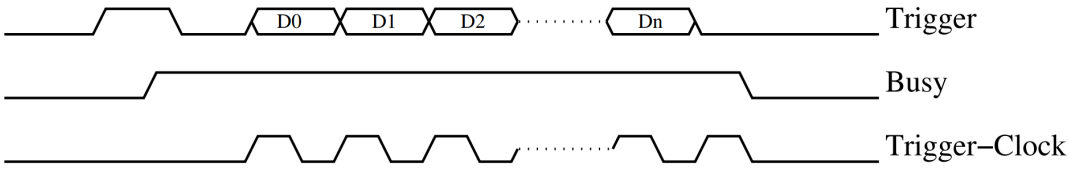
Each plane of the telescope uses the sensor information to generate zero-suppressed hit data that is transmitted to its individual auxiliary board. The auxiliary boards are again connected to the data concentrator board that collects the data from all six planes of the telescope. The concentrated data is then acquired by an FPGA board that deserializes the data streams and subsequently sends it to a National Instrument (NI) PXIe crate based readout system that provides the final data to the data acquisition software [Jan+16].

6.1.2. The Trigger Logic Unit

In order to detect a particle passage and trigger the corresponding event in the data stream, the EUDET-type telescopes are equipped with four sets of a scintillator and a photo multiplier tube (PMT) combination, two of which are mounted in front of and two behind the setup. The signals of the PMTs are used as inputs for a fourfold coincidence logic which is integrated in a dedicated trigger system for the EUDET telescope: the Trigger Logic Unit (TLU). The



(a) Simple handshake



(b) Trigger data handshake

Figure 6.3.: Trigger handshakes between TLU and DAQ systems. In simple handshake mode, the busy line is raised as soon as the trigger arrives at the DAQ system and released when the readout is completed. As long as the busy signal is set to high, no triggers are issued by the TLU. In trigger data handshake mode, the trigger ID is transferred to the DAQ system while the busy line is raised. Therefore, the DAQ system is applying a clock signal to the trigger-clock line while receiving the individual bits on the trigger line [Cus09].

TLU provides additional LEMO and RJ45 connections that are used to distribute the output of the coincidence and trigger logic. One of the RJ45 is already used by the telescope, while the remaining connections can be used to trigger up to four additional setups at the same time. All four connections include a *busy* line that allows each subsystem to suppress the transmission of any further triggers, while it is reading out data and preparing the detector for the next trigger. This ensures that all data streams contain the same number of triggered events and keep synchronized. The TLU can operate in three different of these *handshake* modes: *no-handshake*, *simple handshake* and *trigger data handshake* mode. If the system is operated in no-handshake mode, the busy signal is ignored and the TLU issues a trigger every time a particle traversal is registered by the scintillators and the coincidence logic. In simple handshake, each system is expected to raise the busy line immediately after it receives the trigger signal from the TLU. As soon as the system finishes its readout, it has to release the busy line again and therefore signals the TLU that it is ready for the next trigger. Only if all busy lines are released, the TLU issues new triggers and sends them to the connected systems again. If the TLU is operated in trigger data handshake mode, the DAQ system has to provide an additional Trigger-Clock line that is used as common clock between the two to transfer a *trigger ID* from the TLU to the connected system. Similar to the simple-handshake, the busy line is supposed to be raised by each DAQ system as soon as it receives the trigger from the TLU. However, instead of just releasing the busy line after the readout, the DAQ system is starting to apply a clock signal to the Trigger-Clock line which will initiate the TLU to send out the trigger ID on the trigger line [Cus09]. The simple and trigger data handshake is illustrated in figure 6.3.

6.1.3. The EUDAQ framework

The data acquisition software which is used to read out the telescope at the DESY test beam is a generic multi-platform data acquisition framework, called EUDAQ. The development of EUDAQ started as part of the EUDET project and is now continued as a general project on GitHub.com [Git18]. The framework is split into several *processes* that are using TCP/IP sockets as their communication channel of choice. One of these processes, the *Run Control*, serves as central element for the whole data acquisition procedure and takes care of the initialization, configuration and control of all other processes that register with it. A graphical user interface (GUI) helps the user with these steps and also provides additional information about the current particle and trigger rate. Systems that are able to produce data, like the telescope, have to provide their individual *producer* processors, which connect to the Run Control and send their data streams to a central *Data Collector* that collects the data of the individual producers and writes the combined raw data to disk.

A *Log Collector* and an *Online Monitor* serve as basic monitoring tools to control the status of all DAQ systems, their position in the beam and the synchrony of the data streams during the acquisition phase [EUD16].

6.1.4. The EUTelescope data analysis framework

The generated raw data are the starting point of a complex analysis chain, which should provide detailed information about the performance of the device under test (DUT). The analysis of the DESY test beam data is based on the EUTelescope framework which in turn is embedded in the ILCsoft framework. The ILCsoft software package is developed by the linear collider community and combines several data processing tools for the detector development towards the future linear collider project. The ILCsoft framework is based on the *Linear Collider I/O* (LCIO) data format, the *Geometry API for Reconstruction* (GEAR) markup language, the *Abstract Interface for Data Analysis* (AIDA) and the event processor for *Modular Analysis & Reconstruction for the LINear collider*, called Marlin. The latter is responsible for the execution of several independent sub-routines, called *processors*, which form the actual data analysis chain. Each of these processors can expose certain parameters which can be set in dedicated Extensible Markup Language (XML) files, called *steering files*.

EUTelescope is built on top of this ILCsoft package and provides a collection of Marlin processors and its steering files that are specialized for test beam analyses. All these processors are supposed to be executed consecutively and to store their results in a common LCIO data file for each individual run.

LCIO is an event-based data format, which stores the data of all DAQ systems that is acquired after each trigger under one sequential event number in the file. Each of these events consists of an *event header* and the *event data*. The event header contains general information about detectors in the setup, a timestamp and the run number which is set and increased by EUDAQ at the beginning of every new run. The event data consists of multiple data *collections* that are generated by the individual processors within the analysis chain. Some of these processors require additional information about the telescope geometry, which is defined in an individual GEAR Markup language file. A GEAR file contains all information about the global position of each detector plane, their individual material budget and a detailed description of their sensor geometry, including the number and size of the pixels as well as their orientation in the beam. Figure 6.4 illustrates the most common reconstruction chain for the DESY test beam data that includes the following processing steps:

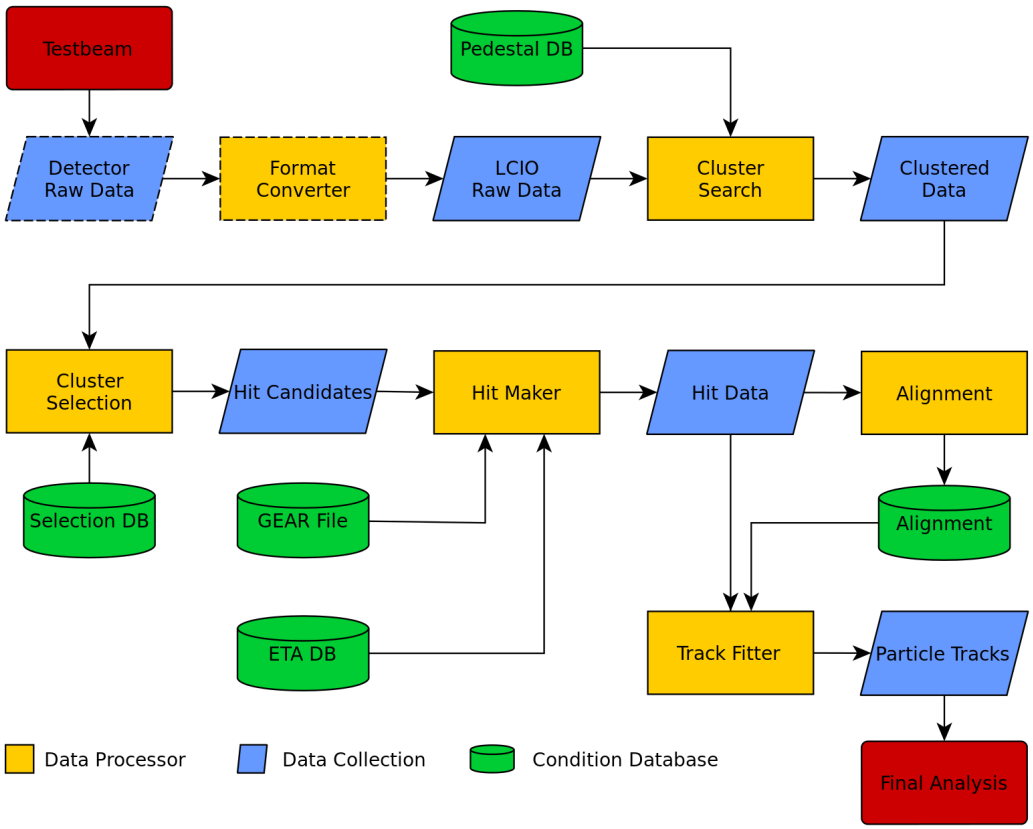


Figure 6.4.: The EUTelescope data analysis framework. The raw data from the test beam is converted into the LCIO file format, which is used for every further step in the analysis. A sequence of processors (yellow boxes) uses the data to generate a set of intermediate data collections (blue rhomboids) and databases (green cylinder) which ultimately lead to the reconstructed particle tracks that are used for the final analysis [DES18].

Format converter

The starting point of the analysis is the conversion of the raw data (TrackerRawData) into the common LCIO file format. Therefore, each DAQ system has to provide its own decoder which is used by the converter processor to generate the individual collections for the LCIO event data block. Typically, these decoders already include zero-suppression, which means that all pixels without any hit information are excluded from the decoded data, which keeps the file size and the processing time as small as possible.

Cluster search and cluster selection

When a particle hits the silicon sensor and generates charge carriers in the bulk, the charge is most likely not collected by a single channel but distributed among several adjacent pixels instead. This effect is called *charge sharing* and leads to *clusters* instead of isolated hits that have to be identified by the clustering algorithm. If the algorithm finds such a cluster in the zero-suppressed data, it determines the *seed pixel* that contains the highest amount of charge of all pixels in the cluster and assigns all neighboring pixels with a signal above a certain threshold to it. At this point also noisy pixels are identified and excluded from the analysis. The processor can now either simply save the coordinate of the seed pixel or calculate the center-of-gravity within the cluster, which increases the resolution compared to the binary resolution given in equation 6.1. Especially at higher incident angles, charge sharing becomes even more pronounced and the clustering even more important.

Hit maker

Until this point, the hit and cluster positions of each plane are given in form of row and column tuples. The *hit maker* transforms these row and column combinations into a three dimensional coordinate system by obtaining the necessary information about the geometry from the corresponding GEAR file and applying the specified transformation to each cluster in the setup. The processor also performs a coarse pre-alignment of the setup which is used as a starting point for the subsequent alignment processor.

Alignment

Despite careful arrangement of the telescope and the other DAQ systems in the beam, the alignment by eye and hand can never achieve the precision that is required for sub-pixel resolution in the micrometer range. For that reason, EUTelescope provides several track based alignment processors that compensate for the misalignment during the offline analysis. All these processors are based on different algorithms that are suitable for one or several test beam facilities and mainly depend on the particle energy and the material budget of the setup. For highly energetic particles at the CERN ($> 120\,\mathrm{GeV}$) [Eng18] and the Fermilab ($< 120\,\mathrm{GeV}$) [Fer18] test beam facility for example, straight line approximations without considering multiple scattering, fit perfectly well to the expected path of the particles through the setup. At the DESY test beam facility and an electron energy of $E < 6\,\mathrm{GeV}$ however, multiple scattering is not negligible anymore. Therefore more complex algorithms had to be developed to describe the particle path with higher accuracy. The most prominent one is the General Broken Line (GBL) algorithm [Kle12]. In order to properly account for multiple scattering of the particles, additional parameters like the particle energy and the scattering material of the setup have to be passed to the algorithm. The GBL algorithm then performs a refit of the initial trajectory, that is defined by the

global hit coordinates (x, y, z) of all detector planes. The resulting fit provides a complete covariance matrix which can be used as input for any kind of fit algorithm. EUTelescope makes use of the Millepede II software package to solve a linear least-squares fit problem with a simultaneous fit of all given parameters [Blo07]. In order to deal with very large numbers of parameters, Millepede II divides the given parameters into two classes, global and local parameters. In case of a track based alignment, local parameters correspond to each individual track and therefore change from event to event. Global parameters on the other hand are fixed for all events within one run and can be identified as the alignment constants of all detector planes. The final alignment corrections are saved in a dedicated database or immediately applied on the initial alignment by editing the corresponding values in the given GEAR file.

Track Fitter

The final step of the analysis starts with the adjustment of the individual hits with the corrections of the alignment processor. This can be achieved by two approaches: either the hit maker is executed with the updated GEAR file once again or the already existing hits are updated with the alignment corrections that have been stored in a database file. No matter which approach is used, the results are fully aligned hits in 3D space. Similar to the preceding alignment processor, also the *track fitter* can use different algorithms to finally reconstruct the tracks in the telescope. Again, GBL is one of these options which is often used in combination with DESY test beam data. When a track is reconstructed, the track fitter starts to interpolate an imaginary hit to the DUT position and stores it in an output file. The final output file marks the end of the telescope reconstruction, but at the same time also marks the starting point of the user analysis, which can either run as an additional EUTelescope processor or as an independent analysis outside the framework.

More information about the EUTelescope framework and its processors can be found in [DES18].

6.2. The MaPSA light beam test

The DESY test beam facility was used to perform first test beam measurements of the MaPSA light in Europe. The main objective of this beam test was to obtain information about the efficiency of the PS-p light sensor in order to evaluate and verify the layout for the design of its full-size successor. The time slot and telescope were shared with collaborators from the Institute of High Energy Physics (HEPHY) in Vienna, Austria, who began their investigation of the inverted MaPSA as a possible solution for a flipped design of the final macro pixel subassembly. The following section briefly introduces the setup as well as the readout and trigger chain that is used for efficiency measurements of the PS-p light at the DESY test beam facility in Hamburg, Germany. A more detailed discussion of the MaPSA light beam test, including the the data acquisition software, the analysis framework and the final results can be found in the master thesis of Gregor Vollmer [Vol17].

6.2.1. The MaPSA light test beam setup

The MaPSA light (inverted MaPSA) setup is mounted on (behind) the DATURA telescope frame which is shown in figure 6.5. The whole MaPSA light setup (GLIB, daughter board and MaPSA light carrier board) is mounted on a carbon fiber carrier plate that is installed upright between the two telescope arms to achieve the best possible track resolution for the

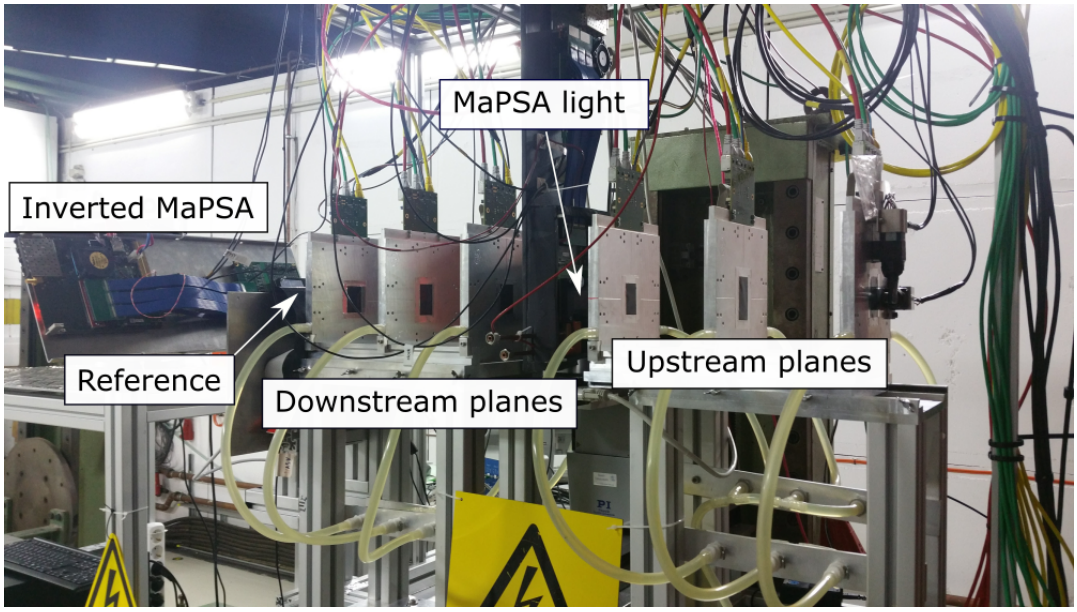


Figure 6.5.: The MaPSA light test beam setup. The MaPSA light setup, mounted on a carbon fiber plate, is placed on three movable stages between the telescope arms. The timing reference is mounted on the telescope frame right behind the last plane of the downstream arm. The inverted MaPSA setup is placed on a separate table behind the telescope.

analysis. The setup is screwed on two linear stages that make it possible to move the assembly in two directions (x and y) perpendicular to the beam axis (z) and thus remotely align the assembly in the telescope with an accuracy of a few micrometers. An additional rotation stage enables the possibility to perform rotational scans of the assembly and thus simulating different incident angles of particles and hence different positions of the sensor in the final detector. A timing reference detector (REF) right behind the last plane of telescope is necessary to deal with the long integration time of the MIMOSA26 planes. In case of the MaPSA light beam test, a single chip assembly of the CMS Pixel Phase-I Upgrade detector with an active area of about $1\,\text{cm} \times 1\,\text{cm}$ was utilized for this purpose. The detector consists of 52×80 pixels with a cell size of $100\,\mu\text{m} \times 150\,\mu\text{m}$ that are read out at the LHC bunch crossing rate of 40 MHz. Since this matches the acquisition rate of the MPA-Light, it is most likely that both systems are only detecting the triggered particle and only a few more that might arrive in the same clock cycle. Therefore, the timing reference can be used to identify tracks in the telescope with correct timing of the DUT. Only those tracks are considered in the final analysis, while all other particles that pass the telescope during its 115.2 µs long integration time are rejected. The CMS Pixel detector is read out by the Digital Test Board (DTB) which offers an external clock and trigger input. Since the readout of the CMS Pixel detector is quite fast compared to the telescope and the MaPSA light, no busy signal is necessary to perform the handshake with the TLU. More information about the CMS Pixel Phase-I Upgrade detector can be found in the work of Simon Spannagel [Spa16].

The test beam setup is supplemented by the hardware of the inverted MaPSA which is placed on another table at the end of the telescope. However, the following sections will focus exclusively on the MaPSA light setup.

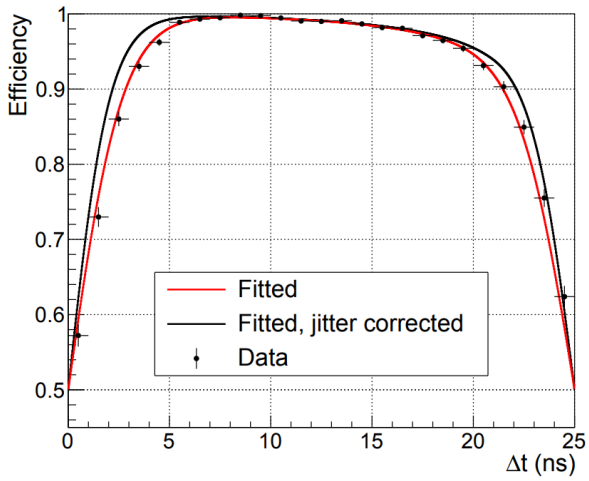


Figure 6.6.: The MPA-light hit efficiency as a function of the phase difference between the particle arrival and the 40 MHz clock of the MPA-Light. The red curve represents the fit to the data points while the black curve shows the jitter corrected efficiency distribution. The timing jitter is introduced by the difference in frequency of the beam clock and MPA-Light clock [CMS18].

6.2.2. The MPA-Light readout

The MPA-Light offers two different readout modes that can be used to acquire the binary output of each individual pixel front-end: the asynchronous and synchronous mode. While the asynchronous mode is mainly used for calibration and testing purposes the synchronous mode is more dedicated to triggered readout and data acquisition in general. Especially at higher rates when multiple particles can hit the detector during one clock cycle, simply counting hits in each pixel cell, as it is done during the asynchronous readout, is no longer sufficient. However, the fact that the expected rate at the DESY test beam is hardly exceeding 1 kHz at the desired particle energy of 5 GeV to 6 GeV, no major difference between the two readout modes should be noticeable. Test beam measurements at the FNAL test beam facility, however, revealed that the hit efficiency of the MaPSA-light in synchronous mode depends on the phase difference between the particle arrival and the 40 MHz clock edge of the chip (shown in figure 6.6). The arrival of the particle is determined by the beam clock of the accelerator. Due to the different frequencies of the accelerator clock and the MPA-Light clock, timing jitter is introduced to the measurement which has to be taken into account during the analysis. Running in asynchronous mode circumvents this chip feature and therefore provides a more undistorted measurement of the sensor performance. In addition, by concentrating on the asynchronous readout mode, the adaption of the GLIB firmware for the trigger logic at the DESY test beam could be reduced to a minimum. The main changes that have been implemented include the support of an external trigger input and a busy output. With those changes, the MPA-Light readout is fully compatible with the TLU running in simple handshake with the setup. Figure 6.7 illustrates the final trigger logic of the MaPSA light setup at the DESY test beam.

When a particle arrives, the PMTs fire and the TLU issues a trigger that is sent to all connected DAQ systems. Each system thereupon raises its busy line and prevents the TLU from sending further triggers. The MPA-Light uses this trigger signal to close its shutter and start transmitting its ripple counter data, which takes about 500 µs to complete. As soon as the MPA-Light is read out and ready to receive the next trigger, the shutter is opened again.

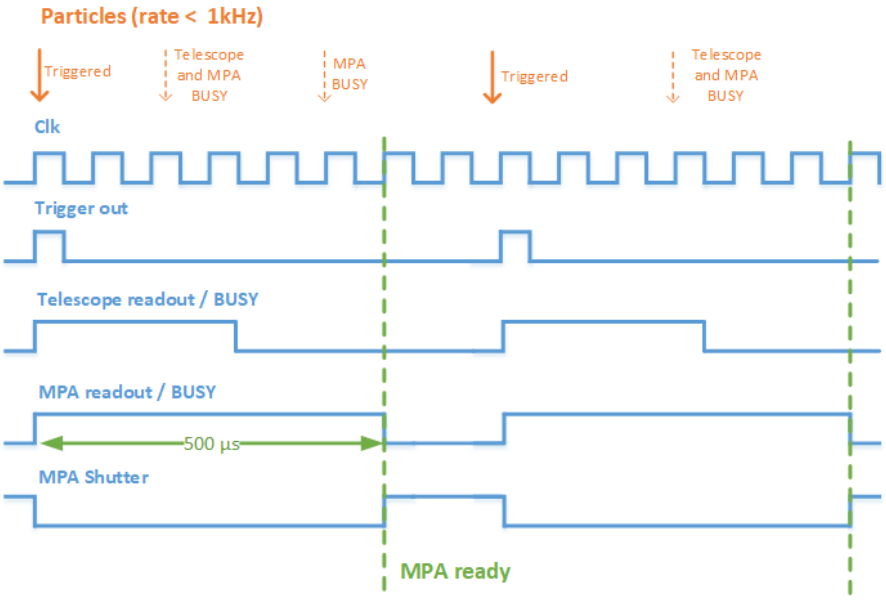


Figure 6.7.: Trigger logic at the MaPSA light test beam. When a particle arrives (orange arrow) and all busy lines are set to low, the TLU issues a trigger and sends it to the connected systems. As soon as the trigger is registered by the MaPSA readout, the MPA-Light closes its shutter and simultaneously raises the busy line and starts its readout. After the readout has been completed, the shutter is opened again and the busy line is released.

In order to provide a busy signal for the simple handshake of the TLU, the inverted state of the MPA shutter is used and connected to the busy line.

The MaPSA light readout is not included in the EUDAQ framework, but is operated as a standalone system that saves its data locally and not in the global binary file of the data collector. Synchronization of the individual data streams is still ensured by the simple handshake with the TLU. Unfortunately, occasional event skipping in one or all of the data streams was observed during the acquisition phase which had to be taken into account during the analysis. The reason for this event skipping and the subsequent shift of data streams is most likely related to a problem in the trigger system of the TLU that could not be solved at that time.

Since the CMS Pixel timing reference shows noticeable efficiency variations during a 25 ns clock cycle, one of the PMTs is set in coincidence with a 7 ns *gate* signal, which is driven by the global 40 MHz clock. This makes it possible to cut out the most efficient clock phase for the reference plane and to use the resulting signal as one of the PMT inputs of the TLU. The final readout schematics is illustrated in figure 6.8.

6.2.3. MaPSA Light analysis

In order to accommodate for the independent data streams of the telescope and the MPA, a slightly modified analysis chain compared to the one introduced in Section 6.1.4 is used for the MaPSA light test beam data. Instead of processing all data in EUTelescope, only the telescope and reference plane data are passed through the previously introduced analysis steps. In case of the MaPSA light beam test, the EUTelescope analysis ended with a second call of the hit maker processor which used an updated GEAR description to generate the aligned hits in the global reference frame. At this point, a new *MapsaDataMerger* processor is introduced to the analysis chain which extracts all hits from the LCIO file, decodes the MaPSA data and

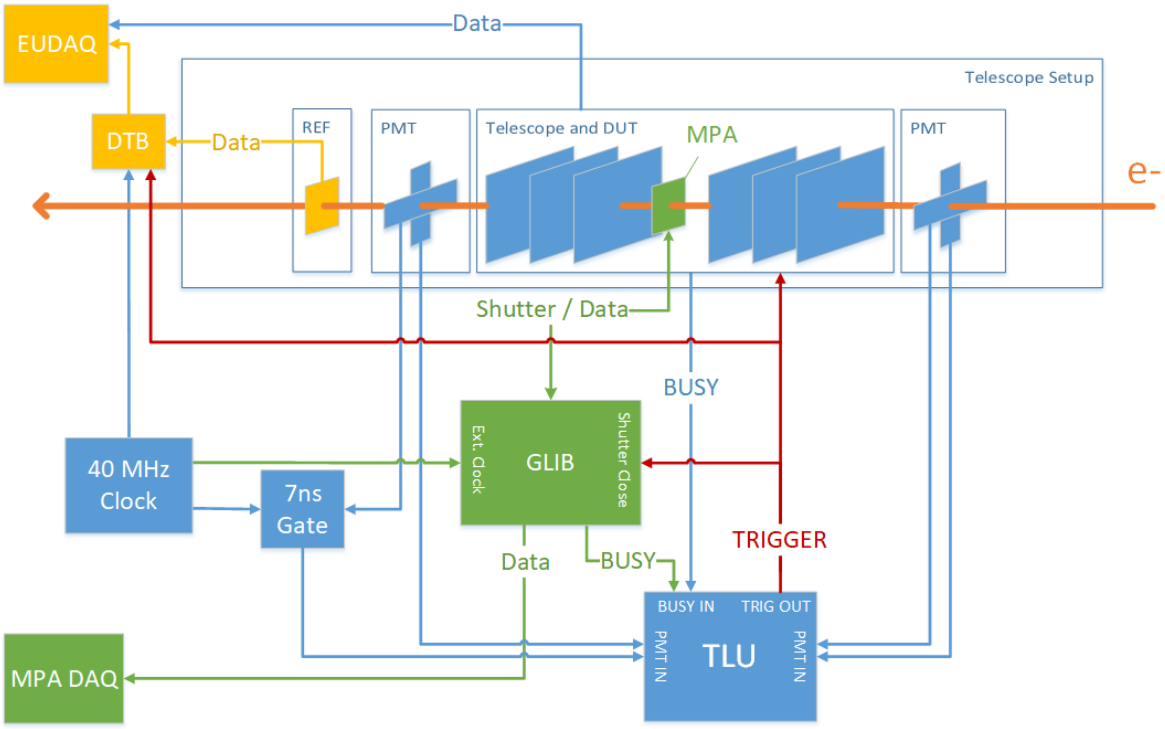


Figure 6.8.: The MaPSA light test beam readout and trigger schematics. One of the PMTs of the telescope is set in coincidence with a 7 ns gate to maximize the efficiency of the CMS Pixel timing reference (REF). The MaPSA light (green) stores its data locally and is not connected to EUDAQ which collects the data of the telescope (blue) and the reference plane (yellow).

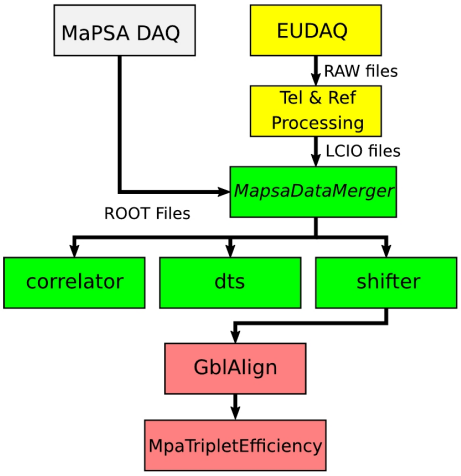


Figure 6.9.: Modified MaPSA light analysis chain. The telescope and reference raw data are still processed by the EUTelescope framework (yellow) and stored in the LCIO file format. The subsequent MapsaDataMerger extracts all necessary data from these LCIO files and combines it with the MaPSA data (gray) in a common ROOT output file. The resulting ROOT file is then passed to the data quality analysis (green) which re-synchronizes any shifted data streams and prepares it for final alignment and efficiency analysis (red) [Vol17].

saves them in a common ROOT[2] data file. The reason to switch from LCIO to ROOT was the unstable state of EUTelescope at that point of time, which resulted in noticeable problems with some processors of the framework. Especially the alignment and track finder processor were severely affected by this problem and would have required a major overhaul to process the MPA data as well. Fortunately, the alignment processor was still able to align the telescope plane without major effort but left the reference plane unaligned.

For that reason, the two final processing steps, the alignment of the DUT and the REF as well as the track finding algorithm, were re-implemented as an independent software package written in C++ on top of ROOT and the Eigen3 template library for linear algebra [Tux18]. The modified MaPSA light analysis chain is illustrated in figure 6.9.

The ROOT output file of the MapsaDataMerger is the starting point for a variety of analyses that are performed sequentially and in parallel. This includes a *correlator*, a *detailed time shift (dts)* analyzer and a data stream *shifter*, that are necessary to deal with the event skipping that occurred during almost all runs of the MaPSA light beam test.

Correlator

Due to the independent data streams of the telescope and the MPA, the EUDAQ Online Monitor can only provide information about the telescope and the reference plane. For that reason an additional correlator is added to the analysis that combines the data of both systems and generates all necessary plots that are consulted for the DQM. Especially correlation plots, in which the hit coordinates of two independent detector planes are plotted against each other, are the most useful representation of data stream synchronization during the acquisition.

[2]The ROOT data analysis framework is a modular scientific software toolkit, developed at CERN [CER18c]

Detailed Time Shifts (dts)

Data synchronization was never assured during the MaPSA light beam test due to problems in the trigger system. Therefore the detailed time shifts (dts) analysis is introduced that extends the correlation plots of the correlator by correlation-vs-time plots for various different event shifts between the data streams. This is especially useful to find the exact event at which synchronization is lost and to determine the new shifts for the remaining data.

Shifter

The shifter finally reads the initial ROOT file and applies a constant index shifting to the data streams which results in a perfectly synchronized output ROOT file that is ready for the final analysis.

GblAlign

GblAlign is the first step in the custom analysis framework. It uses the General Broken Lines (GBL) and Millepede-II algorithm to align the DUT and the reference plane in the global coordinate system, similarly to the alignment processor of the EUTelescope framework.

MpaTripletEfficiency

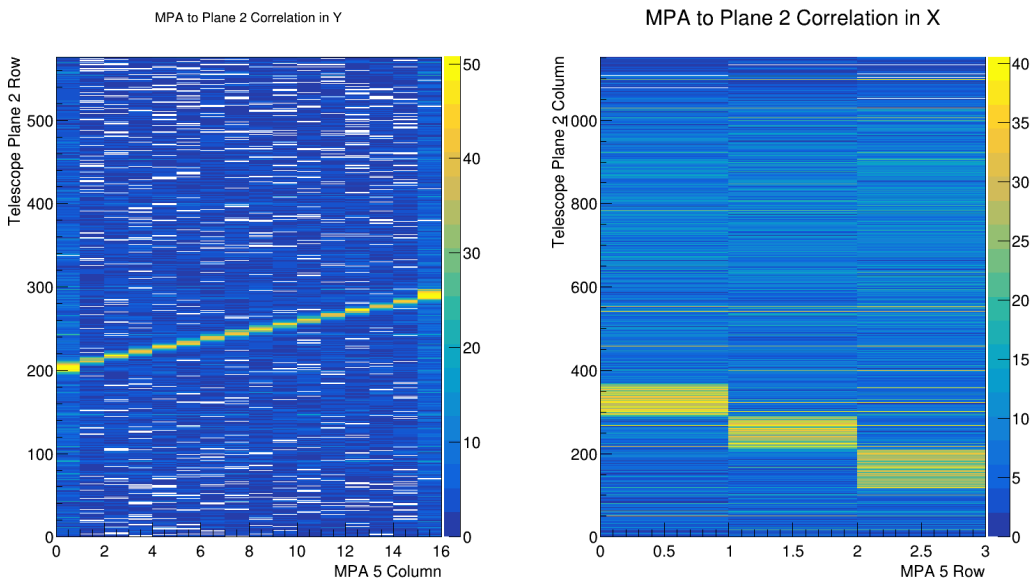
The MpaTripletEfficiency step performs two task at once: first, it reconstructs the particle tracks, using a simple *triplet matching* approach and second, it performs the final efficiency analysis of the MaPSA light. For the triplet matching algorithm, the particle track is split into an upstream and a downstream part that refer to the corresponding up- and downstream arm of the telescope. The algorithm is based on a linear extrapolation between the hits of the first and third plane and a subsequent cut on the maximal distance (*residual*) between the measured and extrapolated hit on the second plane of each arm:

$$\text{Residual} = \vec{x}_{\text{meas}} - \vec{x}_{\text{track}}. \tag{6.2}$$

The resulting downstream triplets are then extrapolated to the reference plane in order to perform the timing cut by rejecting triplets without a matching reference hit. For the final track matching all remaining downstream triplets with a reference hit and all upstream triplets are extrapolated to the DUT position in the middle of the telescope and again cut on the distance between the two extrapolated hits. Only the extrapolated hits of the matched upstream triplets are then used for the efficiency analysis. The efficiency of the detector is defined as the number of reconstructed tracks with a DUT hit divided by the total number of extrapolated tracks

$$\text{Efficiency} = \frac{\text{Tracks with DUT and REF hit}}{\text{Tracks with REF hit}}. \tag{6.3}$$

In practice, the efficiency is obtained by extrapolating the upstream triplet onto the DUT plane and looking for a DUT hit within a user-defined proximity to the extrapolated hit. If at least one hit is detected, the module is considered efficient at the coordinate of the extrapolated hit. Plotting the results on a two-dimensional histogram will ultimately lead to the desired efficiency map of the detector.



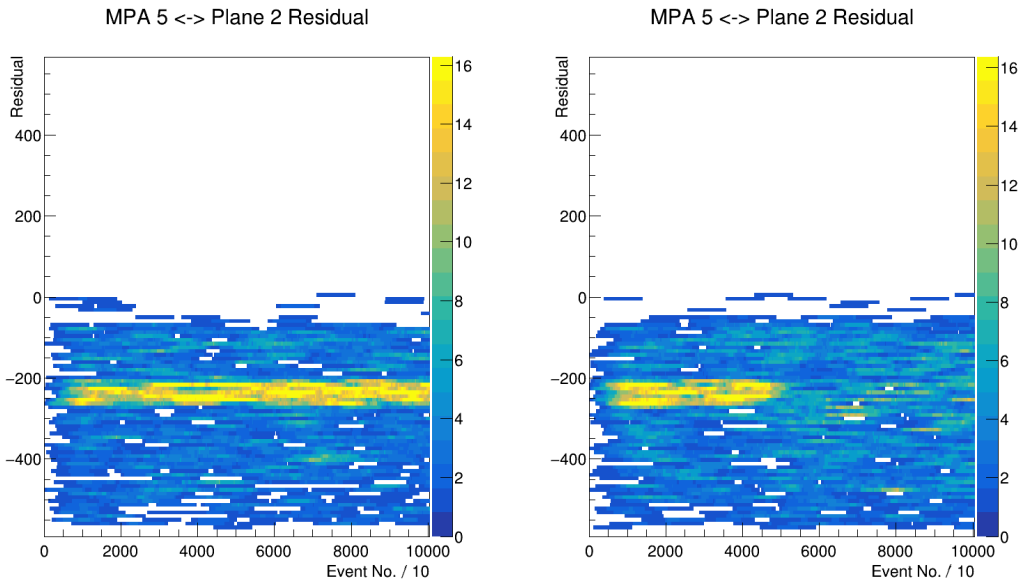
(a) **(b)**

Figure 6.10.: Correlation between MPA 5 and the last upstream plane (Plane 2) of the telescope. The two systems are mounted at an angle of 90° towards each other, leading to correlation between MPA columns and telescope rows and vice versa. Correlated hits are clearly recognizable as bin entries along a straight line (yellow) through the plot.

6.2.4. Correlation and time shifts

Correlation plots during data taking can serve multiple purposes during a beam test. Even before the actual measurement program is conducted, correlation plots are consulted as the most helpful tool for the spatial alignment of the DUT and the reference plane in the telescope. Only if all subsystems are well aligned towards each other, the acceptance and therefore the overlap of the sensitive area is maximized. A high acceptance is essential when it comes to the time it takes to take a certain number of events with tracks in all subsystems. Since the DUT and the reference plane are comparably small against the telescope acceptance window (including the scintillators), the overlap of the two systems together with the efficiency of the reference plane is the main driving factor of the maximum achievable acceptance in the setup. With an active area of roughly 66 mm^2 and assuming full efficiency within the correct clock phase, the CMS pixel reference can reach a maximum acceptance of about 29 %. This means that less than a third of the triggered events actually contain a necessary reference hit for the analysis. Since the MaPSA light with two MPA-Lights bump bonded to the sensor only covers an active area of about 15.6 mm^2, the maximum achievable acceptance of the whole system assuming a uniform hit distribution on the sensor is about 7 %. For a detailed efficiency analysis, the target number of tracks in all subsystems was chosen to be around 300 000. Thus, about 4 300 000 events had to be recorded in order to reach the desired target number of tracks.

Two exemplary correlation plots between one of the two MPA chips (MPA 5) and the closest telescope upstream plane (Plane 2) are shown in figure 6.10. The uniform blue background is generated by random combinations of all registered hits in both planes. In contrast, hits that are generated by a traversing particle have a fixed correlation between their respective hit coordinates and thus lead to higher counts in these bins of the two dimensional histogram which is shown here. A good spatial overlap of the subsystems is given when all possible correlating



(a) (b)

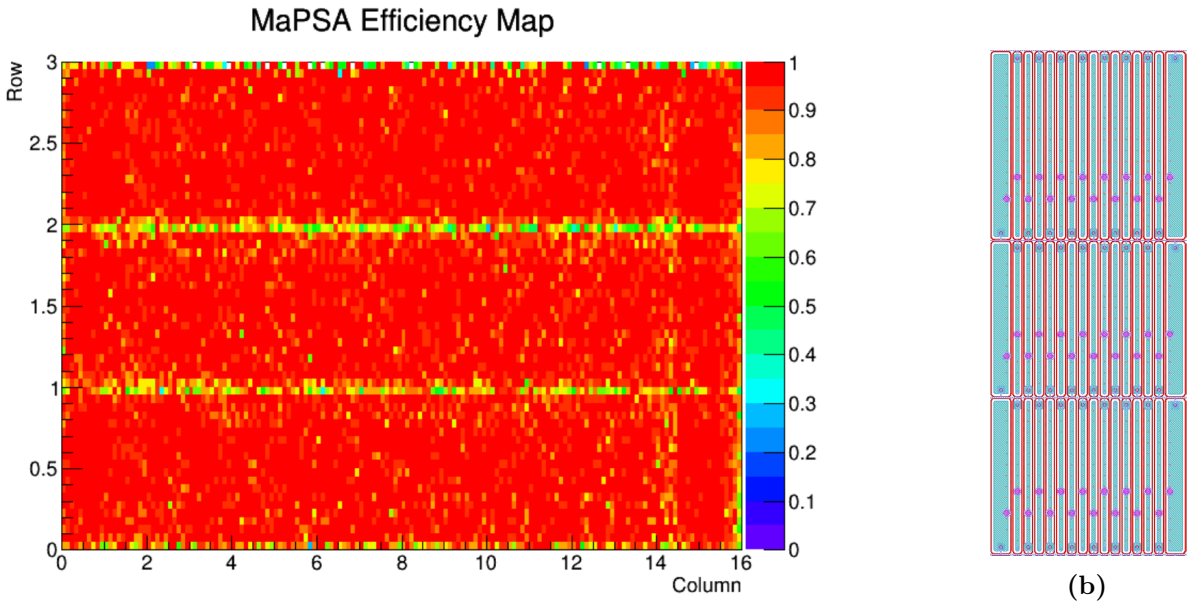
Figure 6.11.: Correlation between MPA 5 and the last upstream plane (Plane 2) over the event number. Figure 6.11a shows perfect correlation of the two systems until the end of the run. In figure 6.11b on the other hand a clear sync loss of the data streams is recognizable after approximately 50 000 events.

hit combinations are visible in the plot. Since the MaPSA light is mounted at an angle of 90° with respect to the telescope planes, the MPA rows are correlated with the telescope columns rather than their rows and vice versa. Positive or negative slopes of the visible diagonals are related to the arbitrary definition of the point of origin in the respective pixel matrix. This distinctive correlation can only be seen if the data streams of the two systems are synchronized. If the data streams are not synchronous, only random hit combinations and no straight line is visible in the plot. Therefore, correlation plots also provide valuable information about the data synchrony and are very useful during the setup and debug phase of a beam test. However, event skipping and shifts between the data streams are hardly noticeable since this is only implied by a slowly fading correlation line caused by the increasing number of random hit combinations.

To solve this problem, the detailed time shift (dts) analysis introduces the correlation-vs-time plot which is shown in figure 6.11. The plot shows the residual between the MPA Light and the telescope hits, calculated for a certain number of events, over the event number itself. While figure 6.11a shows perfect correlation between the two systems until the end of the run, figure 6.11b clearly indicates a sync loss after about 50 000 events of that run. By manually shifting the data streams and detecting the new shift index, the data stream can be synchronized by the shifter afterwards. Since these data shifts occur randomly in time, the number of events per run was usually limited to 100 000 events in order to avoid multiple index shifting of the data streams during one single run.

6.2.5. Efficiency of the MaPSA light

The synchronized data output streams of the shifter are subsequently passed to the re-implemented alignment processors which again use GBL and Millepede-II to align the DUT and the CMS reference pixel detector in the global coordinate system. Finally, the MpaTriplet-



(a) (b)

Figure 6.12.: Efficiency map of the PS-p light read out by one of the two bump bonded MPAs (a). Almost all parts of the observed area are fully efficient. Only in the region between the individual pixel rows the efficiency can drop to about 60 % which can be traced back to the aluminum bias rails that are running across the pixel matrix (b).

Efficiency uses the aligned hits for triplet matching and performs the final efficiency analysis. Figure 6.12 shows one example of the final two dimensional efficiency map of one MPA bump bonded to a PS-p light with a standard layout at perpendicular incidence of the particle. The efficiency of the MaPSA light is almost constantly reaching 100 % across the whole connected part of the sensor. However, quite severe inefficiencies between the individual pixel rows are still visible. Consulting the design of the PS-p light in his standard configuration, illustrated in figure 5.8, leads to the conclusion that this area matches the position of the bias rails which are running horizontally through the pixel matrix. Since the pixels are quite long compared to the bias rails, these edge effects can only lead to a global efficiency loss of a few percent. In addition, as soon as the sample is rotated, the effects become even more negligible. Nevertheless, the question arises whether this kind of inefficiency can be avoided by simple design changes to the bias rail region. Especially the PS modules in the central part of the barrel region could benefit from the increased efficiency. Furthermore, effects after irradiation have not yet been taken into account, which could decrease the efficiency at the bias rail region even further. For these reasons, a detailed simulation study is conducted that provides deeper insight into the charge collection process below the bias rail. The results of these simulations are used to develop a suitable solution to increase the efficiency of the final PS-p sensor.

7

TCAD simulations of bias rail implementations

The MaPSA light test beam measurements revealed that the bias rail region between the individual pixel rows of the PS-p light lead to undesirable inefficiencies at perpendicular incidence of particles. To address this problem, detailed Technology Computer Aided Design (TCAD) simulations are conducted to gain deeper insight into the processes inside the silicon sensor and to develop an optimized design for the final semiconductor device. These TCAD simulations are based on finite element simulations and numerical solutions of several differential equations on a discrete and regular mesh that is spread throughout the entire device. For this particular study, the Sentaurus TCAD software suite from Synopsys is used. The Sentaurus TCAD package provides a collection of software tools that are necessary to simulate the fabrication, operation and reliability of semiconductor devices [Syn18b]. In case of silicon sensors, the software suite is used to reproduce their electrical properties, determine the electric field distribution and to simulate the drift of charge carriers along the electric field lines. All these simulations provide valuable information to predict the performance of the device. In the following chapter the Sentaurus TCAD simulation package along with its workflow and necessary input is introduced. The investigated device geometries and the simulation techniques are presented. Finally, the results of the individual simulations, which serve as input for the final PS-p design process later in this work, are presented and discussed in detail. In contrast to similar studies conducted within the ATLAS collaboration [Unn+16], the conclusion is based on the maximum electric field in the bulk and the charge collection efficiency of the device.

The results of this study have been presented at the 11th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors (HSTD) in Japan [SD19].

7.1. Technology Computer Aided Design

The Sentaurus TCAD package contains multiple simulation tools that are executed sequentially. A typical TCAD simulation workflow is sketched in figure 7.1. The first step of every simulation is the definition of the device geometry. The corresponding instructions to generate these devices are defined in TCL-based script files (*command_dvs.cmd*). Small variations such as the doping concentration or the thickness of the bulk can be defined as different parameter sets of the same device in the *boundary_fps.tdr* file or the graphical user interface. The script alongside the parameter set are passed to the Sentaurus Structure Editor (SDE) which generates the final geometry file and the corresponding mesh file (*grid_mesh.tdr*). These mesh files include thousands or even millions of so-called *mesh points* at which all equations of the regarded physics models are solved numerically. As soon as these equations have converged at all these mesh points, a stable state has been found and the simulation concludes. The accuracy of these results depends on the number of mesh points in the device. As a general rule of thumb, the higher the granularity of the mesh, the higher the accuracy of the results in the end. However, more mesh points also imply that the equations have to be solved more often and therefore more computing power and time are needed to complete the simulation. For that reason, SDE

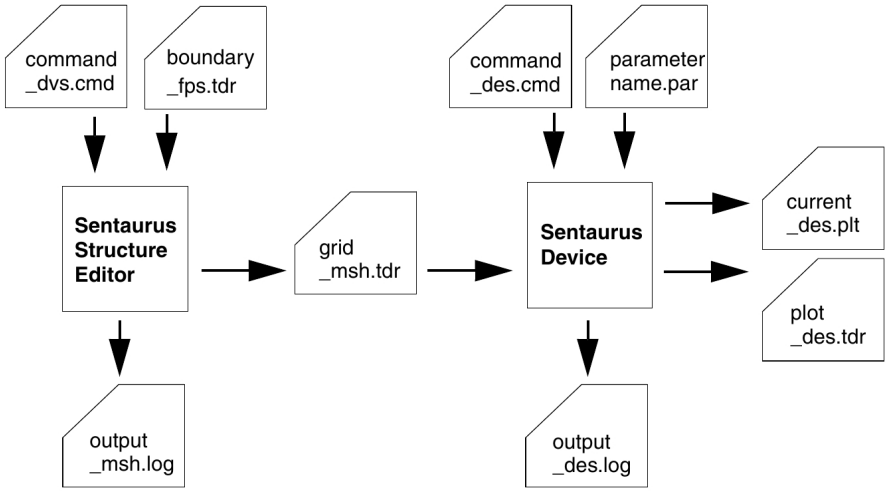


Figure 7.1.: The Sentaurus TCAD workflow. The Sentaurus Device Editor takes the geometry files and generates the corresponding mesh file for the device simulation. The mesh file is passed to the Sentaurus Device simulator, which again loads certain script files with all necessary physics models and the desired simulation instructions. The simulation results are stored in two different output files that serve as input for the final analysis [Syn18a].

tries to distribute the mesh points in an intelligent way. While the mesh is coarser in the bulk region, where the doping profile and the electric field are uniform, the mesh becomes more dense in the transition region between the bulk and the implants at the frontside. This approach provides a reasonable balance between the required computing time (coarse mesh in the bulk) and accuracy (dense mesh at the frontside) of the results.

The subsequent Sentaurus Structure Simulation tool (SDevice) takes these mesh files and loads a user defined *command_des.cmd* script file and performs the actual device simulation. Similar to the SDE, small parameter variations, defined in a *parameter_name.par* file can be passed to the tool as well. In order to determine the electrostatic potential and therefore the electrical properties of the device, the Poisson and continuity equation have to be solved during this step. The Poisson equation as defined in the Sentaurus TCAD package is given in the form of

$$\nabla \cdot \left(\epsilon \nabla \phi + \vec{P}\right) = -q\left(p - n + N_D - N_A\right) \tag{7.1}$$

with the electrical permittivity ϵ, the polarization vector $\vec{P}$, the elementary charge q, the electron and hole density n and p as well as the concentration of the ionized donors and acceptors N_D and N_A, respectively. The continuity equation, which ensures charge conservation in the device, is expressed as

$$\nabla \cdot \vec{J}_n = q\left(R_n - G_n\right) + q\frac{\partial n}{\partial t}, \qquad -\nabla \cdot \vec{J}_p = q\left(R_p - G_p\right) + q\frac{\partial p}{\partial t}, \tag{7.2}$$

where $R_{n/p}$ and $G_{n/p}$ denote the recombination and generation rate of electrons and holes, $\vec{J}_{n/p}$ the respective current density and $\frac{\partial n/p}{\partial t}$ the change of the charge carrier density over time. Both differential equations are solved numerically and iteratively at every mesh point until the error drops below a user defined break condition. The final numerical results of all mesh points are stored in *_des.plt* and *_des.tdr* files, which serve as input for the final analysis.

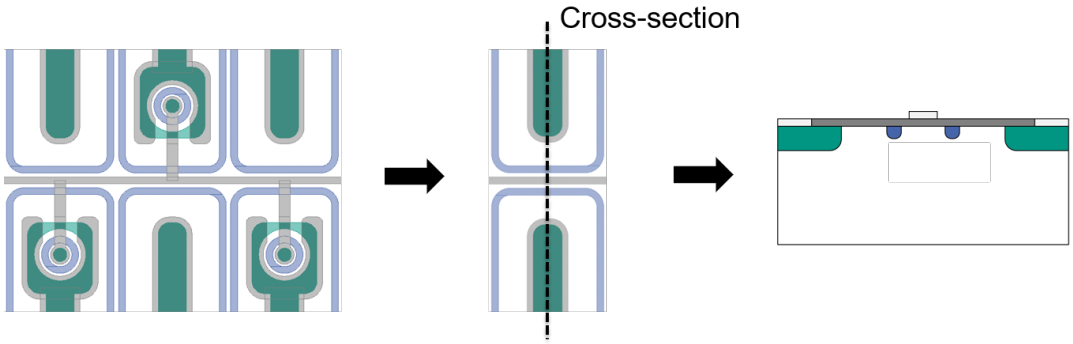


Figure 7.2.: Generation of the device geometry for the simulation. The initial PS-p light geometry is simplified by omitting the punch-through structure and only considering two adjoining pixel cells. In order to reduce the mesh size and computing time, only a two dimensional simulation is performed.

The Poisson and continuity equation are the two most basic equations that have to be solved during the device simulation. However, Sentaurus TCAD offers a wide variety of additional physics models that have to be applied to describe the effects in the device more properly [Syn18b]. An exemplary command file of the Sentaurus Device Simulation tool including all physics models used for this study can be found in Appendix A.

7.2. The device geometry

Implementing a very detailed representation of the device geometry in the simulation framework is essential to obtain accurate results to reproduce and predict the performance of the device. However, the more detailed and larger the device, the more mesh points and thus more computing time are required to ensure the desired accuracy. Since most silicon sensors feature a high degree of symmetry, two-dimensional simulations are the perfect choice to reduce the number of mesh points to a reasonable amount. If the geometry is confined to a small area of interest, the number of mesh points can be reduced even further. The final geometry that is used in this simulation study is based on a 200 µm thick n-in-p type sensor, very similar to the PS-p light sensor in its standard design variation which was investigated at the DESY test beam. In order to simplify the problem even further, the alternating punch-through structure is omitted. The process of generating the default device geometry is illustrated in figure 7.2.

The base design consists of two pixel implants with an implantation depth of 1.5 µm and a peak concentration of $10^{19}\,\mathrm{cm}^{-3}$ that are separated by a gap of 75 µm. Each pixel is isolated by an individual p-stop ring with a width of 6 µm and an implantation depth of 1.5 µm. A p-stop doping concentration of $10^{16}\,\mathrm{cm}^{-3}$ has been proven to be the "sweet-spot" between high inter-pixel resistance, ensuring proper pixel isolation, and early breakdowns of the sensor due to high electric field strengths [Pri16]. The distance between two neighboring p-stop rings is set to a default value of 13 µm, which matches the PS-p light layout. The bulk doping concentration is set to $10^{12}\,\mathrm{cm}^{-3}$, a good starting point for almost all silicon sensors based on high resistivity bulk material and a full depletion voltage of 100 V to 150 V. A uniform p^+ implantation with a peak concentration of $10^{19}\,\mathrm{cm}^{-3}$ at the backside ensures an ohmic contact between the bulk and an additional aluminum layer that serves as the electrical contact of the device. The oxide trapped charge Q_{ox} in the 1 µm thick silicon dioxide layer on top of the implants and between the aluminum vias at the frontside is set to $1 \times 10^{11}\,\mathrm{cm}^{-2}$, an empirical value that fits well for unirradiated devices that have been produced at Hamamatsu K.K. in Japan [Har17]. The 6 µm

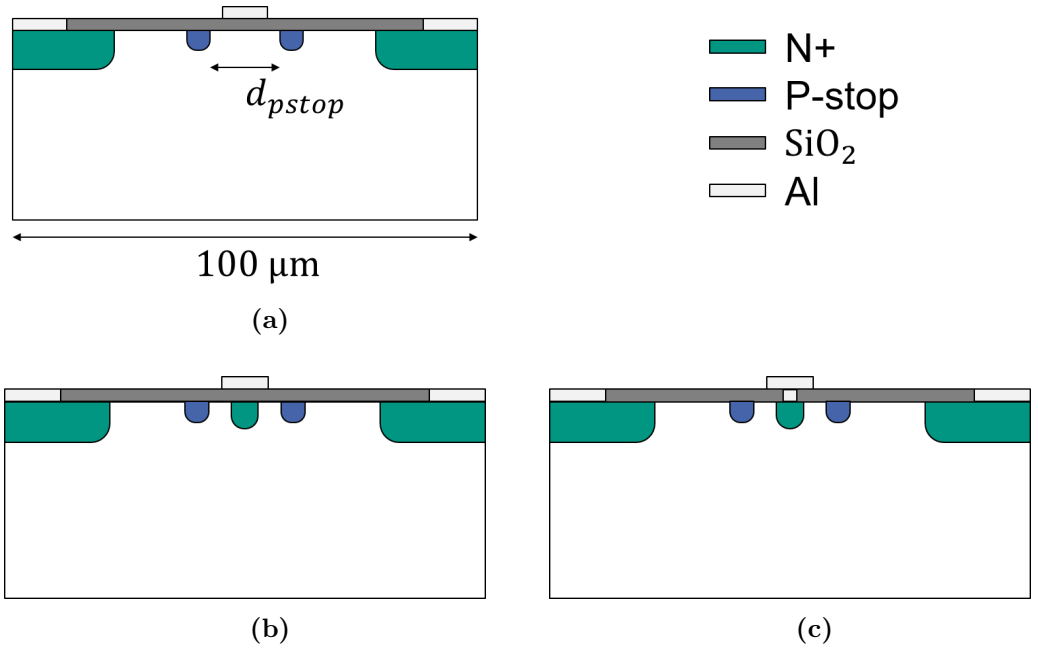


Figure 7.3.: Cross-sections of three bias rail geometries used during the simulation. Three different approaches are investigated: the reference design, which only includes a grounded aluminum rail on top of the silicon dioxide (7.3a), one design with a floating n-doped implant below the aluminum rail (7.3b) and a sensor with a connected implant which is set to ground potential by the aluminum rail (7.3c).

wide aluminum bias rail runs exactly in the middle between the two pixel implants on top of the silicon dioxide layer. All following design variations are based on this base layout.

7.2.1. Bias rail implementations

During this study three different bias rail approaches have been investigated. All approaches include an aluminum rail on top of the silicon dioxide layer. Two of them are equipped with an additional n-doped implant which runs exactly underneath the bias rail. This 1.5 µm deep implant has a concentration of $10^{19}\,\mathrm{cm}^{-3}$ and a width of 4 µm. The difference between these two layouts is the electrostatic potential the additional implant is set to: either the implant is grounded by the aluminum rail through an additional conductive via in the silicon dioxide or it is kept floating. The latter situation simulates the condition of a bump bonded readout chip without a bias ring connection. The final three designs are shown in figure 7.3.

The last design variation that is applied to all three approaches is a varying p-stop distance d_{pstop}. For the design without an implant, the distance is reduced gradually from 13 µm down to 0 µm, resulting in a common p-stop configuration of the pixel isolation. In that case, the pixels are no longer isolated by their individual rings but share one wider p-stop that ensures a proper pixel isolation. For the other two designs, the distance can only be reduced down to 6 µm due the additional bias rail implant which prevents the two p-stop rings from merging.

7.3. The electric field distribution

Once the different geometries have been defined, the SDE can create the mesh file for each individual device and pass it to the Device Simulation tool. There, the mesh file is used to integrate the device in a small electronic circuit in order to provide the necessary potentials

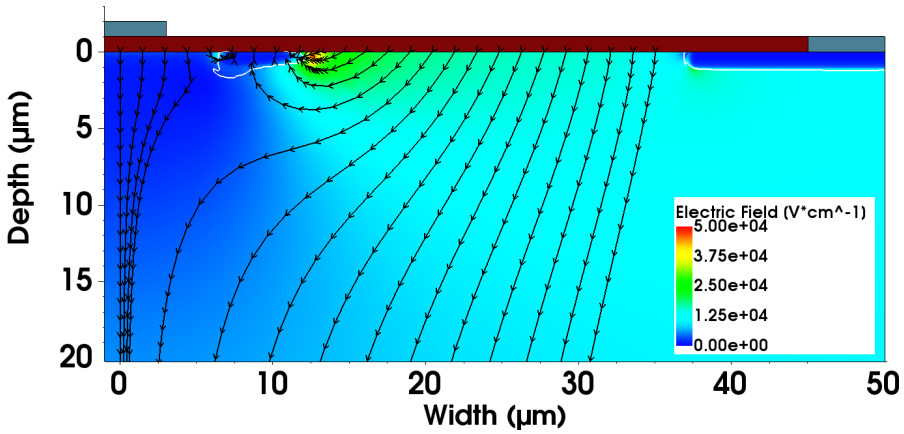


Figure 7.4.: Electric field distribution at the frontside of the base design at $V_{\text{Bias}} = -150\,\text{V}$. The maximum electric field in the bulk is located at the interface between the p-stop (white line) and the electron accumulation layer below the silicon dioxide. Higher field strengths in the oxide layer are not taken into account.

to simulate the configuration of the device during operation. In a minimal working setting, the circuit solely consists of the device itself and the necessary bias voltages for the individual aluminum terminals. For the n-in-p type silicon sensors used in this study, all terminals on the frontside, both pixels and the bias rail, are set to ground potential, whereas the backside is set to $-150\,\text{V}$, ensuring a slight over-depletion of the bulk and thus maximizing the sensitivity of the device. The resulting potential difference between the frontside and the backside leads to a linearly increasing electric field across the bulk, where the field lines run perfectly in parallel to each other through almost the entire device. Only in the region very close to the implants at the frontside the field lines are getting bent and the electric field becomes more inhomogeneous. A close-up of the electric field distribution at the frontside of the standard layout is shown in figure 7.4.

The electric field lines start at the grounded pixel implants and at almost the entire silicon–silicon dioxide interface due to the fixed oxide charge. Most of the field lines run across the silicon bulk and end at the negative terminal at the backside of the device. Free electrons follow these field lines in the opposite direction and are either collected by the pixel implants or accumulate at the interface to the silicon dioxide. In order to prevent short circuits between the pixels, the resulting accumulation layer is disrupted by the p-stop implants, which significantly disturb the shape of the electric field at this location. The particularly high field in the oxide below the rail of approximately $300\,\text{kV}\,\text{cm}^{-1}$ should not impair the performance of the device, as the dielectric strength of the insulating silicon dioxide is comparably high ($6\,\text{MV}\,\text{cm}^{-1}$ [Har17]) and not of concern at this point.

However, the situation changes for the electric field in the silicon bulk. Even small local spikes that exceed the maximum tolerable electric field strength of $3 \times 10^5\,\text{V}\,\text{cm}^{-1}$ can lead to an early breakdown of the sensor [Har17]. As a consequence, the sensor would have to be operated at lower bias voltages, which could lead to an under-depletion of the bulk and thus to considerable charge and efficiency losses of the device. For that reason, determining the maximum electric field in the bulk is one of the most important steps to predict the high voltage stability of the device.

7.3.1. The maximum electric field in the bulk

The location of the maximum electric field depends on the chosen bias rail approach, which is shown in figure 7.5. For the design without an additional implant and the geometry with a floating implant below the bias rail, the maximum electric field is always located at the interface between the p-stop and the electron accumulation layer closer to pixel implants. In case of a grounded implant, the maximum is also located at the interface between the p-stop and the electron accumulation layer, but closer to the bias rail. The reason for the increased electric field at these points is the high potential difference between the floating p-stop implant, which has approximately the same potential as the bulk, and the conductive electron layer which is set to ground potential by the nearby grounded pixel or rail implant. By comparing the absolute values of these local maxima, a first tendency towards a preferred bias rail approach and p-stop distance can be obtained. The simulated maximum electric field as a function of the p-stop distance for all three bias rail approaches is shown in figure 7.6. The results show that the maximum electric field for the design without and the design with a floating implant increases with increasing p-stop distance. This is caused by the fact that moving the floating p-stop implant closer to the grounded pixel implant causes more field lines to bend towards the p-stop implant and thus increases the electric field strength in that particular region. However, comparing these two approaches, the design without an implant seems to be slightly more favorable, as it shows consistent lower electric field strengths across all possible p-stop configurations. Moreover, since the minimal p-stop distance is not limited by an additional rail implant, the maximum electric field can be further reduced to a minimum in the common p-stop configuration. For the connected implant approach, where the maximum electric field is located closer to the bias rail, the dependence between the p-stop distance and the maximum electric field is reversed. In this case increasing the p-stop distance results in less bent electric field lines between the grounded rail and floating p-stop implant and therefore to a reduced electric field strength in the end.

Both approaches, the base design without a bias rail implant in the common p-stop configuration as well as the geometry with a grounded implant with a wider p-stop distance seem to be the two preferred configurations that feature the lowest maximum electric field and thus ensure the best high voltage stability of the device.

The analysis of the electric field, however, can only provide a first indication of why the test beam measurements of the PS-p light show severe inefficiencies between two adjoining pixel rows. For that reason, further simulations have to be conducted to shed more light on this particular problem and to develop possible design improvements to avoid preventable inefficiencies in advance.

7.4. Transient simulation

To determine the charge collection efficiency of a silicon sensor, a combined heavy ion and transient simulation is performed. During the heavy ion part of the simulation, a charged particle is shot through the device, which generates a user-defined number of electron–hole-pairs along its track. For this study, a constant generation of 75 electron–hole-pairs per µm along the particle path through the device is assumed. The transient part of the simulation is responsible for simulating the drift of charge carriers along the electric field lines through the device. Since this simulation is based on n-in-p type silicon, electrons are collected by the grounded pixel implants on the frontside, while the majority of the holes drift to the backside of the device. This leads to an electric current in the device that can be determined by the simulation tool.

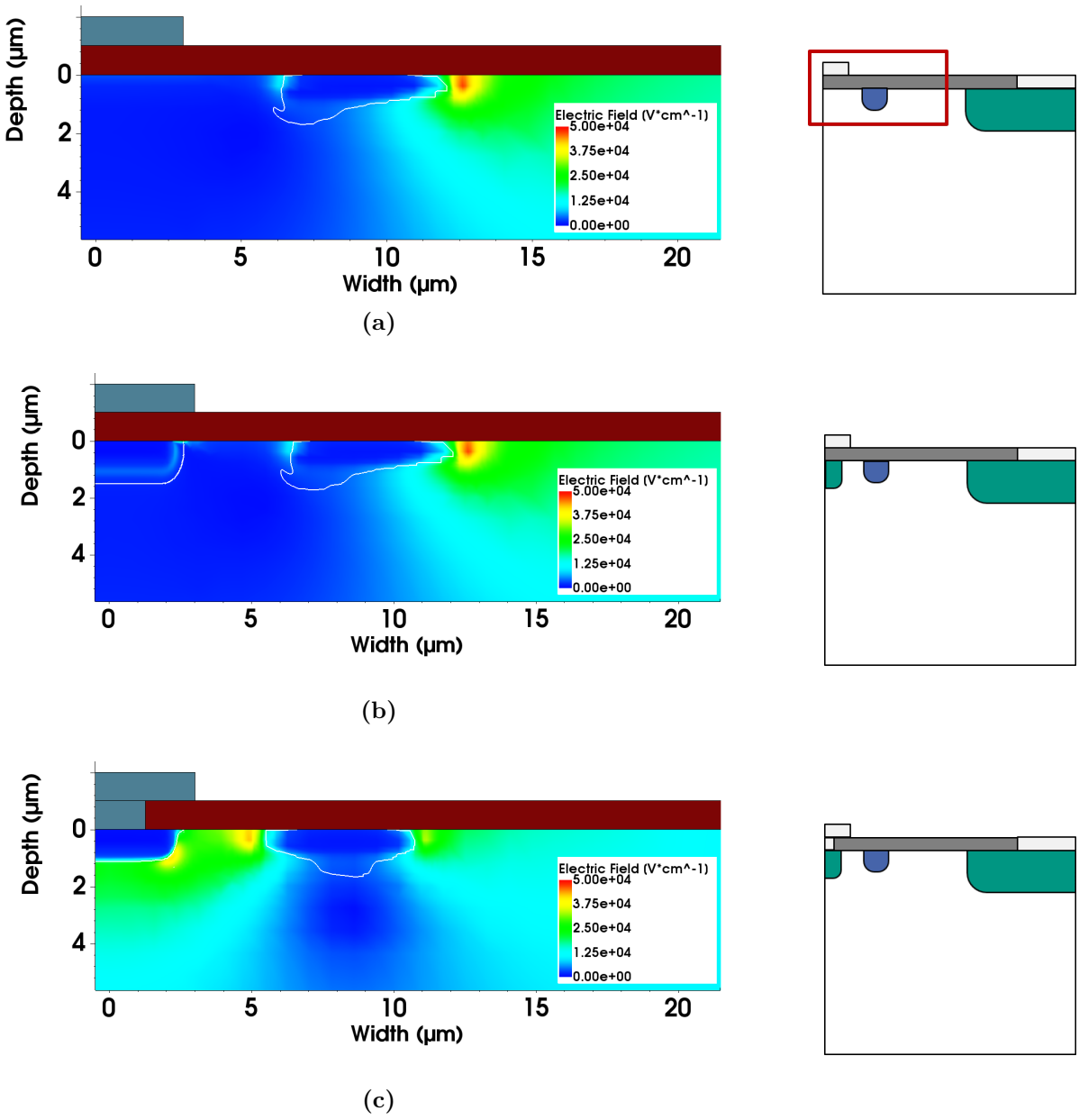


Figure 7.5.: Location of the maximum electric field. The red box in the top right drawing corresponds to the area that is shown in the electric field map. The maximum electric field is always located at the interface between the p-stop and the silicon dioxide. In case of the design without an implant (a) and the design with a floating implant (b) the maximum electric field is located closer to the pixel implant. If the additional implant is grounded by the aluminum rail (c), the maximum is located closer to the rail implant.

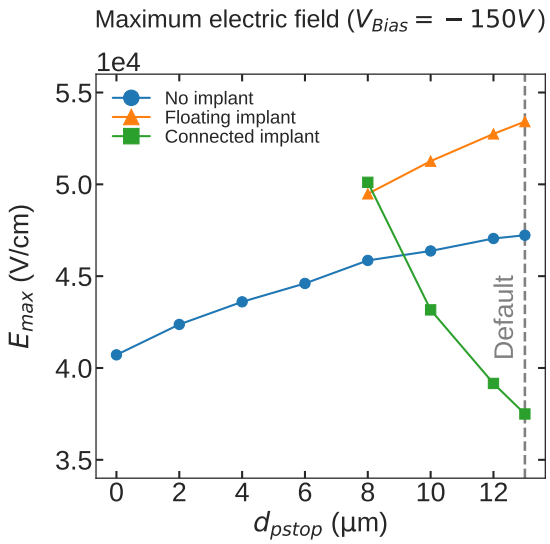


Figure 7.6.: Maximum electric field as a function of the p-stop distance for three different bias rail approaches. The dashed line marks the point of the default p-stop distance that was used for the PS-p light. The designs without an implant (blue) and the design with a floating implant (orange) benefit from closer p-stop rings of the adjoining pixel cells. For the design with a grounded implant (green), on the other hand, the maximum electric field reduces with increasing p-stop distance. Only the design without a bias rail implant is able to form the common p-stop configuration at $d_{\mathrm{pstop}} = 0\,\mu\mathrm{m}$.

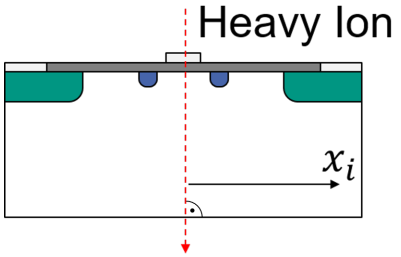


Figure 7.7.: Schematic of a heavy ion simulation of the standard geometry. The charged particle penetrates the sensor at the frontside and generates charge along its track through the bulk (red dotted line). By shifting the impact point from the middle towards one of the pixels, a position dependent charge collection efficiency can be obtained.

By integrating the induced current at each terminal over the time, the collected charge Q_i can be obtained:

$$Q_i = \int_0^T I_i(t)\ \mathrm{d}t\ ; \qquad T = 25\,\mathrm{ns}. \tag{7.3}$$

An integration time of 25 ns is chosen, which matches the typical integration time of all readout chips of the CMS tracker. The charge collection efficiency (CCE) is then defined as the sum of charge which is collected by each pixel i divided by the total amount of positive charge Q^+_{tot} generated in the device

$$CCE = \left| \frac{Q_1 + Q_2}{Q^+_{tot}} \right|. \tag{7.4}$$

The normalization factor Q^+_{tot} is composed of the charge collected by the backside Q^+_{back} and the positively induced charge at the bias rail between the two pixel cells Q^+_{rail}. If negative charge is induced at the rail Q^-_{rail}, the normalization consists solely of the backside contribution. In this case, electrons are attracted by the bias rail are therefore no longer available for signal generation within the rather short integration time.

$$Q^+_{tot} = Q^+_{back} + Q^+_{rail} \qquad \text{for } Q_{rail} > 0, \tag{7.5}$$
$$Q^+_{tot} = Q^+_{back} \qquad \text{for } Q_{rail} \leq 0. \tag{7.6}$$

If the remaining charge in each pixel does not exceed the threshold of the connected readout chip, the efficiency of the entire detector will be affected. In order to obtain a spatial dependency of the CCE in the device, the heavy ion particle and its interception point are shifted along the device. Due to the mirror-symmetric geometry of the device, only one half of the sensor is included in the scan, which is shown in Figure 7.7. The simulation is performed with non-periodic boundary conditions, which means that the vertical components of the electric field and the current density at the edge of the device are set to zero.

The charge carrier lifetimes of electrons and holes, before they recombine with one of their respective counterparts in the bulk, are set to the default values of Synopsys TCAD $\tau_e = 1 \times 10^{-5}\,\mathrm{s}$ and $\tau_h = 3 \times 10^{-6}\,\mathrm{s}$, respectively. Since the drift times of the charge carriers are in the order of nanoseconds and thus significantly shorter than their lifetime, the default value remained unchanged for the entire simulation. Finally, no further adjustments are made

regarding the surface recombination velocity S_0, which is set to $10^3\,\mathrm{cm\,s^{-1}}$ for both, electrons and holes, throughout the simulation.

7.5. Analysis of the Charge Collection Efficiency

The results of the charge collection efficiency simulation for all different bias rail approaches are shown in figure 7.8.

In general, a strong dependency between the heavy ion impact point and the charge collection efficiency at the pixels is noticeable. If the particle penetrates the sensor close to the pixels, all charge is collected by the implant and processed by the connected readout electronics, leading to a CCE of 100 % regardless of the implemented bias rail approach. However, as soon as the particle hits the sensor closer to the rail region, the situation changes and differences between the individual geometries become noticeable. Figure 7.8a shows the location-dependent charge collection efficiency of the standard geometry, which is solely equipped with a single aluminum rail on top of the silicon dioxide without an additional implant underneath. Some of the electrons that are generated in the area between the two pixel implants get attracted by the grounded aluminum rail on top of the oxide and start to drift along the corresponding electric field lines. According to the Shockley-Ramo theorem, this will induce a measurable current in the bias rail until the electrons get absorbed in the accumulation layer at the silicon dioxide interface between the p-stops. However, due to the finite inter-pixel resistance, the excess electrons of the accumulation layer are still able to overcome the p-stop barrier after a certain period of time and can be collected by the pixel implant. This again will induce a current of opposite polarity in the bias rail, which compensates the current that was originally generated. Nevertheless, since the integration time is comparably short against the release time of the electrons in the accumulation layer, most of the temporally trapped electrons are lost for the readout and the subsequent signal processing, leading to a reduced CCE of the sensor. By reducing the distance between the p-stop less space below the rail is exposed to the charge carriers and thus less charge is attracted by the bias rail and the CCE increases. In case of the base layout, the p-stop rings can be brought into a common p-stop configuration, where the common p-stop effectively shields the rail by repelling the electrons and guiding them to the pixel implants. In the common p-stop configuration the position dependence disappears and the CCE becomes constant at 100 %. The situation changes significantly as soon as a grounded n^+-implant is added below the aluminum rail, which is shown in figure 7.8b. In this case, the rail acts as a bias ring extension into the pixel matrix, which can increase the high voltage stability of the sensor due to a reduced maximum electric field in the default p-stop configuration. However, this approach also introduces an additional charge collecting electrode between the pixels, which is not connected to any front-end electronics of the readout chip. Therefore, all charge that is collected by the rail implant is not available for signal detection and thus reduces the CCE to almost 0 % if the charge is generated below the rail. The additional rail implant also prevents the p-stop rings from merging and forming the preferable common p-stop configuration. The same is true for the last of the three investigated bias rail approaches: the floating implant. Since the pixels of DC coupled sensors are usually grounded through the virtual ground potential of the readout chip, there is no need to ground the bias ring during operation, which would keep the bias rail and therefore the rail implant floating. The CCE in the floating implant configuration is shown in figure 7.8c. As expected, the CCE increases significantly compared to the grounded implant setting. However, the most preferred common p-stop configuration is still not achievable in this design due to the rail implant between the p-stop rings.

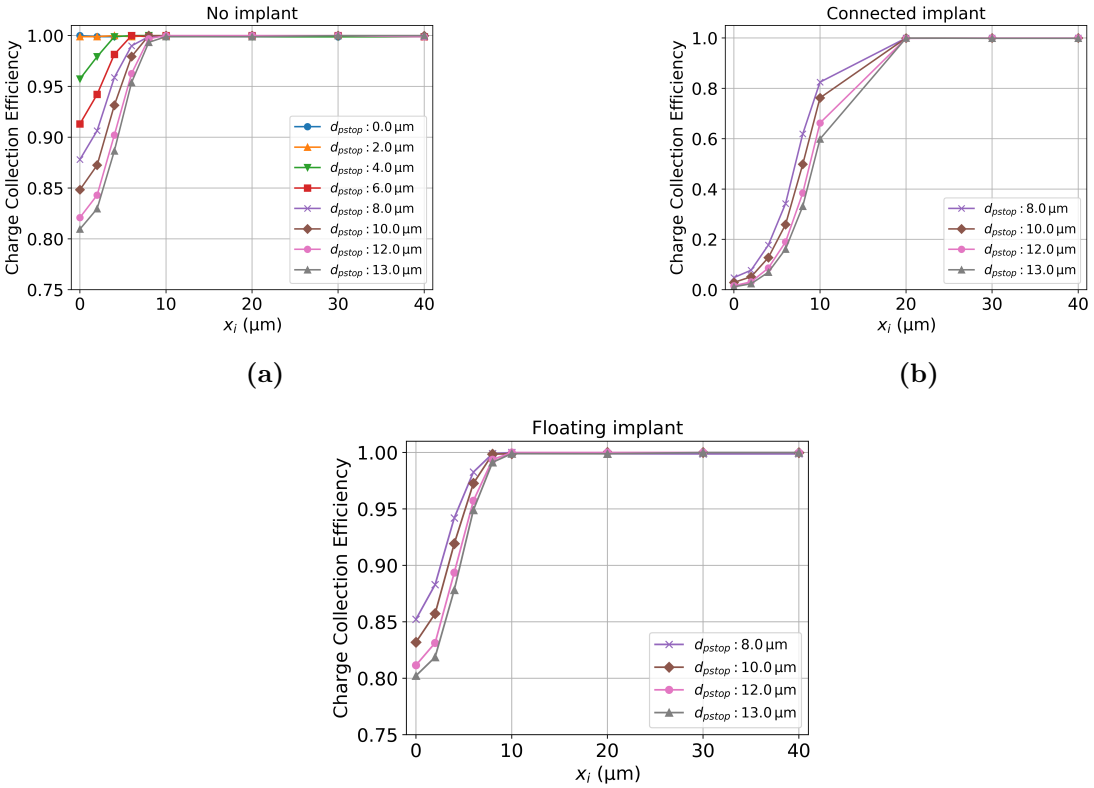


Figure 7.8.: Charge collection efficiency (CCE) as a function of the heavy ion impact point at $V_{\text{Bias}} = -150\,\text{V}$ for different p-stop distances and bias rail approaches. All designs benefit from closer p-stop rings which leads to higher CCE regardless of the rail approach. For the base design without a bias rail implant (a), the CCE drops to almost 80 % if the particle hits the sensor exactly in the middle of the bias rail ($x_i = 0\,\mu\text{m}$) and the p-stops rings are separated by 13 µm. In the common p-stop configuration, the CCE becomes constant at 100 % across the entire sensor. If a connected implant is added in the gap between the pixels (b), the CCE drops down to 0 % below the rail. If the additional implant is kept floating (c), the CCE recovers and almost reaches the same level as the design without the implant.

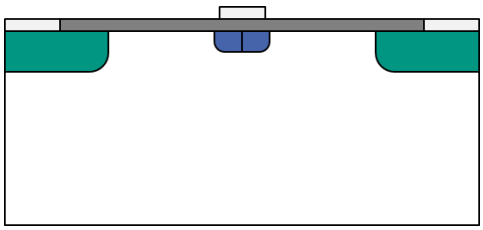


Figure 7.9.: Schematic of the common p-stop design. The individual p-stop rings are merged together, forming the desired common p-stop configuration (blue). In this approach, the bias rail (gray) on top of the oxide (dark gray) is effectively shielded by the p-stop, preventing the electrons from accumulating below the silicon dioxide and therefore reducing the charge collection efficiency.

7.6. Suggestions for the final layout

All three investigated bias rail approaches are suitable solutions to test segmented silicon sensors before assembly. The actual implementation of this rail, however, has a significant effect on the performance of the sensor during data-taking. While a grounded rail implant will always lead to a CCE of almost 0 % between two adjoining pixel rows, a floating implant can recover most of these inefficiencies and increase the CCE to a minimum of 80 %. By reducing the p-stop distance from 13 µm down to 8 µm the CCE can be increased even further to 85 % below the rail. Nevertheless, the simulations show that a bias rail with only an aluminum rail on top of the silicon dioxide is the most promising concept. This design features a low maximum electric field in the bulk as well as the highest CCE among the three approaches. What makes the no-implant approach even more favorable in the end is the possibility to reduce the distance of the p-stop down to 0 µm and thereby forming the preferred common p-stop configuration, which is illustrated in figure 7.9. Sensors with such kind of isolation technique feature a high efficiency below the bias rail, hence a constant CCE of 100 % along the gap between two pixel rows. These results are in good agreement with the simulations conducted within the ATLAS collaboration [Unn+16].

Since moving the individual p-stop rings closer together is a rather small design change of the already tested layout, the common p-stop design is considered as a superior successor of the PS-p light prototype design. For that reason, it is not surprising that the results of this simulation have been taken into account during the design process of the first full-size PS-p prototype wafer which will be discussed in the following chapter.

Part III.

The PS-p

8
The PS-p prototype

After the successful testing of the PS-p light sensors, the design of its first full-size successor is the next step towards the final PS-p sensor for the PS modules of the CMS Outer Tracker. Therefore, all the experience of recent years has been incorporated into the design of the first PS-p prototype wafer and the choice of its base material. The simulation results presented in the previous section have been taken into account and had a significant impact on the development of additional smaller prototype sensors on the wafer. The following chapter gives a detailed overview of the chosen wafer material as well as the design process of the first PS-p prototype wafer, including the full-size sensor and various smaller prototypes.

8.1. Wafer properties

Similar to the PS-p light prototype, the first thoughts in the project are devoted to the decision on a suitable wafer material. Since most of this discussion has already been covered in chapter 5, only the most important arguments are presented in the following.

The CMS Outer Tracker community can look back on many years of experience with numerous silicon sensor projects with various manufactures, including the sensors of the current CMS Outer Tracker, the HPK campaign, the more recent 2S sensor prototypes as well as the PS-p light sensor wafers. Consequently, there is detailed knowledge about the required wafer properties such as growth process, bulk resistivity and active thickness, to ensure high signals and excellent radiation hardness throughout the entire lifetime of the detector. In case of the PS-p the choice fell on the well known float zone silicon (FZ) base material with a bulk resistivity between $4\,\mathrm{k\Omega\,cm}$ and $8\,\mathrm{k\Omega\,cm}$.

Unlike the 2S sensor, however, the active thickness of the PS-p is not primarily determined by the signal height required to achieve a desirable signal-to-noise ratio of $S/N > 10$. The reason for this is the very low front-end noise of the MPA readout chip of less than 200 electrons compared to about 1000 electrons in the CBC [CMS18]. Therefore, thin sensors are preferred for several reasons. First, thin silicon sensors contribute less to the material budget in the tracker. This leads to less multiple scattering of traversing particle, resulting in a better momentum and energy resolution. Second, since the PS module is designed in such a way that only the sensor back plane is attached to the cooling system of the CMS Outer Tracker, the 16 MPAs with a total power consumption of almost 3 W have to be cooled through the bump bonds and the sensor itself [CMS18]. Less thermal mass, i.e. thinner sensors, contribute to a better heat transfer from the chips to the cooling system. Third, a smaller active thickness leads to less leakage current and lower depletion voltages (shown in section 4.3), which reduces the overall power consumption of the module. And finally, thin sensors convince by their better annealing behavior and thus guarantee constant performance even after long maintenance intervals at room temperature. In addition to these wafer properties, the CMS Outer Tracker community has defined various parameter limits that must be met by each individual sensor. These limits include a full-depletion voltage of $V_{\mathrm{dep}} < 150\,\mathrm{V}$, a breakdown voltage of $V_{\mathrm{break}} > 700\,\mathrm{V}$ and a current per pixel of $I_{\mathrm{pixel}} < 300\,\mathrm{pA/pixel}$, to name but a few. A detailed overview of all

requirements can be found in the technical design report of the Phase-2 Upgrade of the CMS Tracker [CMS18].

The selected wafer size for the PS-p prototype is 6-inch, which has become an industry standard size for silicon sensors in recent years. This allows the wafers to be produced on optimized production lines instead of small batch R&D lines at the foundries. The 6-inch wafer is also big enough to hold two full-size sensors, which immediately halves the number of required wafers. Both arguments are reflected in lower costs and thus strengthen the decision to produce the first full-size PS-p prototype on a 6-inch wafer.

8.1.1. Submission at HPK

After the official call for tender of 40 prototype wafers, HPK has again prevailed among the applicants. Not only do they agree with all the requirements set by the Outer Tracker sensor community, they have also produced sensors in very good quality in the past, namely during the HPK campaign as well as the first prototypes of the 2S sensor. Hamamatsu proposed to split the order into two independent batches with 20 wafers each and to agree on the material of the second batch depending on the test results of the sensors of the first one. In the end, the final order included one batch of 20 silicon wafers with an active and physical thickness of 200 µm (thFZ200) and a second batch including the same number of wafers with a physical thickness of 320 µm and a moderate deep diffused backside to reach an active thickness of 290 µm (FZ290).

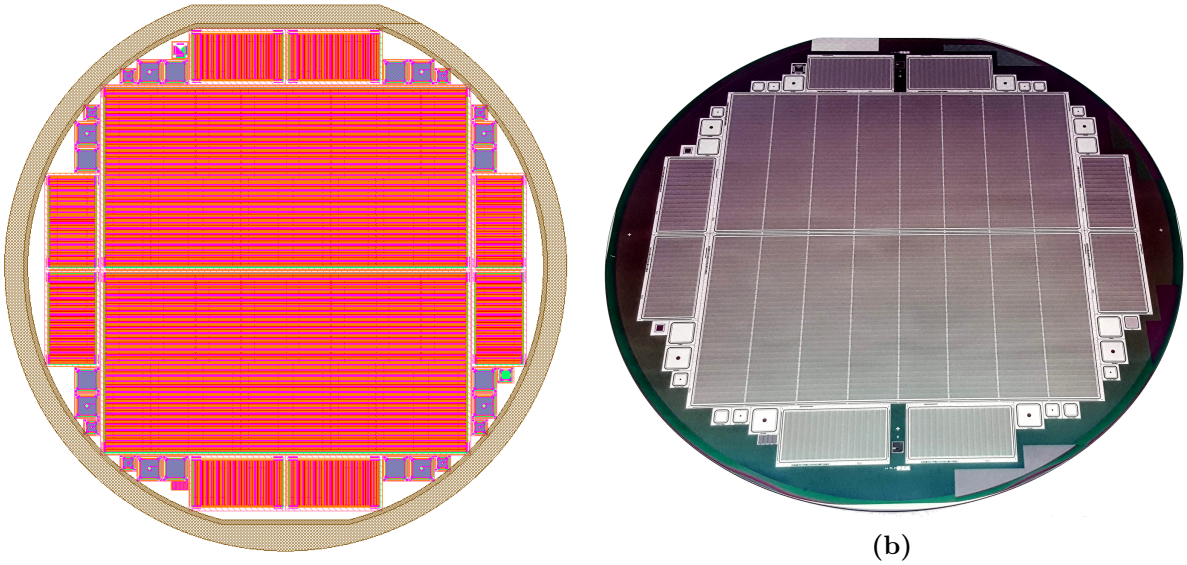
8.2. Design of the PS-p prototype wafer

The production of silicon sensors and semiconductor devices in general are based on the photolithographic process (see e.g. [Spi05]). Photolithography uses light to transfer a geometric pattern from a photomask onto a substrate that has been coated with a light-sensitive photoresist material. Only the light exposed parts on the photoresist are removed by a subsequent chemical treatment, exposing the substrate for further processing, like etching, ion implantation or deposition of new material. Designing a silicon sensor is therefore mainly devoted to the design of these photomasks, with each mask representing one main step in the production process. In case of the PS-p, six of these layers are required to form a fully functional sensor: the n^+-implants, the p-stop rings, the conductive vias through the coupling oxide, the highly doped p^{++} sensor edge, the metallization layer and the openings of the comprehensive passivation layer. Unlike the 2S sensor, no polysilicon layer is required due to the use of punch-through structures instead of polysilicon bias resistors for biasing.

The minimum and maximum size of the individual microstructures as well as the distances between them are limited by the machines used by the manufacturer and specified in their design rules. The final sensor design must also comply with the boundary conditions set by the PS module designers as well as the chip developers, who for example define the position of the bump bond pads and the expected capacitance of the pixels. The design process of the photomasks of the first full-size PS-p prototype wafer is one of the main topics of this work and is presented hereafter.

8.2.1. Klayout and the macro framework

The implementation of the photomask design is performed within the high performance layout viewer and editor, called KLayout [Köf18]. KLayout is an open source software tool that provides



(a) (b)

Figure 8.1.: The final GDS output file (a) and the processed PS-p wafer (b). Hamamatsu made some final changes to the proposed wafer layout, which are reflected in the additional space between some single sensors as well as some additional test structures.

full support for the GDS[1] and OASIS[2] file formats. For editing, KLayout primarily features a simple drag & drop system, which can be used to create and arrange arbitrary geometries as well as organizing them in different layers and cell hierarchies. This approach, however, becomes more and more cumbersome for large scale geometries like a silicon sensor. For that reason, KLayout also includes a macro development environment that is capable of interpreting Ruby as well Python scripts for an automated design process. This macro environment was used to create a Ruby based software framework that acts as a wrapper around KLayout's built-in commands in order to provide more characteristic sensor geometries, like rectangles with rounded corners, punch-through structures, bias grids and other sensor peripherals. The individual parameter sets of each geometry are stored in text based configuration files that are passed at the beginning of the macro call. An example of such a configuration file can be found in Appendix B. High-level geometries, like a pixel matrix, are generated by organizing low-level geometries, like a pixel cell, into hierarchical structures, which reduces code duplication and parameter definitions to a minimum.

The framework was initially developed in the context of the CMS Pixel Phase-2 prototype wafer [Sch15] and has now been transferred to the Python programming language and further developed for the PS-p prototype wafer.

8.2.2. The wafer layout

The finalized 6-inch PS-p prototype wafer GDS output is shown in figure 8.1. The two full-size PS-p sensors in the middle of the wafer are surrounded by eight smaller macro-pixel sensors comprising four different layout variants that are going to be bump bonded to only

[1] The *Graphic Data System* (GDS) file format is the de facto industry standard to store layouts of integrated circuits.

[2] The *Open Artwork System Interchange Standard* (OASIS) file format has been developed as a successor to GDS.

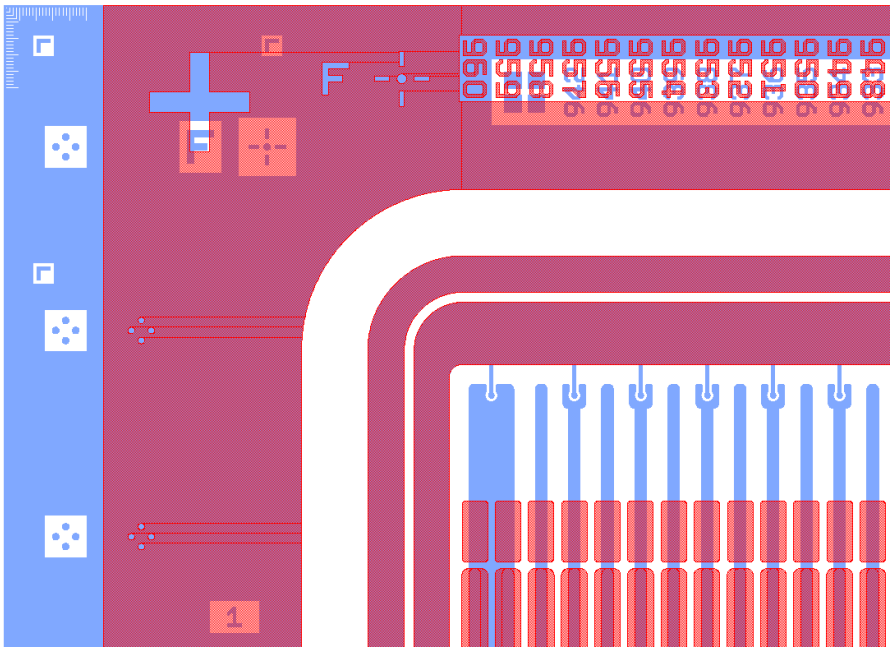


Figure 8.2.: Edge aluminum layers of a PS-p (blue) and PS-s (red) on top of each other. The bias and guard ring lie perfectly on top of each other, leading to the exact same active area of both sensors. The PS-p is 600 µm longer on its long side than the PS-s, exposing both edges and their alignment marks simultaneously.

one MPA readout chip instead of 16 as the full-size one. These *single* sensors are intended for smaller R&D projects and the first prototype assemblies. The latter are of particular interest to the chip developers, who can use them to ensure proper operation of their readout chip before producing the first working full-size macro-pixel subassembly (MaPSA). The wafer is supplemented by several diodes, MOS structures, gate controlled diodes (GCD) and a so-called Flute structure [Hin+18] [GF66]. All these smaller structures are used as reference structures for quality assurance in dedicated process quality control (PQCs) centers during the production [CMS18]. This work, however, focuses exclusively on the full-size PS-p sensor and its single sensor derivatives. Determining their electrical properties as well as the efficiency of the different single sensor layouts to assess the proposed design changes derived from the TCAD simulations are the main objectives discussed in the following chapters.

8.3. The full-size PS-p sensor

The two full-size PS-p sensors take up the main part of the wafer. Each of these two sensors has an outer dimension of 98.740 mm × 49.155 mm and includes a matrix of 32 × 944 individual pixel cells. The sensor has been designed in close cooperation with the MPA chip developers and the designers of the PS-s. Already at a very early stage in the design process, the Outer Tracker community agreed on an almost identical sensor periphery for the PS-p and the PS-s in order to cover the exact same active area and to provide similar alignment marks on the sensor edge for a simplified alignment process during module assembly. As shown in already mentioned in section 3.2.4, the PS-p is 600 µm longer than the PS-s (figure 8.2), making both sensor edges visible for pattern recognition algorithms during the assembly procedure.

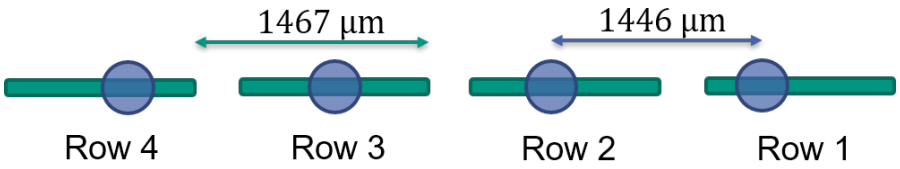


Figure 8.3.: Shifting bump bond pads on the PS-p. Since the pixel pitch is different to the pitch of the bump bond pads on the readout chip, the latter have to be shifted within the pixel cells across the pixel rows.

8.3.1. Pixel cells

The most widely used cell, called the *standard* or *normal* pixel includes a 1392 µm long and 25 µm wide n^+-implant, which leads to the agreed width to pitch ratio of $w/p = 0.25$ for all sensors of the Outer Tracker. The aluminum overhang of 5 µm and the 6 µm wide p-stop rings that are separated by a gap of 4 µm are also the same as for the two strip sensors. However, instead of polysilicon resistors, each pixel of the PS-p includes a punch-through structure (PTS) that is necessary to ground the pixel implant during testing and establish a protection mechanism for the readout chip. This PTS is attached alternately to the lower and upper end of the macro-pixel cells along the individual pixel rows.

In contrast to the PS-p light, the Outer Tracker sensor community decided to integrate only the wider gap pixels with an implant width of 125 µm to cover the space between two neighboring MPAs and to discard the edge pixel and thus also the corner pixel geometry in the first and last row of the sensor. However, to maximize the active area of the sensor the additional space at the edge that would otherwise have been added to the edge pixels is now evenly distributed among all pixels on the sensor. As a result, the pixel pitch along the columns increases from 1446 µm of the PS-p light and the MPA to 1467 µm. In order to avoid changes to the MPA floor plan, it is important to keep the distance between the bump bond pads unchanged. For that reason, the bump bond pads have to be shifted within the pixel cells across the pixel rows in the matrix, which is depicted in figure 8.3.

In the end, all these changes lead to a reduced complexity of the sensor, while keeping the active area maximized and the development of the MPA unaffected. Nevertheless, it is important to point out that the sensor pitch must be used for track reconstruction instead of the pitch of the front-end connections. One section of the final PS-p layout, including both types of pixel cell geometries and the overlying MPAs, is shown in 8.4.

8.3.2. Peripheral structure

In total 30 208 pixels are placed on the PS-p sensor, forming the active area of over 4400 mm^2. This active area is surrounded by several peripheral structures in order to test, isolate and protect the matrix from external influences. The periphery of the PS-p consists of a global p-stop which encloses the active area, the bias grid, the guard ring and the sensor edge. The mentioned bias grid comprises 31 aluminum bias rails that run in between the individual pixel rows, connecting all PTS of the individual pixel with the all-surrounding bias ring. All these structures are again surrounded by the guard ring that protects the inner geometries from the high potential of the sensor edge. The dimensions of these peripheral structures are identical to those of the PS-s (see figure 8.2).

The quite large area of the sensor edge is used to display for instance the sensor label, the row and column numbering and an arrow to define a dedicated orientation of the otherwise completely symmetric device. Multiple alignment marks in the corner and along the short

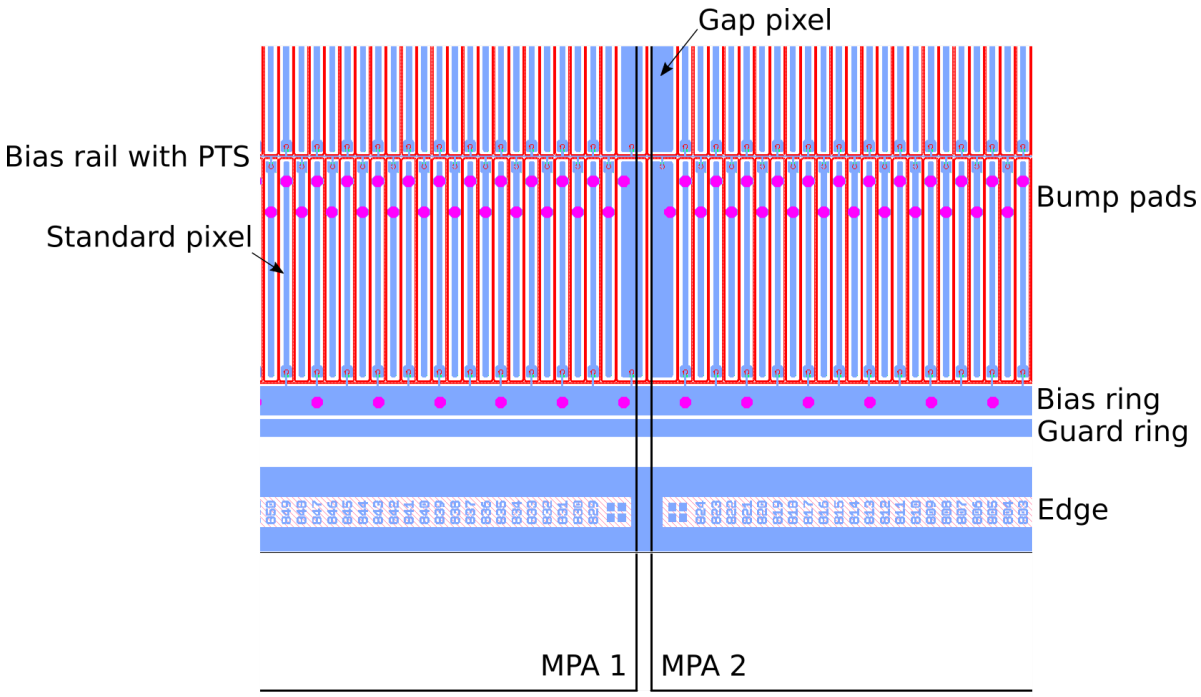


Figure 8.4.: One section of the PS-p pixel matrix. Gap pixels with a pitch of 200 µm below the edge of each MPA cover the additional space between two neighboring readout chips. In total, 31 bias rails run in between the pixel rows, connecting the individual PTS with the bias ring.

edges are added to support the alignment of the PS-p to the PS-s. A measurement scale in each corner and the middle of the short edge are used as a reference measure for the dicing precision of the sensor. Lastly, alignment marks along the long edge of the sensor are used to align the sensor with the MPAs during the flip-chip process.

One corner of the final sensor periphery, including its dimensions is shown in figure 8.5.

8.4. PS-p single sensors

In addition to the two full-size sensors, a total of 8 *single sensors* are placed on the PS-p prototype wafer. All these smaller prototypes are based on the same pixel geometry and a very similar periphery as their full-size equivalent. However, some of them differ in their respective bias structure as well as in their individual pixel isolation geometry. In total, four different layout variants have been designed, that are shown in figure 8.6. These smaller prototypes are dedicated to a detailed sensor design study to find an improved layout of the PS-p light prototype and to verify the simulation results that have been presented in chapter 7. The term "single" in this case refers to a sensor that will only be connected to one MPA readout chip instead of 16 like the full-size one. These *Single-MaPSAs* are the first fully functional particle detectors equipped with the full-size MPA readout chip. The performance of these assemblies will be discussed in Chapter 10.

8.4.1. The Standard layout

Half of the single sensors on the wafer (four out of eight) have the same pixel design as their full-size equivalent. Individual p-stop rings, bias rails and a PTS for each pixel cell are the

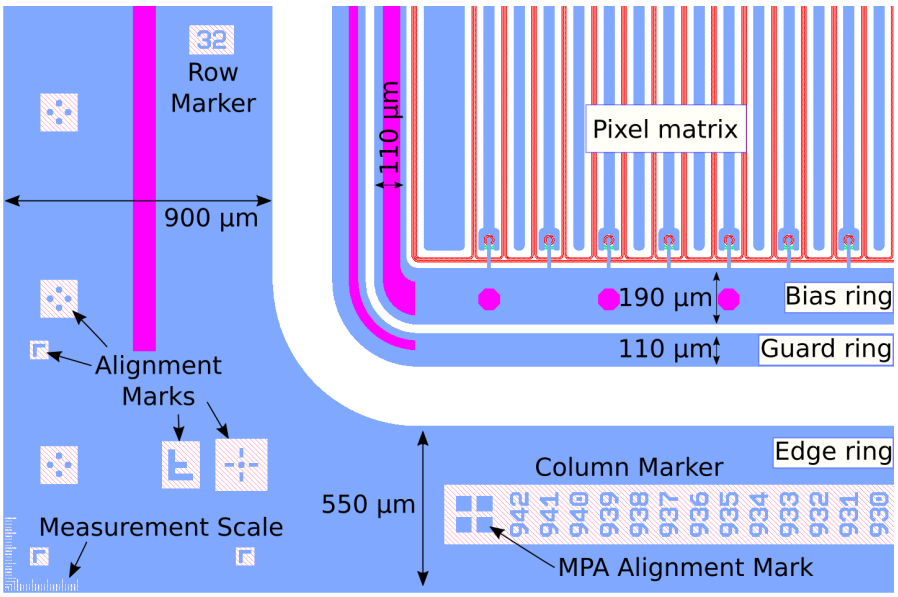


Figure 8.5.: The PS-p sensor edge. The aluminum layer (blue) of the sensor edge displays several alignments marks, a row and column marker, the MPA alignment marks as well as a measurement scale in each corner to verify the dicing precision of the sensor. Each structure includes several longitudinal passivation openings (purple) that are used to contact the aluminum layer during the testing procedure. Hexagonal shaped passivation openings on the bias ring are necessary to connect the ring with the MPA readout chip and thus setting it on ground potential.

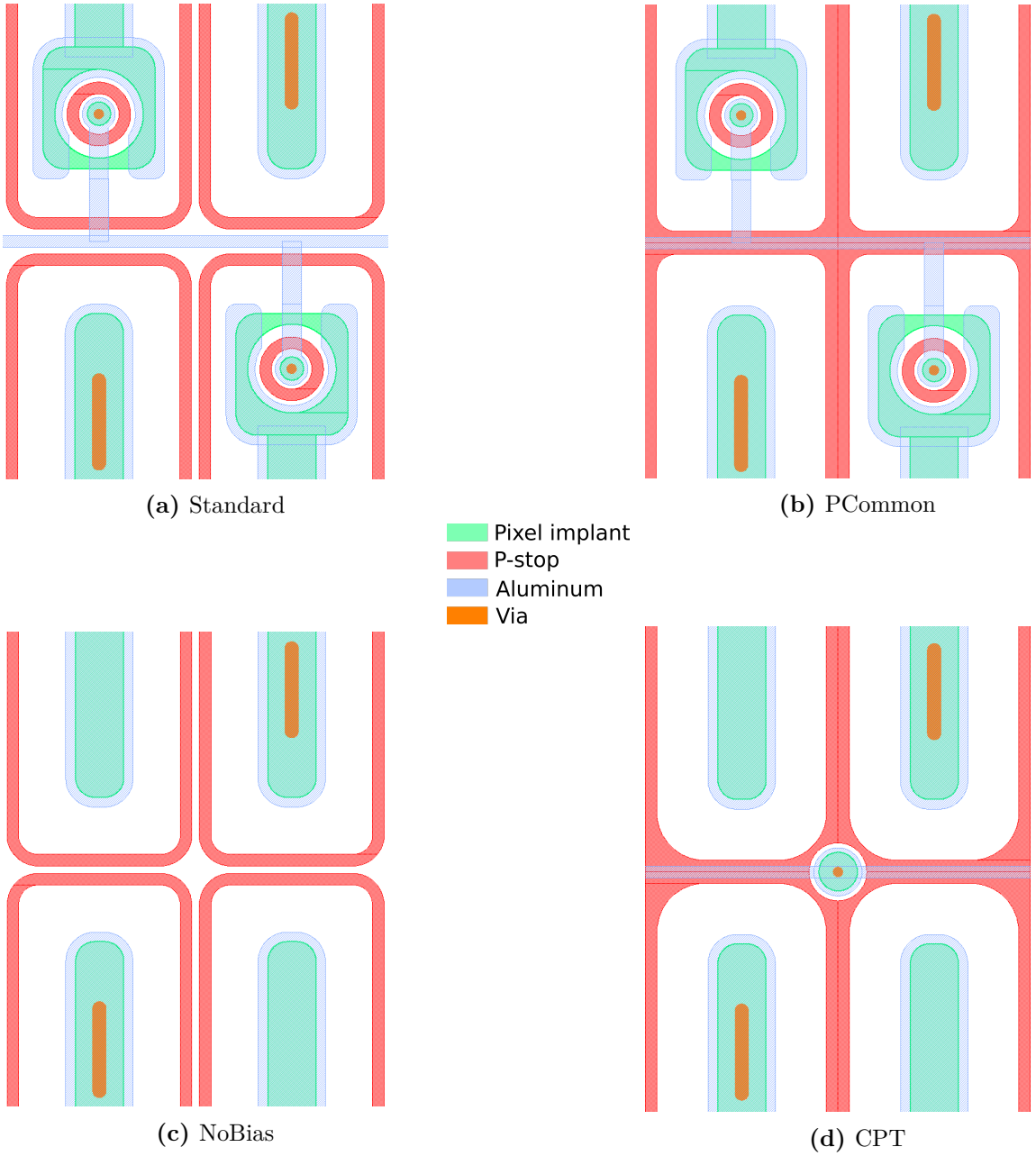
main characteristics of this design. This *Standard* single sensor should perform similarly to the full-size prototype. Thus, the Standard single sensor is used as reference sensor against which all other designs must measure themselves.

8.4.2. The PCommon

Half of the remaining sensors (two out of four) are based on the *PCommon* design, that reflects the optimized design derived from the TCAD simulation results. The sensor still features individual punch-through structures for each pixel cell and the aluminum bias rail between the pixel rows, but comes with the preferred common p-stop configuration. Since there are only very minor differences to the Standard layout, the PCommon sensor seems to be the most promising design variant and therefore exists twice on each wafer.

8.4.3. The NoBias

One of the two remaining sensors is the *NoBias* sensor, which completely drops the bias scheme, including the PTS of each individual pixel cell as well as the aluminum bias rails between the pixel rows. Each pixel implant is surrounded by an individual p-stop ring and no common p-stop configuration has been implemented on this design. Since the pixel matrix only consists of pixel cells, it is supposed to be the most efficient design variant on the wafer. However, this has the disadvantage that the sensor cannot be tested before it is assembled with its readout chip. The NoBias sensor is considered as a reference for the maximum achievable efficiency of the PS-p layout, which will be discussed in more detail in Chapter 10.



(a) Standard

(b) PCommon

(c) NoBias

(d) CPT

Figure 8.6.: The PS-p single sensor pixel designs. The Standard single sensor (a) includes the same pixel matrix as its full size equivalent. In the PCommon layout (b), the distance between the individual p-stop rings is reduced to 0 µm. The NoBias sensor (c) omits the bias grid completely and the common punch-through design (d) tries to minimize the inefficiencies of the bias grid by substituting four PTS by one common PTS in the middle of a 2×2 pixel matrix and removing every second bias rail from the grid.

8.4.4. The Common Punch-Through

The last sensor on the wafer goes one step further than the PCommon sensor and is probably the most optimized version of the Standard layout that can still be tested before assembly. It includes the preferred common p-stop configuration to shield the bias rails and also substitutes the punch-through structures of a 2×2 pixel matrix by one *Common Punch-Through structure* (CPT) in the center of them below the bias rail. Since all punch through structures include a charge collecting bias dot, removing three out of four of them can lead to a noticeable efficiency increase at perpendicular incidence of the particle. This effect is well known and even more important in small pitch sensors, where punch-through structures take up quite a lot of space in the pixel cell. Since two pixel rows are powered by the CPT simultaneously, every second bias rail can be removed, which could increases the efficiency even further.

9

PS-p laboratory measurements

In early 2018, the first batch of 20 PS-p prototype wafers with an active and physical thickness of 200 µm (thFZ200) has been received by CERN. All ten main structures on each wafer, the two full-size PS-p and the eight single sensors, have been tested by Hamamatsu and only the wafers including two full-size sensors that met the requirements [CMS18] have been included in the batch. Most of the received wafers are going to be post-processed by an external company to prepare them for the bump bonding process. In total, 14 out of these 20 wafers were sent to AEMtec in Berlin, Germany, for UBM deposition and the subsequent dicing of the wafers. The remaining six unprocessed wafers of the batch are kept within the Outer Tracker sensor community, five of which have been diced at KIT with a conventional abrasive blade wafer saw. The sensors and test structures of these wafers are used to qualify the wafer material, validate the sensor layout and build first single chip assemblies (Single-MaPSAs) using the gold-stud bump bonding technique at KIT. In order to identify problems at an early stage, it is important to test the material after receiving it. This is necessary to re-evaluate the material selection and, in the worst case, to adjust the mask design for a second batch of 20 wafers that are expected early 2019. For that reason, the following measurement program has been performed: First, some of the full-size sensors have been electrically characterized; Second, a comparison of the electrical properties of the four different single sensor geometries has been carried out. Finally, since some of the sensors show quite early breakdowns, an additional infrared image analysis has been performed to identify possible spots with high current density on the frontside of the sensor that could be caused by some design flaws in the mask set. The results of these measurements are presented in the following.

9.1. Characterization of the full-size PS-p

The following measurements are performed on one of the two ETP probe stations and are based on the previously introduced test procedures of the PS-p light in section 5.4. If not stated otherwise, the measurements are performed at 20 °C and uncontrolled humidity.

9.1.1. I(V) measurements

The current-voltage I(V) measurement provides two of the most important information about a silicon sensor: the overall leakage current and the breakdown voltage. A good PS-p sensor must show a total leakage current of less than $2\,\mathrm{nA\,mm^{-3}}$ at 500 V and a breakdown voltage above 700 V. In addition, only if the current at 700 V does not exceed three times the current drawn at 500 V the sensor is considered suitable to be integrated into one of the PS modules [CMS18].

The I(V) characteristics of the PS-p is obtained by placing the sensor with its frontside facing upwards on the conductive aluminum chuck of the probe station, placing the grounded *bias needle* on the bias ring, applying an increasing negative bias voltage on the chuck while measuring the current that is conducted through the sensor. In total, four of the ten diced full-size sensors have been measured in this way. The results of these measurements together with the measurements performed by Hamamatsu are shown in figure 9.1.

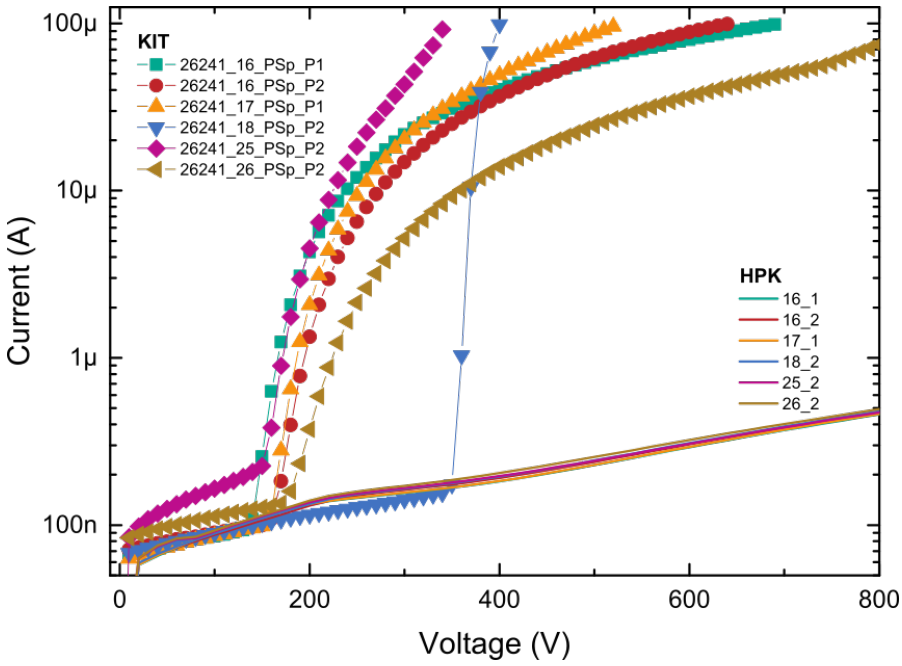


Figure 9.1.: I(V) measurements of several full-size PS-p sensors. Almost all measurements performed at KIT after dicing show an early breakdown below 200 V bias voltage. Only the sensor 18_2 can be operated at 300 V, but does not reach by far the breakdown strength measured by Hamamatsu before the wafer was cut into single dice.

While all sensors look flawlessly on wafer level, it is immediately apparent that all but one of them show a breakdown below 200 V after dicing. After a sharp increase at the beginning of the breakdown, the slope of the current-voltage characteristics starts to decrease at higher bias voltages. Nevertheless, all tested sensors neither meet the requirement of a total leakage current of less than about 10 µA at 500 V nor a breakdown voltage above 700 V. Thus, all of them are disqualified for later use in the module production. However, they are still good enough for first assembly tests and operation below their breakdown voltage.

Since the breakdown occurred right after the dicing process of the wafers, the question arises whether the problem is caused by the dicing process itself. For this reason, the same measurements are repeated with two sensors that are still located on an undiced wafer. The results of two consecutive measurements of both main sensors on one wafer are shown figure 9.2.

At first, both sensors show the same flawless behavior that was already observed by Hamamatsu. However, repeating the measurement after storing the wafer in its original packaging overnight, reveals the same problem of an early breakdown as for the diced sensors, shown before. The problem can therefore not solely be traced back to the dicing process itself.

During a more detailed examination of the wafer, scratches on the backside aluminum layer were observed. These scratches were most likely not present during the wafer probing by Hamamatsu and probably not during the first test on the probe station. Taking the wafer off the aluminum chuck after the first measurement and putting it back on for the second measurement the day after, could have certainly caused some of the scratches on the backside that eventually led to the soft breakdown. One possible explanation could therefore be related to a rather thin backside implantation of the thinned material that might be affected by the scratches on the backside. If this turns out to be true, that would complicate mass production considerably, since the sensors are handled several times before they are integrated in their

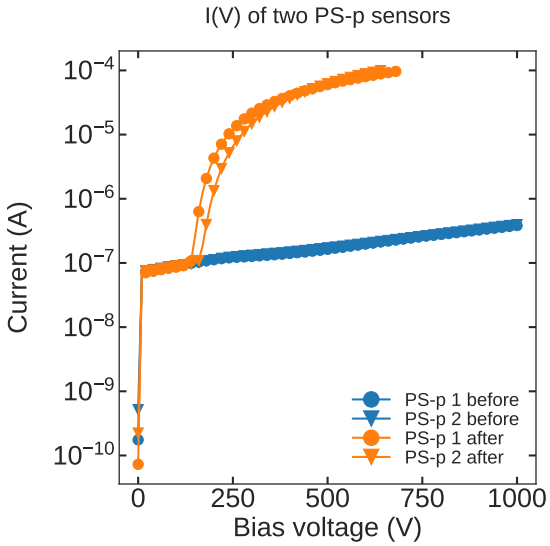


Figure 9.2.: Two consecutive I(V) measurements of two full-size PS-p sensor before and after dicing. During the first measurements (blue) no breakdowns were observed. However, if the same two sensors are measured again the day after storing it in its original packaging, the soft breakdown reappears.

final module. To verify this hypothesis, further measurements were conducted, which include intentionally scratching a structure of the PS-p wafer and comparing the results with the same measurements in the unscratched state of the structure. In order to avoid wasting one of the valuable macro-pixel sensors for this destructive and irreversible measurement, only diodes have been used for this kind of measurement.

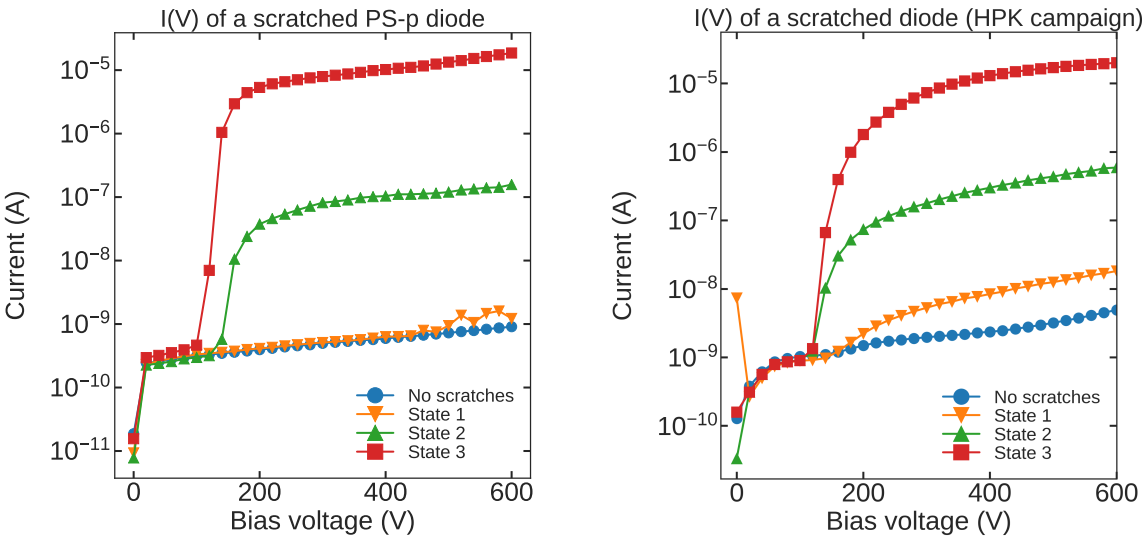
9.1.2. Scratched diode measurements

The PS-p prototype wafer includes 16 diodes of two different sizes that are spread around the two full-size sensors along the wafer edge. They are bundled with a set of additional PQC structures that were not separated during the dicing process and thus remain together on a small silicon fragment. One of the diodes on one of these silicon fragments is used to perform several consecutive I(V) measurements, while the entire piece of silicon is moved between each individual measurement.

The same procedure is repeated with a second 200 µm thick diode, which is left over from the Hamamatsu campaign and which has been fabricated on a similar float zone base material as the PS-p. The resulting I(V) measurements obtained on both diodes are shown in figure 9.3.

Similar to the results of the wafer measurements, the first I(V) characteristics without any intentional scratches show the expected results without any breakdown up to 600 V. However, even small scratches after the first movements on the chuck lead to the undesired soft breakdown, which has already been observed with the PS-p. This applies to the diode on the PS-p wafer as well as the diode of the Hamamatsu campaign, shown in figure 9.4. With an increasing number of scratches to the backside, the I(V) characteristics deteriorates further and more and more resembles the behavior of the full-size sensor.

All measurements performed so far indicate that the problem of the soft breakdown is primarily related to the susceptible backside of the thinned wafer material, used by HPK. In order to validate this theory, further measurements of the PS-p have to be conducted that



(a) **(b)**

Figure 9.3.: Consecutive I(V) measurements of two scratched FZ200 diodes. Both diodes, one from the PS-p wafers (a) and one included in the HPK campaign (b) initially reveal good I(V) characteristics but show a soft breakdown behavior after scratching the aluminum backside multiple times on the chuck. The states 1 to 3 refer to three consecutive states with an equal degree of scratches between both diodes on the backside.

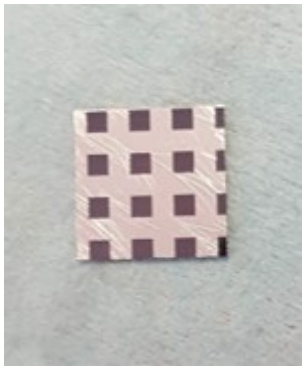


Figure 9.4.: Scratches on a diode of the HPK campaign. Even the small number of scratches shown here leads to a soft breakdown of the diode.

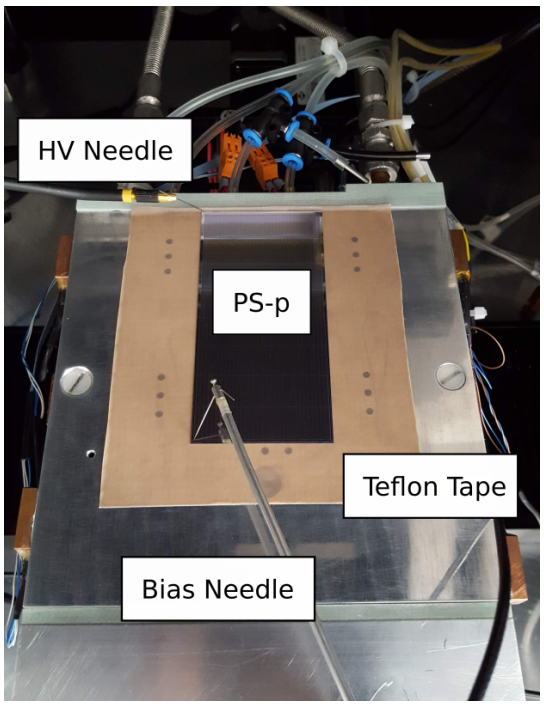


Figure 9.5.: Front-side biasing arrangement for the full-size PS-p. In order to protect the sensor backside, the full-size PS-p is placed on a protective Teflon tape and is biased through the sensor edge, using the frontside biasing approach.

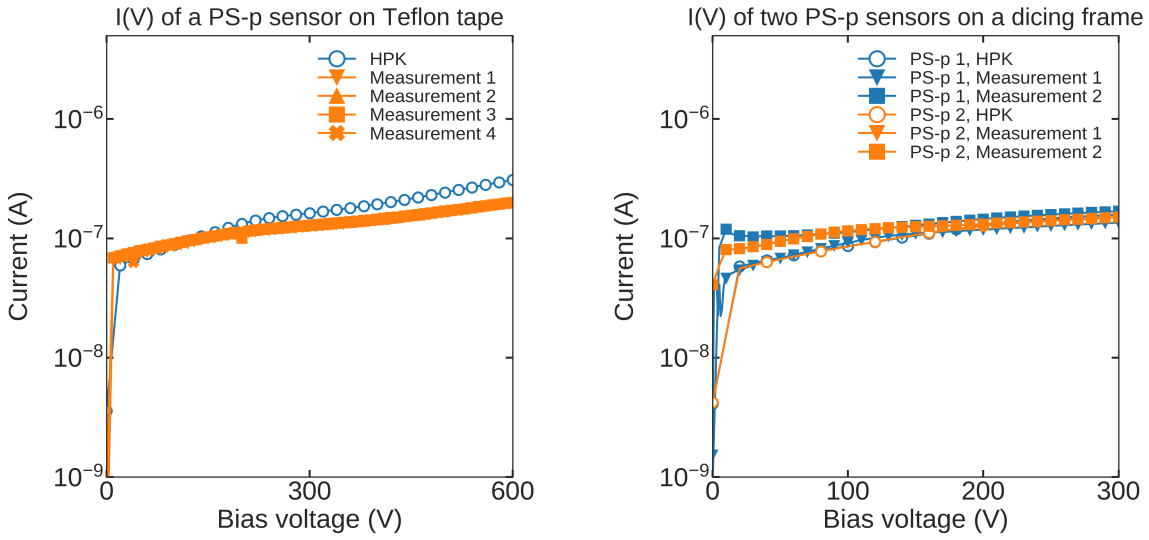
include an additional protection layer between the aluminum chuck and the sensitive backside. This is either realized by an additional Teflon foil that is glued on top of the probe station chuck or the self-adhesive protective foil of the dicing frame that some wafers are still attached to.

9.1.3. Insulated I(V) measurements

Scratches on the backside of the silicon sensors are most likely linked to small movements on the aluminum chuck of the probe station setup while handling the sensor before and after the measurement. However, by insulating the sensor backside from the probe station chuck, no bias voltage can be applied to the rear contact of the sensor anymore. Since the p^{++}-doped sensor edge, the p-bulk and the p^{+}-backside implant form a low-ohmic conductive channel at the edge of the sensor, the high voltage can also be applied to the frontside edge contact instead of the sensor backside, known as *frontside biasing* (FSB) [Bas+18]. At least for non-irradiated sensors, both methods lead to identical I(V) characteristics, whereas the results for irradiated sensors can differ quite considerably due to an increasing resistivity of the silicon bulk with increasing fluences [Bas+18]. The final setup, is shown in figure 9.5 and includes a protective Teflon foil on the probe station chuck as well as a second needle to contact the sensor edge for the FSB approach.

The corresponding I(V) measurements of several so far untested PS-p sensors, that are either already diced or still attached to the dicing frame are shown in figure 9.6.

In order to avoid any damage to neighboring structures, sensors that are still attached to the dicing frame have only be measured up to 300 V, which is still sufficient to detect a soft breakdown at the depletion voltage around 150 V. However, no breakdown has been observed after multiple repeating measurements over a period of several days on neither of the sensors.



(a) **(b)**

Figure 9.6.: I(V) measurements of the full-size PS-p using frontside biasing. In order to protect the sensor backside, the full-size PS-p is either placed on a protective Teflon tape (a) or is still attached to the dicing frame (b). In both cases, the sensor is biased through its edge, using the frontside biasing approach. In this setup, no soft breakdowns have been observed for multiple consecutive I(V) measurements of the full-size sensor.

In addition, no changes in the course of the I(V) characteristics are noticeable. Compared to the measurements done by HPK, some of the probe station measurements perform even slightly better than expected. Nevertheless, all these measurements strongly indicate that the problem of the soft breakdown is not related to the dicing process, but the susceptible backside that comes with the FZ200 material of HPK. After consultation, Hamamatsu confirmed that the backside of their thinned material seems to be more vulnerable than their deep-diffused material, which further supports the assumption. For that reason, it is strongly recommended to protect the backside of the sensors during the full assembly process.

9.1.4. Humidity dependence

While measuring another faulty full-size sensor with a slightly higher breakdown voltage than the damaged ones before, a noticeable shift of the breakdown voltage over time has been observed. The results of 10 consecutive I(V) measurements are shown in figure 9.7.

The temperature during all these measurements was fixed to 20 °C with a fluctuation of about ±0.5 °C. The only thing that changed over time was the relative humidity in the enclosure of the probe station setup, due to the dry air injection. The constant flow of dry air is intentionally used to lower the dew point inside the box and thus allows the sensor to be operated and tested at temperatures around −20 °C and below. However, it seems that this air flow and the resulting change of humidity in the box has a significant influence on the electrical properties of the sensor at room temperature. Although the leakage current does not change at all before the breakdown, the point at which the breakdown occurs shifts towards higher voltages with decreasing humidity. Since all observed breakdowns occur above the depletion voltage, the problem is most likely not related to the backside of the sensor, but might be caused by an

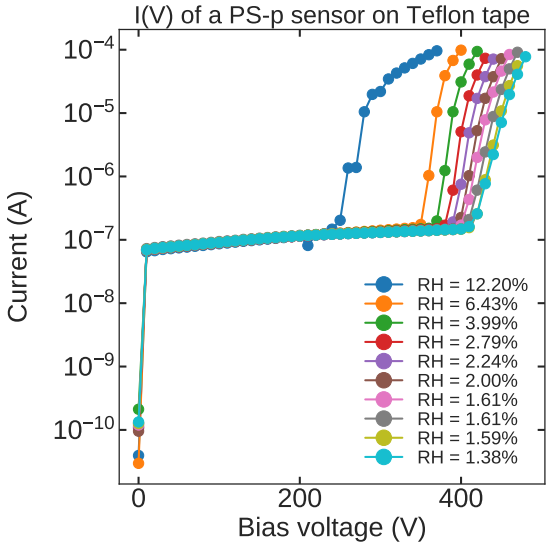


Figure 9.7.: Humidity dependence of the breakdown voltage of the full-size PS-p. Although the overall leakage currents remains the same for all measurements, the breakdown voltage is shifted to higher bias voltages with decreasing humidity in the probe station enclosure.

effect on the sensor surface or the silicon dioxide layer that is directly exposed to the ambient air and the humidity. This humidity dependence of the material has been verified by other institutes of the Outer Tracker sensor community and therefore excludes the possibility that this behavior is related to the probe station setup used at KIT.

The observed humidity dependence of the breakdown voltage is an undesirable effect, but can be accepted as long as the parameters still meet the requirements for the Outer Tracker of CMS.

9.1.5. C(V) measurements

The subsequent C(V) measurements are used to determine the depletion voltage of the sensor and the wafer material in general. This is done with the same needle setup while measuring the capacitance with an LCR meter at an increasing bias voltage. In order to protect the sensor and the equipment, C(V) measurements are usually limited to bias voltages below the breakdown voltage of the sensor. The results of two exemplary full-size sensors that are still attached to the foil of the dicing frame are shown in figure 9.8.

Both C(V) characteristics show a noticeable kink at about 150 V bias voltage, which corresponds to the full depletion V_{dep} of the sensors. This means that the soft breakdown observed in the I(V) measurements of some full-size sensors occurs exactly when the sensor gets depleted, or in other words when the space charge region reaches the backside of the sensor. This again supports the assumption of a sensitive backside of the thinned float zone material. What is unusual, though, is the fact that one of the two sensors shows an additional step towards higher $1/C^2$ values and thus lower capacitances. This step at about 260 V was never observed before, not even with the quite similar FZ200 material of the Hamamatsu campaign. However, almost all other PS-p sensors show this behavior. The first idea is directed towards so far unconsidered effects of the bias network and in particular the punch-through structures, which act as additional series capacitors between the backside of the sensor and the bias ring. For

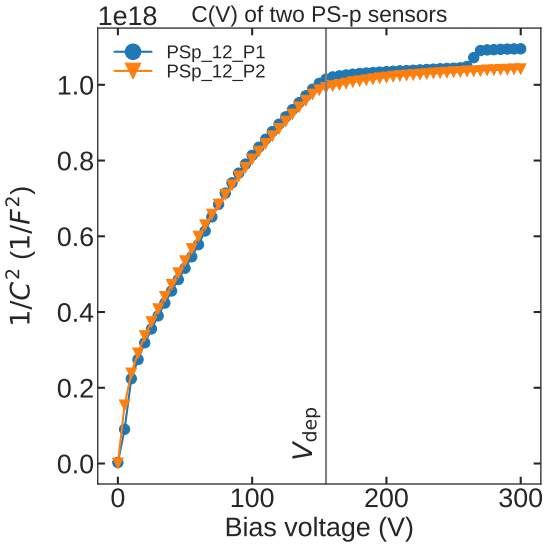


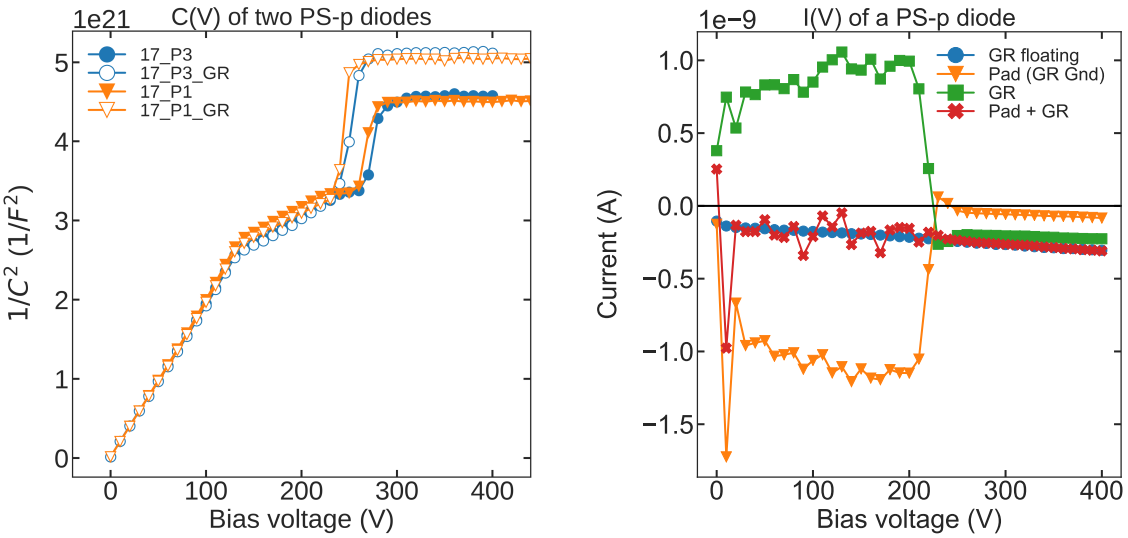
Figure 9.8.: C(V) characteristics of the full-size PS-p. The noticeable kink at about 150 V marks the point of the full-depletion voltage V_{dep}. The second step, seen on one of the two full-size sensors, indicates a sudden and unexpected decrease in capacitance.

this reason, additional C(V) and I(V) measurements with two diodes on the PS-p wafer were performed for comparison purposes. The results of these measurements are shown in figure 9.9a.

Solid markers correspond to a measurement with a floating guard ring, while the curve with hollow markers refers to a measurement with a grounded guard ring. All of these diode measurements show overall higher $1/C^2$ values than the full-size sensor. This is related to the smaller surface area of the diode compared to the macro-pixel sensors on the wafer. The first noticeable kink at about 120 V corresponds to the full depletion voltage V_{dep} and occurs slightly earlier than in the C(V) measurements of the PS-p sensor. The small deviation can be explained by the additional pixel geometry of the device and the associated lateral growth of the depletion region, which influences the course of the C(V) characteristics. As the measurement continues with increasing bias voltage, the $1/C^2$ value increases further up to the point at around 250 V where the capacitance suddenly drops and then stays constant. The constant linear increase after depletion and up to 250 V is very pronounced on diode measurements and is only barely noticeable during measurements on the full-size PS-p. Grounding the guard ring and probing the edge do not show any effect on the course of the measurement. Thus, lateral effects can be excluded at this point. The most plausible explanation aims at an additional, higher doped backside implant that gets depleted with increasing bias voltage. Unfortunately, however, no definite statement can be made at this point.

The pronounced step at around 250 V was already observed in the C(V) characteristics of some PS-p sensors and thus excludes the hypothesis of an influencing bias grid postulated at the beginning of this section. The fact that the total capacitance and the bias voltage at which the sudden drop occurs is affected by a grounded guard ring indicates that this effect is most likely related to the sensor periphery and not the backside of the wafer.

By looking at the I(V) measurements of one of the diodes on the PS-p wafer, shown in figure 9.9b, this becomes even more evident. Starting with a current measurement with a floating guard ring, no differences to I(V) measurements of the sensors can be observed. For an I(V) measurement with a grounded guard ring, however, the current on the pad is significantly



(a) **(b)**

Figure 9.9.: C(V) and I(V) characteristics of multiple diodes of the PS-p prototype wafer. The kink in the C(V) measurements (a) at 120 V marks the full-depletion voltage V_{dep} of the diodes. The sudden decrease of the capacitance at around 250 V resembles the behavior seen on some of the full-size PS-p sensors. By grounding the guard ring (hollow markers) the jump in capacitance is shifted towards lower bias voltages. The I(V) measurement of one diode (b) with a grounded guard ring (orange triangles and green squares) indicates that the diode pad and guard ring are short-circuited at bias voltages below 200 V, leading to a compensating current that is suppressed at voltages above 250 V.

increased at bias voltages below 200 V. At bias voltages above 200 V, the current starts to decrease again and follows the course of the typical I(V) measurement with a slight offset. The corresponding current that is measured on the guard ring shows a very similar behavior, but with opposite polarity at voltages below 200 V. Yet the sum of these two individual currents always equals the current that has been measured during the I(V) measurement with a floating guard ring.

This can be explained by a sudden insulation of the guard ring and the pad at a bias voltage around 200 V. At the beginning of the measurement, the pad and the guard ring are short-circuited by the presence of an electron accumulation layer at the silicon dioxide interface. Unlike in the pixel matrix, the accumulation layer is not interrupted by a p-stop isolation at this point. Even small differences in the electrostatic potential will therefore lead to a noticeable compensating current between the two structures if both are connected to an external potential. This is the case during diode measurements with a grounded guard ring. The comparably high currents with opposite polarity that are observed during these measurements correspond exactly to this compensation effect. This can be verified by summing the two individual contributions, which effectively eliminates the compensating current and reveals the previously measured bulk leakage current.

As the bias voltage increases, the two independent SCRs of the pad and the guard ring continue to grow together, thereby removing free electrons at the silicon dioxide interface until the entire accumulation layer is removed. From this point on, the pad and guard ring are insulated from each other. This immediately eliminates the additional compensating current and reduces the effective area of the SCR around the pad contact, resulting in the sudden drop in capacitance that has been observed during the C(V) measurement.

The same explanation applies to the C(V) measurement of the full-size PS-p. In this case, however, the effect is caused by the lack of p-stop isolation between the floating guard ring and the grounded bias ring instead of a pad. Nevertheless, since the pixel matrix is not involved in this process, performance is not expected to be affected by this effect.

9.2. PS-p single sensors

All further measurements have been performed on the remaining PS-p single sensors. These sensors are more easy to characterize due to their smaller size and the fact that they can be read out by a single MPA instead of 16 as the full-size sensor. The main objective of these measurements is to determine the influence of the different bias grid approaches on their electrical properties. In total, 40 of those single sensor have been tested, 25 of which have been used for the Single MaPSA production.

9.2.1. I(V) measurements

The I(V) measurements of the PS-p single sensors are performed without insulating the sensor backside and thus no frontside biasing is required. Figure 9.10 shows the I(V) characteristics of four single sensors that have been measured by Hamamatsu on wafer level and on one of the two probe stations at KIT after dicing. Each of these sensors represents one of the four design variants that have been implemented on the wafer.

All measurements done at KIT generally show lower leakage current but match well with the results obtained by Hamamatsu. At least three out of the four design variants show no soft breakdown up to 1000 V. The comparably low breakdown voltage of about 380 V of the common punch-through (CPT) sensor, which has been observed by Hamamatsu at slightly higher bias voltages, is reproducible and most likely related to the quite aggressive design of the sensor. Nevertheless, since the depletion of the sensors can be expected at around 120 V to

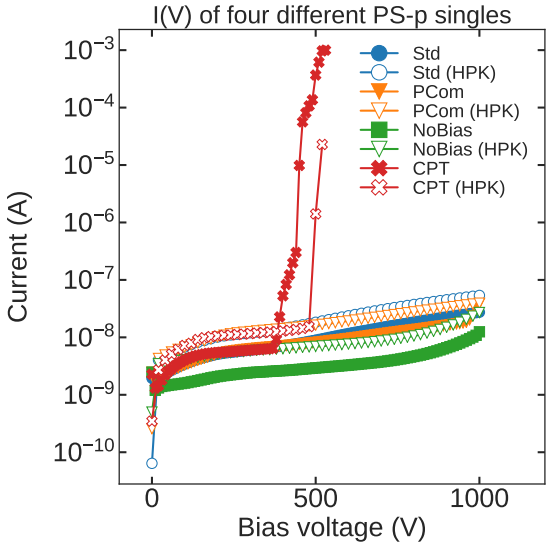


Figure 9.10.: I(V) measurements of the PS-p single sensors. Only the quite aggressive common punch-through layout (CPT) shows an early breakdown at around 400 V that has already been observed by Hamamatsu. The NoBias design shows a lower leakage current, which is related to the unbiased pixel cells due to the non-existing bias grid.

150 V, similar to the full-size PS-p and the diodes, the CPT can still be operated comfortably at bias voltages of 200 V to 300 V. The fact that the CPT sensor draws exactly the same current as the designs with individual punch-throughs demonstrates that the CPT approach seems to work properly.

The NoBias sensor on the other hand draws significantly less current than the other single sensors. Since the NoBias design does not feature any bias grid at all, the pixels cannot be grounded properly during the probe station measurements and the total leakage current is solely composed of the dark current that is drawn by the bias ring and some edge pixels that get grounded by the punch-through effect. The total leakage current of this sensor can only be determined when the sensor is connected to the MPA readout chip, which will provide the ground potential to the individual pixel cells.

9.2.2. C(V) measurements

Since all sensors are based on the same wafer material, it is expected that the shape of the capacitance-voltage measurements will be very similar to the full-size sensor and the diodes presented in the previous section. However, due to the different bias grid implementations, deviations may occur within the four different single sensor geometries. Figure 9.11 shows the result of four exemplary C(V) measurements of the same four singles sensors that have been used for the I(V) measurements.

Eye-catching is the already known step towards higher $1/C^2$ values between 250 V to 300 V. Since this phenomenon is noticeable across all four designs and especially during the measurements of the NoBias sensor, influences from the bias grid can be further excluded.

Compared to the measurements of the full-size sensor and the diodes, however, no pronounced kink is visible in the course of the $1/C^2$ measurements of the single sensors. While the shape of the $1/C^2$ characteristics of the Standard, PCommon and the common-punch through sensor

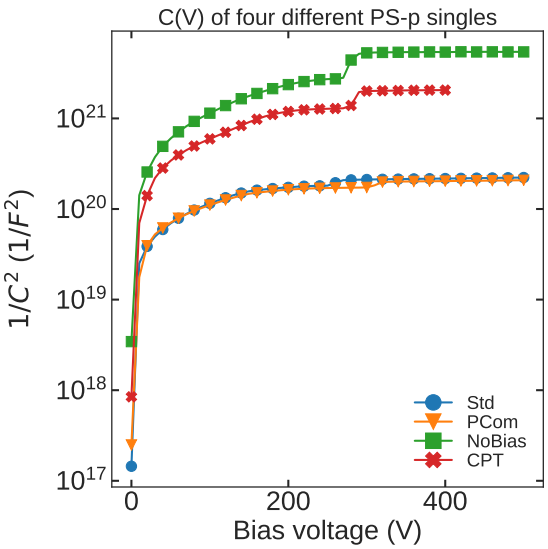


Figure 9.11.: C(V) measurements of the PS-p single sensors. The full-depletion voltage is hardly visible and can only be guessed between 150 V to 200 V bias voltage. The second step towards lower capacitances is independent of the sensor design and appears in all measurements. The total capacitance of the individual sensors is dominated by the number of PTS that are connected to the bias grid.

indicate a small kink at about 150 V to 200 V, the NoBias sensor does not show any full depletion up to the point when the step occurs. The lack of a bias grid makes it almost impossible for the depletion region to reach the pixels in the center of the matrix. Therefore, full-depletion of these sensors appears rather late without a readout chip bump bonded to them. As soon as the sensor is connected to a readout chip, full-depletion is expected at around the same voltage as for the other design variations.

By comparing the absolute value of the capacitances of the four sensors, the differences in their designs become apparent. The very similar design of the Standard and the PCommon sensor is reflected in the almost identical overall capacitance of the sensor. Both designs feature the highest number of punch-through structures on the sensor, since all pixels are equipped with their individual PTS to bias the pixel implant during testing. These PTS are connected in parallel and form a large capacitor that contributes to the overall capacitance of the sensor. The CPT sensor on the other hand substitutes four of those individual PTS with one common punch-through, which reduces the overall capacitance of the sensor and thus increases the $1/C^2$ values in the capacitance-voltage measurement. Providing no PTS at all, as in the NoBias design, results in the lowest capacitance and is further enhanced by the smaller active area due to the unbiased pixel implants in the center of the pixel matrix.

9.3. Infrared imaging

What is left is the question of why the full-size PS-p and some of the single sensors show a soft breakdown at bias voltages close to the depletion voltage. Every measurement up to now indicates that the problem is related to the sensor backside and therefore the wafer material itself that has been selected for this prototype. However, in order to exclude problems with the design and thus the need to change the mask set of the second batch PS-p prototype wafers, investigating the frontside is of great importance. One possible technique for making

problematic areas visible is *infrared imaging*. This technique is based on radiative recombination of electrons and holes in a semiconductor that leads to the emission of infrared light, which can be detected by a camera. The phenomenon of current-induced light emission in solids is known as *electroluminiscence*. The higher the current density, the more light is emitted. This means that local breakdowns or conductive channels on the surface of the sensor appear as bright spots in the infrared images, thus highlighting problematic sections that need further investigation. In the following section, infrared images of a Standard PS-p single sensor are presented and discussed in detail.

9.3.1. Infrared imaging setup

The main equipment for this kind of imaging is an infrared CCD[1]-camera, provided by a company called EHD imaging GmbH. The CCD-sensor of this camera consists of 3326×2504 pixels with a pitch of 5.4 µm whose brightness levels are encoded as 16 bit grey scale values. To reduce the thermal noise and increase the sensitivity of the CCD-sensor, the camera includes a built-in Peltier element that is used to cool the CCD-sensor down to temperatures around $-30\,°C$. The camera is added to one of the existing probe station setups, which provides all necessary equipment to operate the sensor during the imaging process.

The final result of the infrared image analysis includes two pictures: the infrared and the visible image of the device. By superimposing both pictures, the location of bright infrared spots and therefore sections with high current density can be immediately linked to structures on the silicon sensor. The visible image is obtained by taking a picture of the unbiased sensor while the setup is exposed to light. The infrared image on the other hand is acquired in the darkened setup and very long exposure times of the CCD-camera, while the sensor is operated above its breakdown voltage. In this operating mode, the location of the breakdown becomes visible in the form of bright spots in the infrared image. Both images are finally edited and superimposed using an image processing application, like the free and open-source GNU Image Manipulation Program (GIMP). In addition, the infrared image is transformed from the 16 bit greyscale palette to red, which will highlight all the areas with an increased current density. More details about infrared imaging and the setup, including the necessary objectives and the LabVIEW control software can be found in [Vor14].

9.3.2. Infrared images of a Standard PS-p single sensor

Instead of investigating a whole full-size PS-p sensors, the infrared imaging analysis is performed with one of the Standard PS-p single sensors that shows a noticeable soft breakdown at bias voltages below 300 V, shown in figure 9.12 This reduces the number of images that have to be taken to scan the entire sensor surface from about 50 to only 4 images. One of these final images of this sensor is shown in figure 9.13a.

The sensor is operated at a bias voltage of 300 V and an ambient humidity around 14 %. Two bright spots, which indicate high current densities along the bias and guard ring, are immediately visible. Problems in this region of the sensor are unexpected, as the well known geometry of the two rings already showed good results in the past. Since this design is considered to be rather robust against early breakdowns, the problem might be related to this specific sensor and not the design itself.

In order to investigate the humidity dependence of the sensor another set of images was taken at higher ambient humidity in the probe station enclosure. And indeed, looking at the superimposed picture again, taken at an ambient humidity of 35 % more spots appeared along the bias and guard ring as well as in the matrix, which could indicate a problem with the pixel

[1] Charged-coupled device

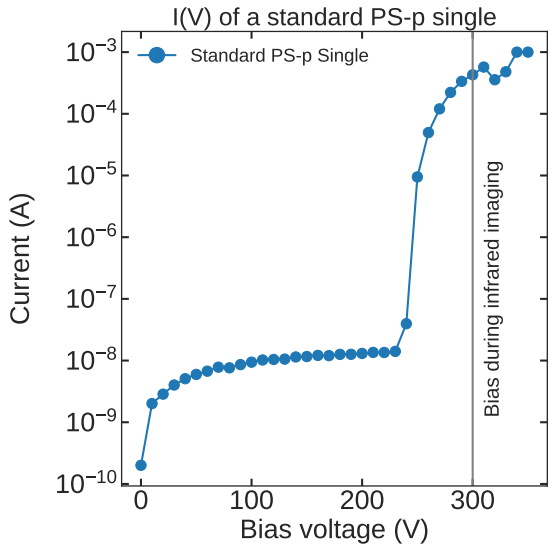
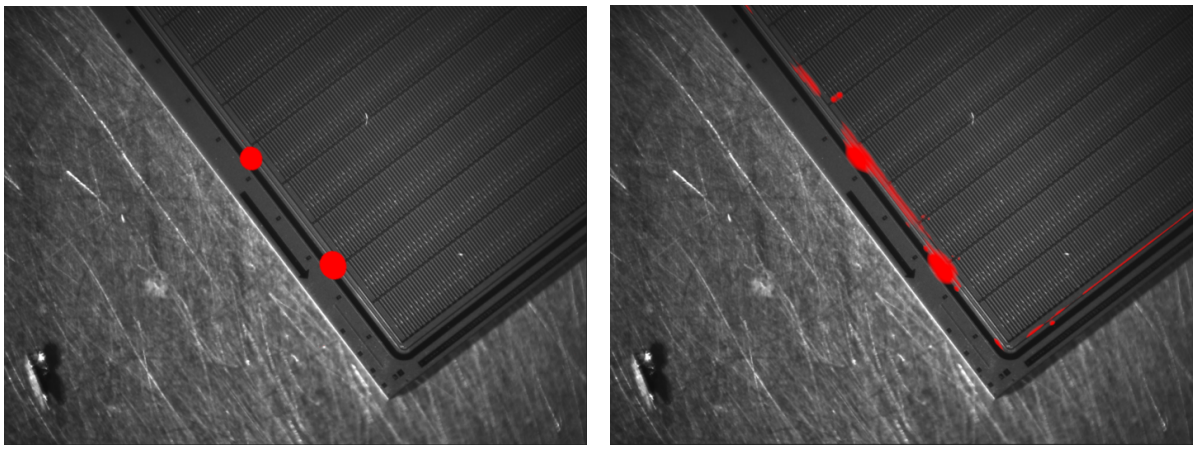
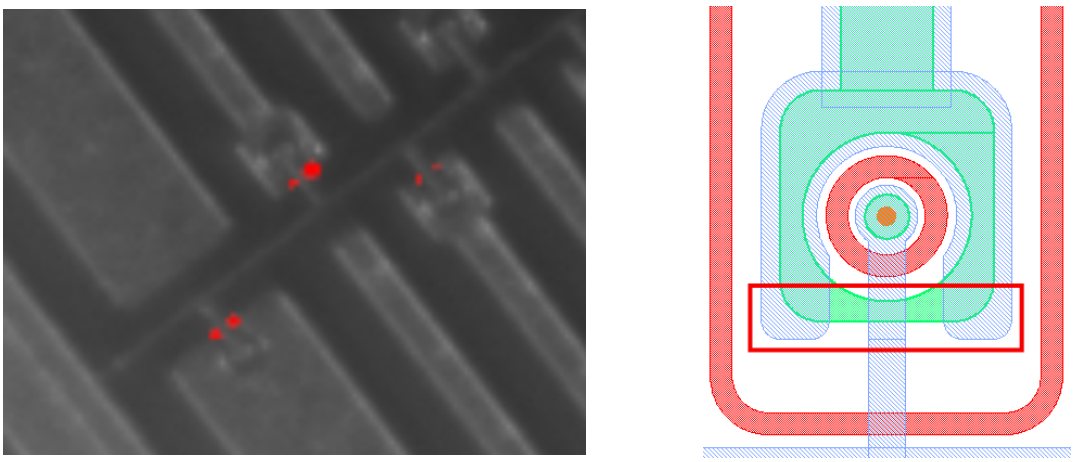


Figure 9.12.: I(V) of a Standard PS-p single used for the infrared imaging. The sensor shows a noticeable breakdown at bias voltages around 250 V. During the infrared image analysis the sensor has been operated at 300 V (gray vertical line).



(a) **(b)**

Figure 9.13.: Infrared imaging of a PS-p single sensor at different humidities. The sensor is operated at 300 V and above its breakdown voltage. Locations with high current densities are marked in red. At a relative humidity around 14 % only the guard and bias ring show two local breakdowns (a). At an increased humidity of approximately 35 % in the probe station enclosure, more areas along the periphery as well as parts in the pixel matrix get affected (b).



(a) (b)

Figure 9.14.: Close-up view of a PTS during the infrared image analysis. Each PTS shows two spots of a high current density (a). These local breakdowns appear close to the bias rail extension of the PTS and the crossing points of the aluminum layer (b, blue) and the pixel implants (b, green), which is marked with a red box.

design. A closer look at the pixel matrix reveals that the bright spots are always located at the PTS of the pixels. In fact, each spot in the pixel matrix that is visible in figure 9.13b is composed of two separated spots around the aluminum bias rail extension of the PTS, shown in figure 9.14.

A closer look at the mask layout of the PS-p reveals a small design flaw of the PTS: One of the most important design rule is the avoidance of sharp edges or crossing points between the individual structures. By looking at the PTS, which is shown in figure 9.14b, it quickly becomes apparent that the layout does not comply with this design rule. Several crossing points between the top aluminum layer and the pixel implant as well the p-stop ring are noticeable. The latter seems to be unproblematic in this case, but the transitions between the pixel implant and the aluminum pad as well as the small bias rail extension of the PTS show an increased current density in the infrared image. Another possible explanation for the high current density at this point could be some kind of surface current in the small gap between the rail extension and the PTS pad. However, similar to the periphery of the sensor, also the PTS geometry has already been tested successfully in the past and no such problem has been reported so far. Therefore, it is not yet clear whether this problem is caused by the layout itself or if the wafer material is affecting the behavior of PTS during the testing procedures. For that reason, the Outer Tracker sensor community decided to keep the PTS structure as it is for now and perform the same IR imaging analysis on the second batch of PS-p prototype sensors, which is expected in early 2019.

9.4. Concluding remarks

In this chapter, an electrical characterization of the first full-size PS-p sensor and its smaller single sensor derivatives on 200 µm float zone material was performed. During these measurements an increased susceptibility to scratches on the backside has been observed. Only if the sensors are handled with utmost care, the sensors keep their initially perfect properties that have been observed by Hamamatsu. Nevertheless, this kind of special treatment is unpractical during the module series production where the sensors are handled multiple times before

they get integrated in the their final module. In addition, a strong correlation between the breakdown voltage and the relative humidity has been observed. Furthermore, local spots of high current density close to the punch-through structure have been observed during the IR imaging analysis and high ambient humidity, which might require operation in a very well controlled environment.

In the end the Outer Tracker sensor community decided to choose the well known 320 µm thick wafer material for the second batch of PS-p prototypes, that has been extensively tested during previous production runs. Adding a moderate deep-diffused backside of 30 µm holds the promise to improve the robustness of the wafer backside and thus simplifies the handling of the sensors during testing and the production. However, switching to a thicker material will also change the power consumption of the sensor and thus the thermal properties of the entire PS module. Therefore, all changes have to be made in close agreement with the module design groups to estimate the impact on the thermal design of the module concept. At the same time a full electrical characterization of the material has to be performed again. This is necessary to see if the problem of the punch-through structures persists despite the change of the wafer material and if the material meets the requirements set by the Outer Tracker sensor community.

10 Measurements of the Single MaPSA

After the electrical qualification of the full-size PS-p and the single sensors described in the previous section, only the latter are used for further measurements to determine the performance of the PS-p prototypes. The single sensors have the advantage that they require only one readout chip instead of 16 that are necessary for the full-size sensor in order to build a fully equipped Macro-Pixel SubAssembly (MaPSA). For differentiation purposes, the assembly of a single PS-p and one readout chip is referred to as *Single MaPSA* from now on. Over 25 of these Single MaPSAs have been built and tested at KIT within the prototyping phase. The assembly procedure includes the gold-stud placement, the flip-chipping, the wire-bonding and the electrical characterization of all individual assemblies. Only a small selection of these prototypes has been used for the final efficiency measurements at the DESY test beam in Hamburg. These measurements were quite similar to the one with the PS-p light and the corresponding MaPSA light, which have been presented in Chapter 6. Finally, some of the assemblies have been irradiated with 23 MeV protons at the irradiation facility at KIT in order to accumulate the radiation damage expected after ten years of operation at the HL-LHC. These assemblies have also been characterized at the DESY test beam, which provides valuable information about the expected performance of the detector at the end of its runtime. All the individual steps, assembly, testing, irradiation and the final test beam measurements are presented in detail in the following.

10.1. Building Single MaPSAs

Building the Single MaPSA is the first step towards the efficiency study of the various sensor designs that are implemented on the PS-p prototype wafer. Therefore, a number of Macro Pixel ASICs (MPAs) are required that have to be provided by the chip developers. However, since the first MPA prototypes arrived approximately at the same time as the PS-p prototype sensors, only a small number of chips was available at that point of time. Most of these chips were dedicated to the chip developers and their extensive testing procedure to verify all functionalities of their first full-size prototype. In addition, none of the chips were equipped with any kind of under bump metallization and bump bonds, which excluded any conventional bump bonding technique at that point of time. Since the sensors have not been post-processed either, gold-stud bump bonding at KIT was again considered as a possible alternative to the conventional approach. For that reason some of the unprocessed and untested chips were sent to KIT to produce the first Single MaPSAs on a much shorter time scale than the initial plans of the community. These assemblies serve as first prototypes for the sensor designers, the chip developers to validate the individual components and the readout chain.

10.1.1. The Macro Pixel ASIC (MPA)

The Macro Pixel ASIC (MPA) is the full-size successor of the MPA light prototype that was used for the PS-p light assemblies. With a size of 25.2 mm × 11.9 mm and a matrix of 118 × 16

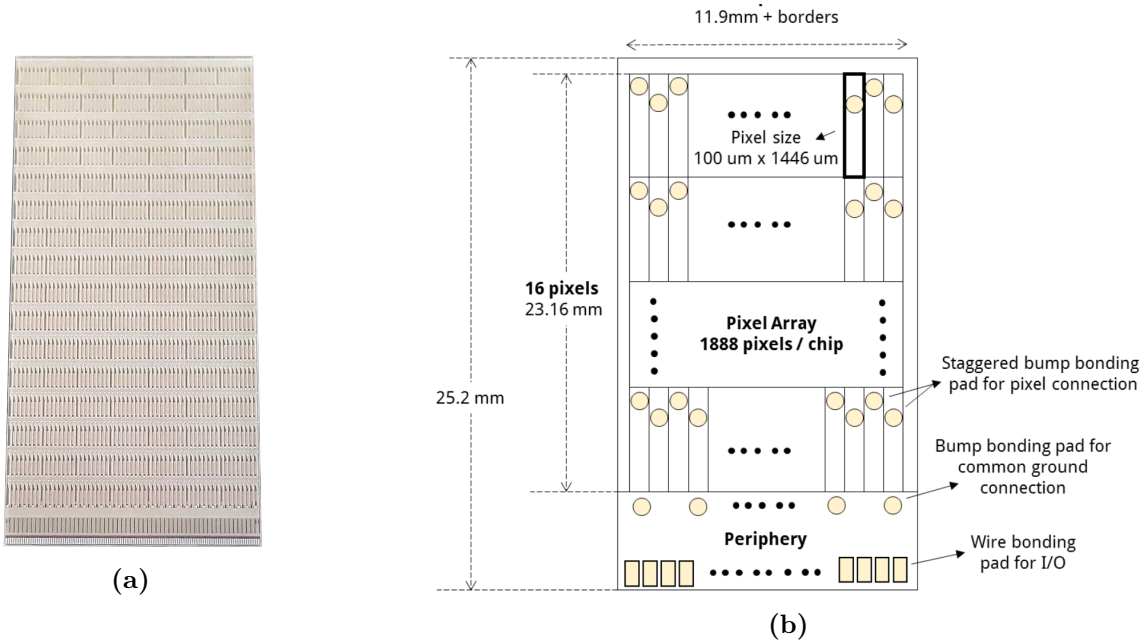


Figure 10.1.: Picture of the Macro Pixel ASIC (a) together with a schematic including its dimensions and electrical connections, also known as *floor plan* (b) [Cer+17].

front-end channels instead of only 16×3, the MPA comprises almost 40 times as many pixel cells as its predecessor prototype. The pitch between the staggered bump bond pads remains unchanged at $1446\,\mu m \times 100\,\mu m$ and is therefore slightly smaller than the pitch on the sensor side ($1467\,\mu m \times 100\,\mu m$). A schematic of the electrical connections as well as a picture of the MPA are shown in figure 10.1.

The MPA is a binary chip with three different acquisition modes: one asynchronous and two synchronous ones. Each of these acquisition modes are enabled individually and can be operated simultaneously. However, only the synchronous readout modes provide the necessary data for the L1 and the stub data paths that have already been introduced in section 3.2.5.

The complete binary readout schematic of the MPA is illustrated in figure 10.2. The starting point of all three acquisition modes is the discriminator output in the analog front-end (FE), which switches to 1 as soon as the shaper output exceeds the threshold of the chip. In order to achieve an asynchronous readout, every pixel cell of the chip contains a 15 bit ripple counter, which simply counts every rising edge of this discriminator output. This is the same asynchronous mode as for the MPA light. In order to start the asynchronous acquisition of the ripple counters, an internal shutter has to be opened, which can be controlled via a *fast command* interface of the chip. As soon as the shutter is closed and the readout is initiated, the data can either be read out via I2C or the stub data line. The asynchronous readout is exclusively used during calibration and testing procedure of the chip. For the actual operation and data acquisition in the test beam, one of the two synchronous readout modes is used. The two modes mainly differ in the first stage of their digitizer that is either *edge* or *level* sensitive. The difference between the two lies in the number of 1s (HIGHs) that their 40 MHz sampled output generates per discriminator pulse, which is illustrated in figure 10.3. The edge sensitive detector produces a single 1 for the duration of one clock cycle as soon as the analog signal crosses the threshold level and the discriminator generates a pulse. The level sensitive detector on the other hand stays HIGH as long as the signal remains above the threshold. Both output signals are sampled *synchronously* to the 40 MHz clock of the chip, leading to a sequence of 1s and 0s with a 25 ns spacing.

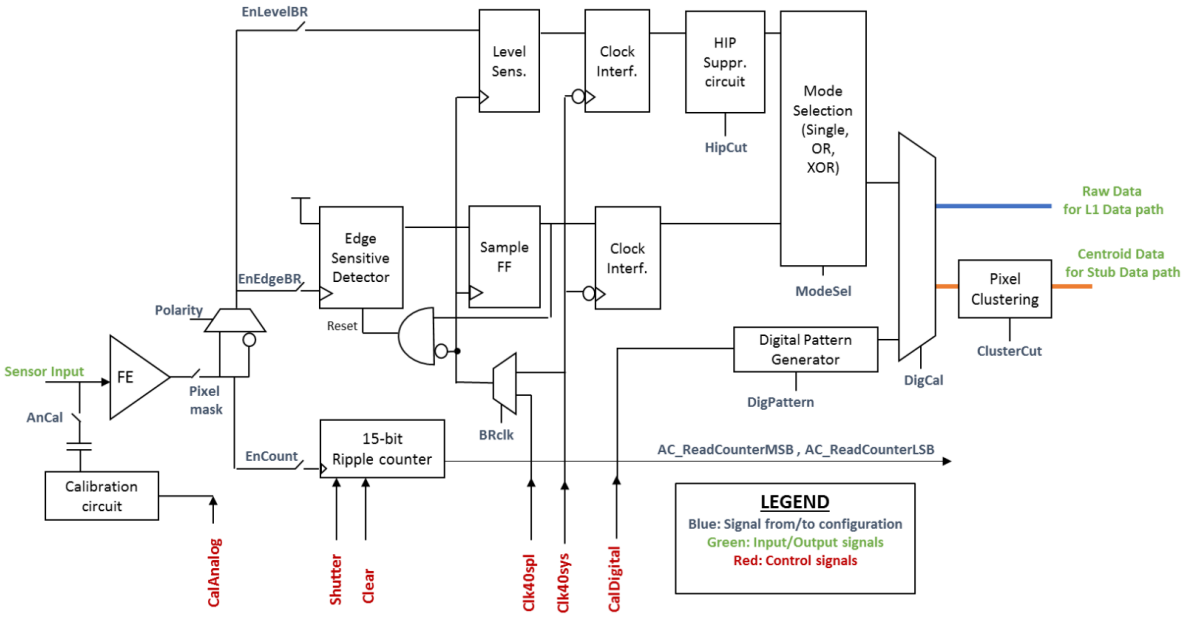


Figure 10.2.: The MPA binary readout schematic. The signal of the analog front-end (FE) can be processed by three different acquisition circuits: the edge and level sensitive synchronous readout paths (EnLevelBR and EnEdgeBR) as well as the asynchronous ripple counter (EnCount). The input signal is either provided by the attached sensor or the calibration circuit [Cer+17].

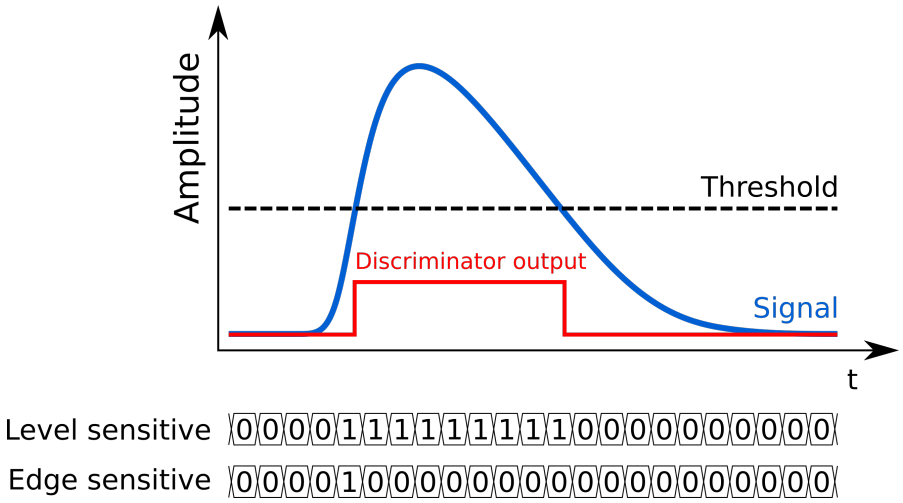


Figure 10.3.: Schematic of the level and edge sensitive readout mode. In level sensitive mode, the output of the binary readout stays HIGH as long as the signal (blue) is higher than the threshold. In edge sensitive mode, the binary output only goes HIGH for one clock cycle when the signal crosses the threshold, triggering a pulse on the discriminator output (red).

In case of the level sensitive mode, an optional highly ionizing particle (HIP) suppression circuit is added to the chain. A HIP generates a signal in the sensor that keeps the output signal of the level sensitive detector HIGH for many consecutive clock cycles. The HIP suppression circuit forces the output to go down to 0 after 1 to 7 consecutive clock cycles, which can be set in the *HipCut* register of the chip. The output of the level and edge sensitive data path can be used exclusively or combined via a logical OR or an exclusive OR (XOR) circuit. In the last step, the data is split and prepared for transmission to one of the 16 L1 row memories as well as the stub data path.

Each L1 row memory consists of a static random-access memory (SRAM) circuit that stores the data of all 118 pixels in one row of the chip. It can store up to 512 events with a length of 128 bit, which accounts for a maximum L1 trigger latency of 12.8 µs. As soon as the chip receives a trigger signal, the event with the correct trigger latency in the memory is selected and sent to the periphery. The chip periphery collects the data of all 16 L1 row memories and prepares it for the final transmission. If no trigger is received within 12.8 µs, the event is discarded.

Due to large size of the MPA, the bias structure of the chip is split seven individual *bias blocks* that power 16 or 18 columns at once. Each bias block includes six 5 bit digital to analog converters (DACs) that are used to adjust the analog front-ends of the pixels that are powered by the individual block. The adjustments include several voltage levels and bias currents for the analog components of the front-end (feedback and preamplifier) as well as some reference values of the digital part of the chip. An additional multiplexer in each bias block allows to probe the voltage levels of the individual DACs on an external I/O pad and to adjust them properly. A schematic of the MPA bias blocks is shown in figure 10.4 [Cer+17].

10.1.2. The Single MaPSA

In order to build a Single MaPSA, one MPA has to be bump bonded to one single PS-p. The first Single MaPSA prototypes are built in close cooperation between the Institute for Data Processing and Electronics (IPE) and the Institute of Experimental Particle Physics (ETP) at KIT. The basic principles of gold-stud bump bonding used for this process are the same as for the PS-p light and have already been introduced in Section 5.6.2. However, while the gold-stud placement is easily scalable with the chip size, the alignment of the two dice for the flip-chip processes became quite challenging. For that reason, several assemblies with non-active (dummy) material have been produced before processing the active material to optimize the alignment procedure and the bonding process. Each of the final Single MaPSAs is glued and wirebonded to a dedicated carrier board that features an industry standard PCI-e x16 connector, which provides enough electrical traces to address all 118 pins of the MPA. One of the wirebonded Single MaPSAs is shown in figure 10.5.

In total, 25 of these Single MaPSA assemblies have been built at KIT and were distributed among the various institutes and developer teams. Nearly 50 % of them are intended for the sensor design study alone, which is presented in the following.

10.1.3. Test setup

In order to communicate with the Single MaPSA on its carrier board, a dedicated readout system has to be used. Similar to the PS-p light readout system, the Single MaPSA setup also consists of an FPGA based acquisition board and a custom made *interface board*. The interface board was again developed by Rutgers University in the United States and houses several voltage regulators that provide all necessary voltage levels to the MPA. An additional ADC on the board is supposed to measure the various voltage levels of the bias blocks during

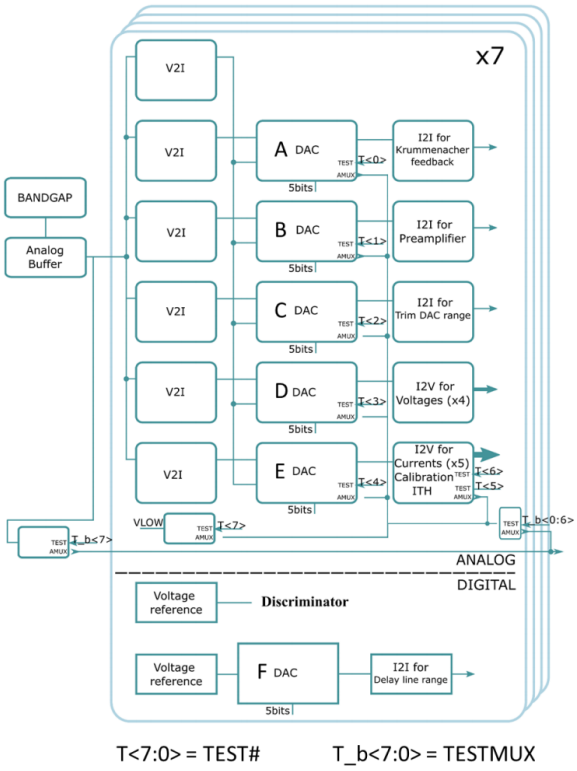


Figure 10.4.: Illustration of the MPA bias structure. The bias structure is split into seven individual bias blocks that can be calibrated independently. Each bias block includes six digital to analog converters (DACs) that are used to adjust the output currents and voltages for the analog front-end [Cer+17].

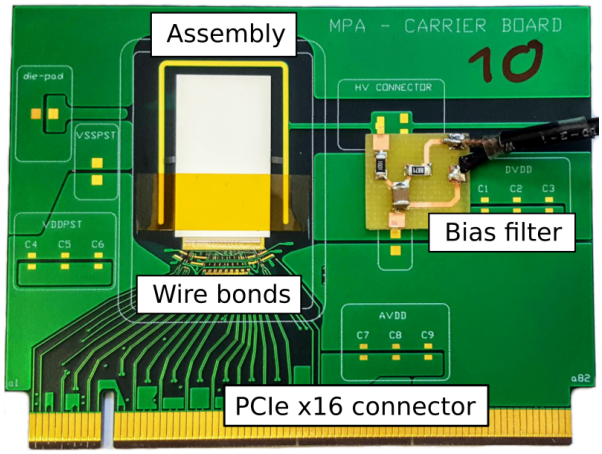


Figure 10.5.: Picture of the Single MaPSA on a carrier PCB. The assembly is placed with the sensor backside facing upwards on a gold-plated ground pad and fixed with a polyimide tape. Each I/O pad of the MPA is wirebonded to its dedicated traces on the PCB, which is routed to the PCI-e connector. The sensor backside is wirebonded to a U-shaped bias contact that is connected to the external power supply through a low-pass filter for noise reduction.

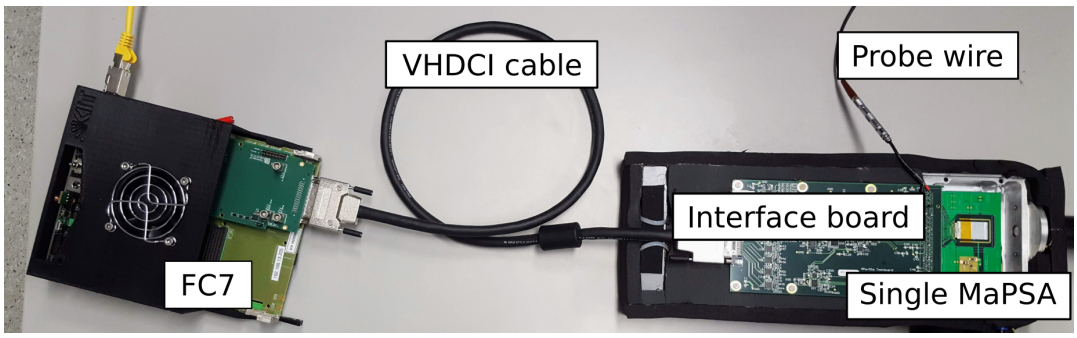


Figure 10.6.: The Single MaPSA test setup. The Single MaPSA on its carrier board is plugged into the PCI-e connector on the interface board, which provides all necessary voltage levels to operate the MPA. The interface board is connected to the FC7, which is used to control and read out the MPA. The FC7 uses an Ethernet connection to send and receive data from the connected readout PC.

the calibration procedure, which is necessary to ensure homogeneous biasing of the front-ends across the entire chip. However, since the ADC on the board is not working properly, an additional wire is soldered to the board, that picks up the probe signal, which is measured with an external voltmeter during the calibration procedure. A small design flaw in the trace mapping of the carrier board required re-soldering the straight PCI-e connector of the interface board to its backside and adding an additional 90° raiser adapter to ensure the correct position of the carrier board for the test beam measurements.

On the other end, the interface board uses a high density 68-pin VHDCI cable to connect to the GLIB's successor evaluation board: the FC7. The FC7 is a versatile μTCA compatible Advanced Mezzanine Card (AMC) for generic data acquisition and control applications. The board is designed around the Xilinx Virtex-7 FPGA and features two FPGA Mezzanine Card (FMC) connectors for user I/O. In order to avoid the use of a bulky μTCA crate, the FC7 is plugged into a custom made adapter card, designed by Imperial College London, UK, which provides one SFP+ cage, equipped with an Ethernet module that is used to connect the FC7 with a readout PC. The FC7 is driven by firmware developed by the the Outer Tracker community, which is able to read out all chips used in the Outer Tracker of CMS (CBC, SSA, MPA, CIC). The final Single MaPSA readout system is shown in figure 10.6.

10.2. Calibration of the assembly

The first step of the qualification process is the calibration of the chip. This ensures that the response of each pixel on the chip to the generated charge in the sensor is the same. The calibration procedure includes the equalization of the seven individual bias blocks and the adjustment of the threshold of the individual front-ends. The latter routine is called *trimming* and is necessary to compensate for small deviations in the front-end electronics that occur during the production process. The bias calibration and trimming results are unique for each assembly and should be determined at least once. All values can be saved to a file and reapplied whenever the chip is power cycled. In order to upload the individual calibrations to the eight chips of one hybrid in the final module, each MPA provides a dedicated 3 bit register to which a chip number is assigned by wire bonding certain pads of the chip to ground potential. Since the final module will provide two independent I2C bus systems all 16 MPAs per module can be addressed.

10.2.1. Calibrating the bias blocks

Calibrating the bias blocks of the MPA is essential to ensure a proper power distribution across the entire chip. This is done by setting the individual DACs of the bias blocks to a default value, comparing the respective output voltages with the target values and adjusting the DACs accordingly. The output voltages are measured by an external voltmeter that is connected to the additional cable soldered to the interface board, which replaces the faulty ADC on the board. Since the voltmeter is controlled and read by the calibration software, the entire calibration process is fully automatic.

10.2.2. Trimming of the analog front-end

There are two different reference values that can be used for the trimming procedure of the individual analog front-ends of the MPA: the noise level and an injected test signal. The latter is generated by an internal calibration circuit, which is built into each pixel cell. This circuit uses an 8 bit DAC to charge a small capacitor and subsequently injects the stored charge into the analog front-end. The higher the injected charge, the easier it gets for the resulting signal to exceed the global threshold of the chip. By comparing the number of registered hits at different threshold values for a fixed signal height with the total number of injected signals, the response behavior of the individual pixels can be determined and adjusted. At lower thresholds, all signals are detected and the ratio between injected signals and registered hits will always be 1. As the threshold value increases, fewer and fewer signals exceed the threshold until none of the signals is detected anymore. Scanning over the entire threshold range results in a so-called *S-curve*. In case the noise level is used as reference, no signal is injected into the analog front-end and only a threshold scan is performed. At low thresholds, the noise is constantly generating hits in the front-end, which decreases with increasing threshold until the chip no longer detects any noise hits. Plotting the number of registered hits over the threshold again leads to an S-curve similar as before. The midpoint of this S-curve, where 50 % of the noise hits are detected, is called the *pedestal*. In the ideal case, the pedestal of every front-end is located at the same threshold value. However, due to the already mentioned deviations during the lithographic process, the pedestals are spread across a certain part of the threshold range. An illustration of three S-curves with slightly different pedestals are shown in figure 10.8

The MPA uses the 5 bit TrimDACs of each pixel cell to adjust the individual front-end thresholds by moving the pedestals to a common user-defined threshold value. The maximum spread of the pedestals defines the necessary TrimDAC range that has to be set in the seven bias blocks (DAC 'C' in figure 10.4). The higher the range, the easier it gets to move pedestals with greater deviation to the common threshold value. A smaller range, on the other hand, leads to a smaller step size and thus to a more precise trimming in the end. For this reason the TrimDAC range should be as small as possible and at the same time large enough to adjust as many front-ends as possible.

When the trimming is completed, a second threshold scan with test pulses might be performed to validate the trimming result and perform a final fine adjustment. For the MPA and its asynchronous readout, which is used for this calibration procedure, a very unique response behavior is created by this scan. Figure 10.8a shows the number of entries in the counter for a single pixel for different threshold values, which are given in steps of the least significant bit (LSB). The sensor of the assembly has been operated at a bias voltage of 200 V to reduce the noise by thermally excited charge carriers in the sensor, which would impair the result of the scan. Starting at very high thresholds, no signal exceeds the chip threshold and thus no hit is detected. As soon as the threshold gets low enough for some of the injected signals to exceed it, the number of detected signals increases with an S-curve shaped turn-on curve. As

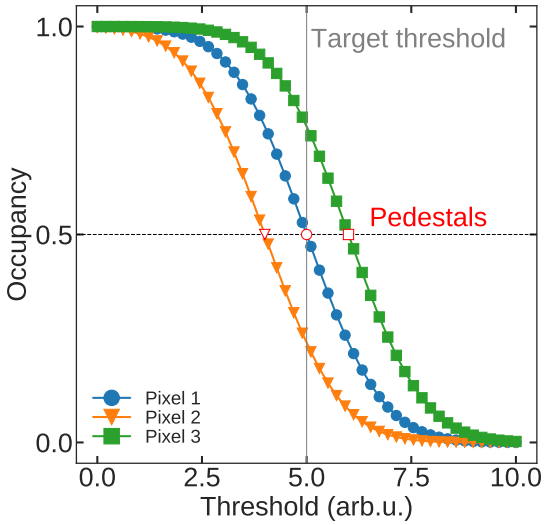


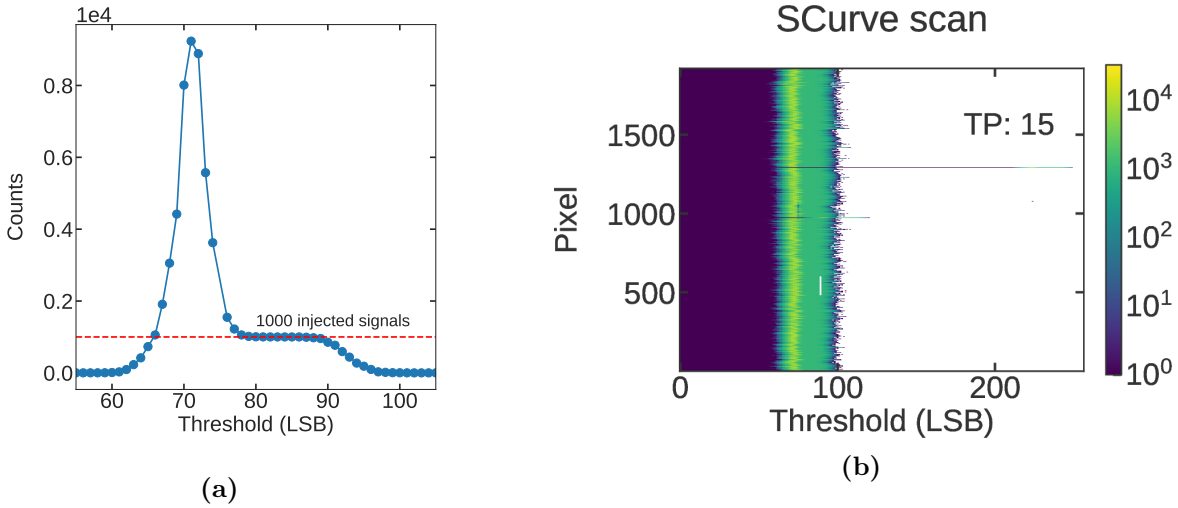
Figure 10.7.: Illustration of three exemplary S-curves with different pedestals. The pedestals of two of them do not match the target threshold of 5 arb.u. and thus need to be trimmed.

long as the threshold stays well above the noise level, the number of detected hits in the ripple counter equals the number of injected signals. However, when the threshold reaches the noise level, not only injected signals but also random noise hits are detected by the asynchronous readout circuit, leading to an increased number of registered hits in the ripple counter. With decreasing threshold, the number of entries in the counter increases further until the point where the number of detected hits decreases again. This behavior is caused by the fact that the ripple counter uses an edge sensitive detector and thus only increases its value when the signal crosses the threshold. As the global threshold decreases to very low values, the signal remains above the threshold more and more frequently and therefore does not increase the counter anymore. This ultimately leads to the point where the signal exceeds the threshold only once at the beginning of the data taking and stays above it from then on, which leads to exactly one registered hit in the ripple counter.

Figure 10.8b shows the final result of the trimming procedure of the first assembly that was built at KIT, operated at 200 V bias voltage. The trim target was set to 70 LSB and the test pulse amplitude for the verification and the fine adjustment was set to 15 LSB. Since the step size of the test pulse DAC and the threshold DAC are not the same, the S-curves with a test pulse are not necessarily expected at a threshold value of 85 LSB. The color gradient of each row in the two dimensional plot represents the S-curve of one front-end on the chip. The noise peaks as well as the falling edges of the S-curves of almost all pixels are well aligned and thus ensure a uniform response behavior of the entire chip. The final trim values of the chip are saved in a dedicated text file and can be uploaded to the chip whenever necessary.

10.2.3. Sr90 measurements

When the bias blocks are calibrated and the front-ends are trimmed, the Single MaPSA is ready for data taking and the last qualification step. In order to verify the existence of the conductive bump bond interconnections between the sensor the MPA, charge has to be generated in



(a) **(b)**

Figure 10.8.: Trimming results of a Single MaPSA using 1000 test pulses with an amplitude of 15 LSB at a trim target of 70 LSB. The response behavior of a single channel (a) features the characteristic noise peak at around 70 LSB and the S-curve beginning at 90 LSB. The overall trimming result of the entire chip (b) is very homogeneous and shows only few channels that could not be trimmed properly.

the biased silicon sensor, which is subsequently read out by the analog front-end. If the interconnection is broken, no signal is detected and the pixel is dead.

Therefore, a signal is generated within the sensor, using an electron emitting radioactive Sr^{90} source. The ripple counter of each front-end counts every rising edge of the signal and thus detects every particle traversal during the data acquisition time. The hit maps of two exemplary assemblies with very different bump bond quality are illustrated in figure 10.9.

The assembly presented in figure 10.9a is severely affected by missing bump bond connections that are most likely related to uneven gold-studs that occurred on the first few assemblies that were processed on a different machine than the rest. Figure 10.9b, on the other hand, shows a perfect assembly without any missing bump bond connection. Generating these *hitmaps* is the last step of the qualification process of the Single MaPSAs. Only the most promising assemblies with the best trimming results and the highest number of pixels connected to the chip are considered for the final sensor design study at the DESY test beam. About 15 out of 25 assemblies are rated very good, which means that only five or fewer pixels in the whole matrix are disconnected or outside the trimming range. In addition, no faulty readout chip has been identified up to this point and all assemblies seem to be operational.

10.3. Beam test at CERN and DESY

In order to determine the performance of the various Single MaPSAs, several test beam studies have been performed in 2018. The first one was carried out in April at the SPS test beam facility at CERN. At this point, the MPA was still evaluated by the chip designers and no beam data had been recorded with it so far. This beam test was conceived as a joint effort of the chip designers, the firmware developers and the sensors designers to generate beam data with the first Single MaPSA prototype. Thus no detailed sensor studies had yet been conducted at this point. Although most of the results that are presented in the following are generated at the DESY test beam facility, some of the results of the CERN beam test are shown as well. Since both facilities provide the same type of EUDET type telescope and DAQ chain, the differences

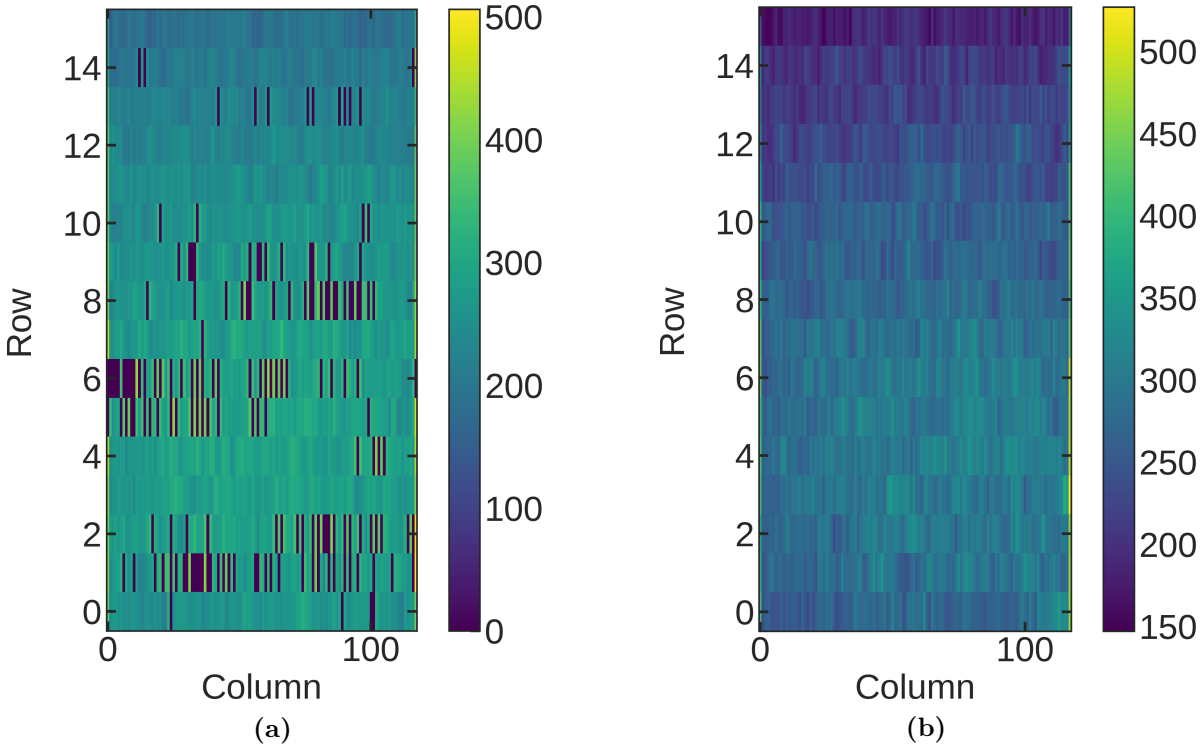


Figure 10.9.: Sr^{90} hitmap of two Single MaPSAs. The first few assemblies (a) show a significant number of dead pixels that are most likely related to uneven gold-stud bumps on the chip or/and the sensor. However, the majority of assemblies show no or only few missing bump bond connections (b).

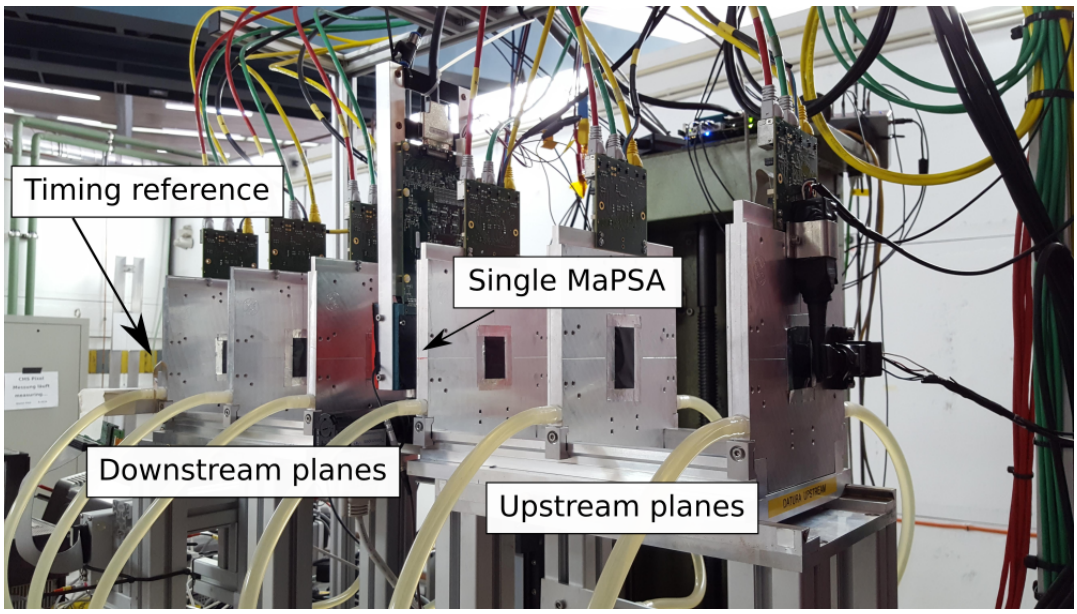


Figure 10.10.: Single MaPSA test beam setup at DESY. The Single MaPSA (DUT) is mounted on two movable and one rotational stage between the three upstream and three downstream planes of the DATURA telescope. The CMS pixel timing reference is placed behind the last downstream plane.

between the two are essentially limited to a different timing reference plane and the type of particles, their energy and their rate. Therefore, only the setup used at the DESY test beam facility is described in the following.

10.3.1. The test beam setup

The Single MaPSA test beam setup is very similar to the one used during the MaPSA-light beam test presented in Chapter 6 and is shown in figure 10.10. The Single MaPSA test setup, including the interface board and the Single MaPSA on its carrier PCB, is mounted on two movable and one rotational stage in the middle of the DATURA telescope between the three upstream and three downstream planes. The interface board is connected to the FC7 board, which in turn is connected to the local Ethernet network. The FC7 performs a full trigger data handshake with the TLU via a custom-made adapter box, which converts four LEMO cables from the FC7 into a single RJ45 connector, which is connected to the TLU. Instead of a small single chip assembly, a full-size pixel module of the CMS Pixel Phase-I Upgrade detector [CMS12a] is used as reference detector behind the last telescope plane. Similar to the full-size MaPSA, the CMS pixel module is equipped with 16 instead of only a single readout chip and thus covers the full geometrical acceptance window of the telescope easily. Since the long side of Single MaPSA is mounted perpendicular to the long side of the MIMOSA 26 this is also partly true for the Single MaPSA itself. With a size of about 12 mm × 25 mm, only up to 6 to 7 of its 16 rows are covered by the overlapping geometrical acceptance of the telescope, the scintillators and parts of the reference plane. For the entire analysis, x is defined along the short (100 µm) pitch of the assembly, whereas y runs along the long edge (1467 µm) of the pixels.

10.3.2. Data acquisition system

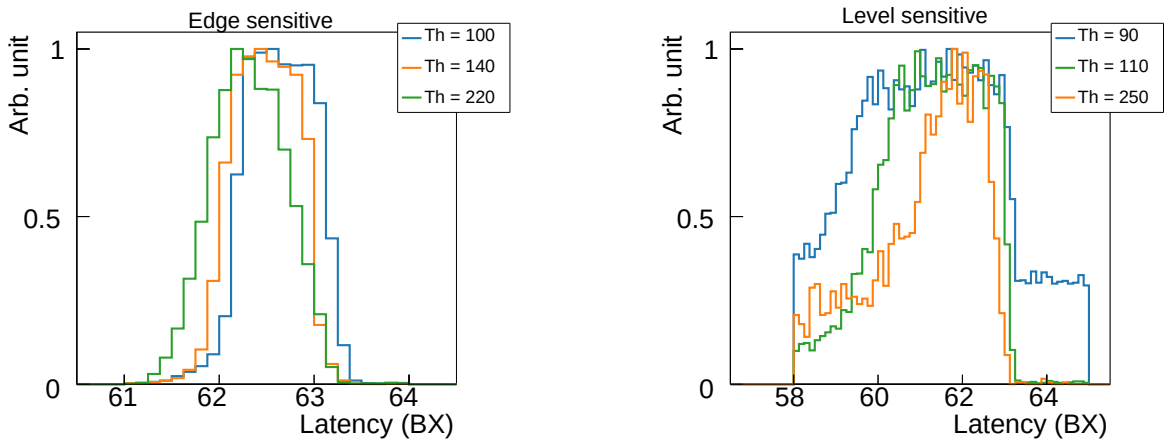
The trigger chain of the system is very similar to the one used at the MaPSA-light beam test. Four scintillator and PMT assemblies serve as input for the TLU. If all four PMTs are firing within a defined correlation window, a trigger signal is generated and distributed to the telescope, the reference plane and the Single MaPSA setup. The data of the Single MaPSA is then saved on the FC7 until the DAQ software reads it from the FPGAs memory. The entire DAQ system is based on the EUDAQ framework, which has been introduced in Chapter 6. In contrast to the MaPSA-light beam test, however, all data is stored in the common *.raw* file that is generated by EUDAQ's Data Collector and then processed by the EUTelescope framework. To achieve this, a Python script is used, which reads the data from the FC7, connects to the Run Control and sends the data to the global Data Collector. From this point on, the entire setup is fully controlled by the Run Control. This also enables the possibility to use the built-in Online Monitor to align the setups in the beam and to verify data synchrony during data taking by monitoring the correlation between the various data streams.

10.3.3. Latency scan

After calibrating the bias blocks and trimming the Single MaPSA to the nominal threshold value of 77 LSB, the latency between the particle and the arrival of the trigger signal in the readout chip has to be determined. This latency is given in steps of 25 ns, which corresponds to one bunch-crossing (BX) of the LHC. This value is stored on the MPA and defines the memory address that has to read to retrieve the data of the particle passage. In addition, the sampling time of the signal can be fine-adjusted in steps of 3.125 ns, by changing the phase of the 40 MHz sampling clock with respect to the internal 320 MHz driver clock of the FPGA. These finer steps are given in units of a *Time to Digital Converter* (TDC) and stored on the FPGA itself. In order to find the optimal latency at which the signal pulse reaches its maximum, a latency scan has to be performed. The result of this scan depends on whether the chip is operating in level or edge sensitive mode during the data acquisition. Since the particle arrives randomly in time and the trigger signal of the TLU is not synchronized with the 40 MHz clock of the MPA, the result is blurred within one clock cycle of 25 ns. Figure 10.11 shows the results of multiple latency scans at various thresholds for each readout mode at the CERN test beam.

Each plot shows the number of events with registered hits normalized to the number of entries of the highest bin for three different threshold values. Figure 10.11a shows the result of the latency scan in edge sensitive mode and figure 10.11b in level sensitive, respectively. In both cases, the result of the latency scan depends on the threshold of the chip. In edge sensitive mode, where exactly a single 1 is generated for one clock cycle at each particle passage, the width of the distribution is determined solely by the uncertainty of the particle arrival. With higher threshold, the distribution is shifted towards lower latency values, due to the *time walk* of the front-end. Time walk describes the effect that signals with different pulse height cross the threshold of the chip at different points in time and is defined as the time difference between the crossing point of a high signal with a steep rising edge and the crossing point of a signal that barely exceeds the threshold. As shown in figure 10.3, increasing the threshold will move the intersection point of the threshold and the rising edge to a later point in time. This results in a shorter time distance between the threshold crossing and the trigger, which is reflected in lower latency values.

In level sensitive mode, the distribution becomes wider than in edge sensitive mode. This is caused by the fact that the output of the front-end stays HIGH as long as the signal amplitude remains above the threshold. Therefore, the particle is detected in several clock cycles instead of only one. The distribution is still superimposed by the 25 ns uncertainty of the random



(a) (b)

Figure 10.11.: Latency scan of a Single MaPSA in edge (a) and level (b) sensitive mode. Due to the time walk of the MPA, increasing the threshold in edge sensitive mode causes the distribution to shift towards lower latency values. In level sensitive mode, increasing the threshold leads to narrower distributions, which are still wider than in edge sensitive mode. The offset at a threshold of 90 LSB is caused by random noise hits that are present for each latency and TDC values.

particle arrival. However, instead of shifting the latency, increasing the threshold predominantly results in a narrower distribution due to the shorter time period that the signal remains above the threshold. The fact that the distribution is much wider and stays more or less centered across various threshold values makes it much easier to find exactly one latency that fits almost all values during a threshold scan. For that reason, all measurements have been performed in level sensitive mode. Nevertheless, regular checks and fine-adjustments were carried out to ensure optimal operation of the chip throughout the entire data acquisition.

10.3.4. Measurement program

In total, four different unirradiated Single MaPSAs have been investigated for the sensor design study during the beam test at DESY. Each of them was equipped with a different kind of single PS-p: the Standard, the PCommon, the NoBias or the CPT sensor. The measurement program for each of the four assemblies included a bias scan in which the bias voltage of the sensor was increased from 10 V to 200 V and a threshold scan in which the threshold of the chip was gradually increased from 85 LSB to 250 LSB. In the end, measurements at different angles of incidence were conducted as well. However, if not stated otherwise, most data has been recorded at the nominal setting of a bias voltage of 200 V, a threshold of 110 LSB and perpendicular beam incidence ($\alpha = 0°$).

10.3.5. Data analysis

Unlike the MaPSA light test beam data, all data of the Single MaPSA beam test is processed by the EUTelescope framework. This includes data of the telescope, the timing reference and the MPA. The typical analysis chain of EUTelescope is shown in Figure 6.4 of Chapter 6. First, the raw data is converted into the LCIO file format. Then, clusters in every telescope plane as well as in the REF and the DUT are created. These local clusters are then transformed

into hits in the global frame of reference. These hits are used to iteratively align all planes of the telescope, the REF and the DUT, using the general broken lines (GBL) algorithm and the Millepede II software package. After all planes are aligned, the tracks are reconstructed and interpolated on the REF and the DUT plane. The local coordinates of these interpolated hits together with additional data, such as the cluster size, are stored in a common ROOT file, which is used as input for a standalone analysis software package written in C++. For the following analyses only tracks with a corresponding hit within one pixel cell on the reference plane (150 µm × 100 µm) are taken into account.

10.3.6. Residual distributions

One of the first quantities that is determined during the beam test analysis, is the intrinsic resolution of the DUT. Therefore, the residual distribution of the DUT hit positions and the impact point of the reconstructed tracks has to be determined. The standard deviation or root mean square (RMS) of this distribution is then defined as the measured resolution σ_{meas}, which is composed of the intrinsic resolution of the DUT σ_{DUT} and the pointing resolution of the telescope σ_{Tel}. Assuming that the intrinsic and telescope resolution are uncorrelated, σ_{DUT} is determined by

$$\sigma_{\text{DUT}} = \sqrt{\sigma_{\text{meas}}^2 - \sigma_{\text{Tel}}^2}. \tag{10.1}$$

However, with a distance of $\mathrm{d}z = 150\,\text{mm}$ between the telescope planes on each arm and a distance of about $\mathrm{d}z, \text{DUT} = 80\,\text{mm}$ between the last upstream plane and the DUT, the pointing resolution of the telescope is expected to be about 5 µm and thus much smaller then the measured resolution [Jan+16]. Therefore, the resolution of the DUT can be approximated to:

$$\sigma_{\text{DUT}} \approx \sigma_{\text{meas}}. \tag{10.2}$$

Both, the intrinsic as well as the telescope resolution are dominated by systematic uncertainties like the dependency on the residual cut, the correct estimation of the scattering material as well as the uncertainty of the particle energy. These uncertainties are hard to estimate and thus, only the RMS is shown in the following.

The residual distributions in x and y of a Single MaPSA, equipped with a Standard sensor, which is operated at the nominal settings, are shown in figure 10.12. The intrinsic resolutions of $\sigma_{\text{DUT,x}} = 28.9\,\mu\text{m}$ and $\sigma_{\text{DUT,y}} = 418.2\,\mu\text{m}$ are in good agreement with the expected binary resolution of the Single MaPSA,

$$\sigma_{\text{DUT},x} = \frac{100\,\mu\text{m}}{\sqrt{12}} = 28.9\,\mu\text{m} \tag{10.3}$$

$$\sigma_{\text{DUT},y} = \frac{1467\,\mu\text{m}}{\sqrt{12}} = 423.5\,\mu\text{m}. \tag{10.4}$$

Both distributions are composed of two contributions: residuals of single pixel hits and residuals of cluster hits. In case of single pixel hits, the expected hit position is always located in the center of the pixel. For the Single MaPSA, this leads to an x and y residual distribution that is shaped like a box with a width of 100 µm and 1467 µm, respectively. However, due to the limited resolution of the telescope and the increased charge sharing at the border of the pixel cell, the edges of the box are smeared, leading to the distributions shown in figure 10.12. While the limited telescope resolution yields a slightly larger standard deviation of the distribution, charge sharing and the resulting cluster hits can lead to an increased intrinsic resolution of the DUT, which can even be better the calculated binary resolution. The visible peak on top of

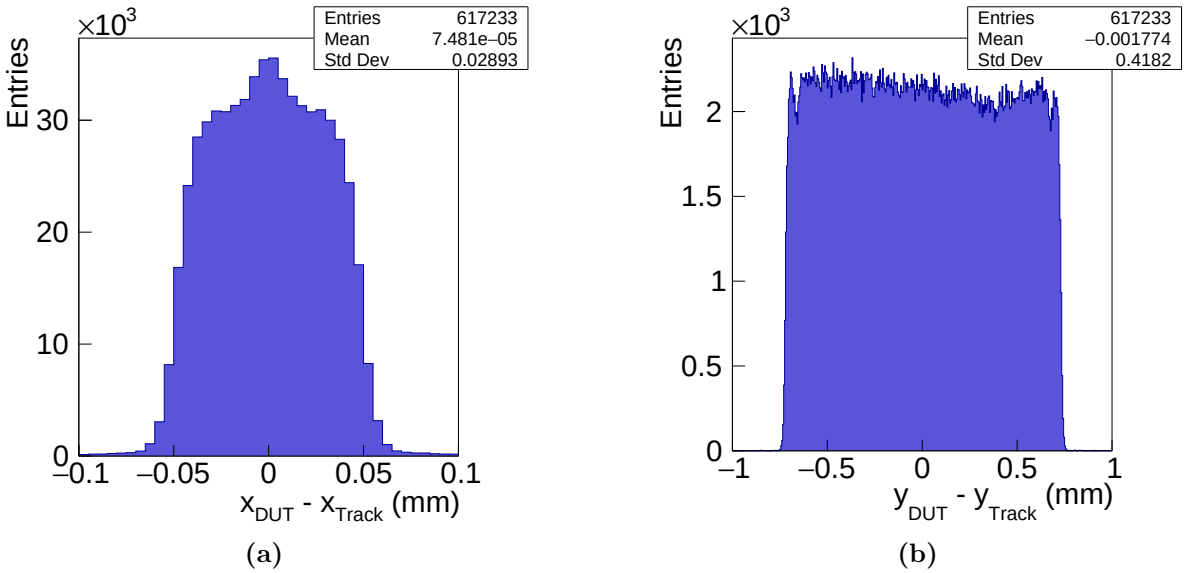


Figure 10.12.: Residuals of a Single MaPSA equipped with a Standard sensor. The distributions yield an x and y resolution of 28.9 µm (a) and 418.2 µm (b), respectively. Both values are in good agreement with the expected binary resolution of a Single MaPSA. The two noticeable dips in the residual distribution along the long side of the pixels (b) are caused by the inefficient punch-through structures of the Standard layout.

the indicated box at 0 mm in figure 10.12a is caused by some of these additional cluster hits between the pixels. However, only clusters that include an even number of activated pixels contribute to this beneficial part in the residual distribution. In this case, the hit position of the cluster is located exactly between two pixels, which leads to a residual that is half as wide as for single pixel hits or cluster hits with an odd number of activated pixels where the hit position is located in the center of a pixel. Fitting an error function in the form of

$$erf(u) = \frac{2}{\sqrt{\pi}} \int_0^u \exp^{-t^2} \mathrm{d}t \qquad \text{with:} \quad u = \frac{x}{\sqrt{2}\sigma} \tag{10.5}$$

to the edges of the distribution yields a standard deviation σ of about 7 µm, which is well in agreement with the expected telescope pointing resolution considering the additional uncertainties mentioned above.

The two noticeable dips in entries at the edges of the distribution in figure 10.12b are caused by the inefficient punch-through structures (PTS) on the Standard layout of the single PS-p sensor. These dips become even more vivid by looking at the combined x and y residual distribution, shown in figure 10.13.

This two-dimensional residual distribution reveals the superposition of all 100 µm × 1467 µm pixel cells that are covered by the telescope. Since the PTS is placed alternately at the top and bottom of the pixel cell, both are indicated as dots with fewer entries than the surrounding pixels.

The intrinsic resolutions of all four different PS-p sensor layouts is summarized in table 10.1. All residuals meet the expectations and only vary within 5 µm along the y axis. Therefore no preferred design choice can be made at this point.

The residuals are also used to verify data synchrony of each run during the analysis. Similar to the MaPSA light beam test, the residual distributions of 1000 events each are plotted against the event number, which is shown in figure 10.14. While in figure 10.14a no synchronization

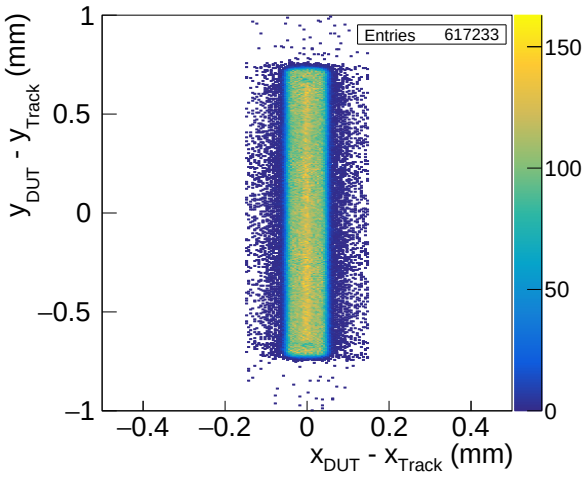
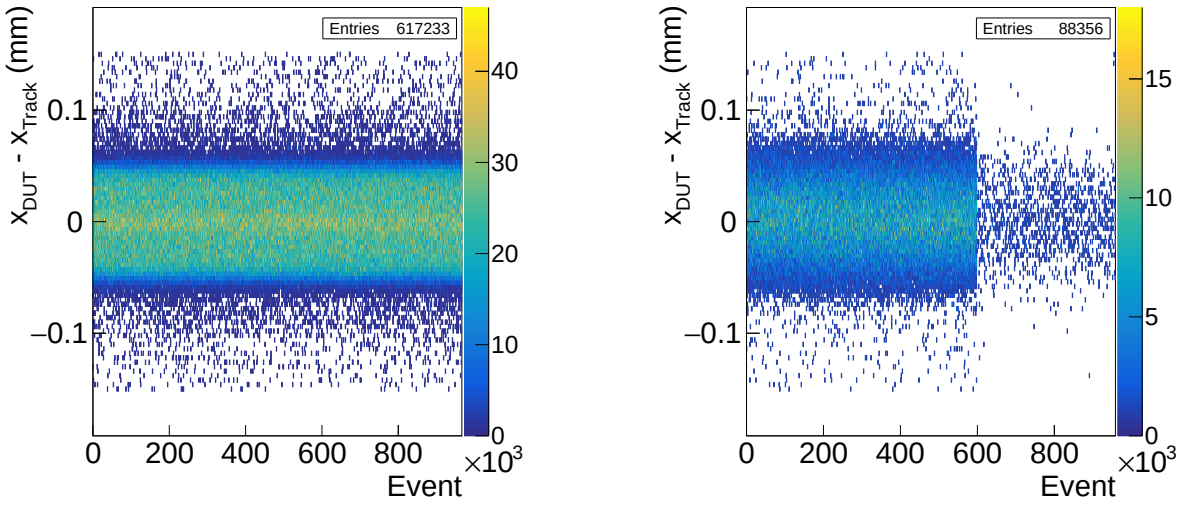


Figure 10.13.: Two-dimensional residual distribution of a Single MaPSA. Combining the x and y residual distribution reveals the superposition of all pixel cells of the Single MaPSA that are covered by the telescope. The alternating PTS are indicated as small dots with fewer entries at the top and bottom of the pixel cell.

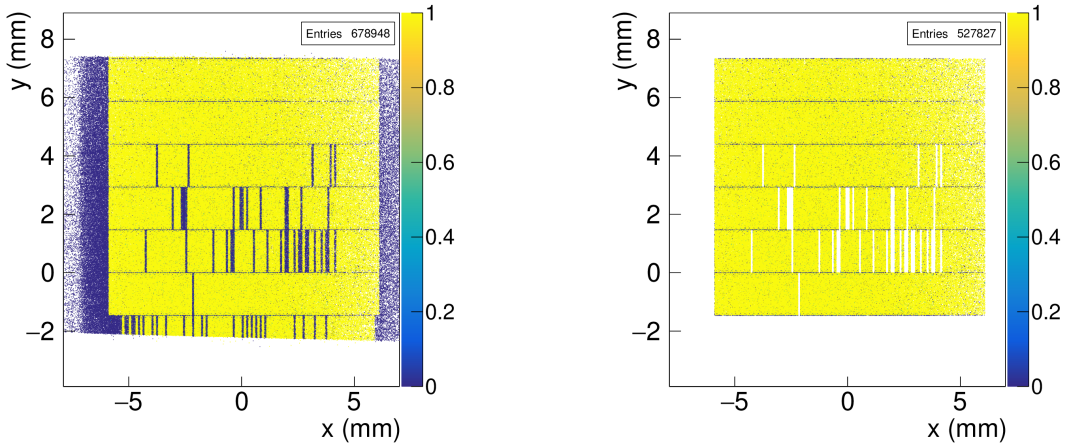
Table 10.1.: Intrinsic resolution of four different PS-p single sensor designs. All measurements were performed at perpendicular incidence, a bias voltage of 200 V and a threshold of 110 LSB.

	Standard	PCommon	NoBias	CPT
$\sigma_{\mathrm{DUT},x}$ [µm]	29.0	29.0	28.8	28.7
$\sigma_{\mathrm{DUT},y}$ [µm]	418.2	422.4	422.7	420.4



(a) **(b)**

Figure 10.14.: Residual in x over the event number. Figure (a) shows perfect synchronization without any irregularities throughout the entire run. In figure (b), the residual distribution changes immediately as soon as synchronization is lost after about 600 000 events.



(a) (b)

Figure 10.15.: Unmasked (a) and masked (b) efficiency map of a Single MaPSA at the CERN beam test. Many unbonded pixels and the passive area around the pixel matrix are responsible for a reduced global efficiency of the assembly. By properly masking these areas, the global efficiency is increased significantly.

loss can be observed during the entire run, the data streams in figure 10.14b only remain synchronous for about 600 000 events.

At this point, fewer tracks with a reference hit are found and the number of entries decreases significantly. These runs were usually repeated or simply divided into an in-sync and out-of-sync part if the synchronization loss was not detected during the data acquisition. Either way, only synchronous data was used for the analysis.

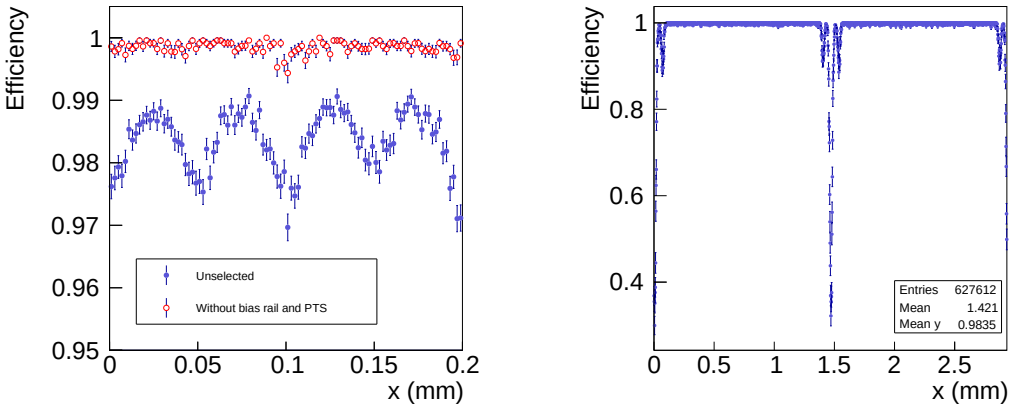
10.3.7. Efficiency Analysis

The efficiency analysis is performed similar to the MaPSA light test beam analysis. Tracks with a reference hit are interpolated onto the position of the DUT and compared with its hit data. If a hit is found in a user-defined proximity of 150 µm in x and 1500 µm in y of the interpolated hit, the interpolated hit position of the track is marked in a two dimensional histogram as efficient (1) and otherwise as inefficient (0). By normalizing each bin of the histogram to the number of entries, the position dependent efficiency is obtained.

Tracks that pass through known noisy and unbonded pixels have been excluded from the analysis in advance. Otherwise unbonded pixels would reduce the global efficiency, while noisy pixels, on the other hand, would artificially increase the global efficiency of the detector. Finally, tracks that do not hit the sensitive area of the Single MaPSA have been excluded as well. An exemplary result of a masked and unmasked efficiency map of one of the first assemblies, used at the CERN beam test, is shown in figure 10.15. By masking defective pixels and the area around the Single MaPSA, the global efficiency in that particular case was increased from 82.31 % to 96.76 %. All results that are presented in the following refer to the performance of properly masked assemblies.

10.3.8. In-pixel efficiency

Depending on the particle energy and the material in the beam, the resolution of the telescope can reach values of 5 µm and below [Jan+16]. This is good enough to resolve structures in and around the pixel cells. However, this is not simply done by looking at a single pixel cell of the



(a) **(b)**

Figure 10.16.: In-pixel efficiency in x (a) and y (b) of a 2x2 pixel matrix of the Standard sensor. Dips within the pixels are related to the punch-through structures in each pixel cell. The dip between the two pixels in x (blue solid markers) is caused by the particularly inefficient corner region between four adjoining pixel cells. By excluding the bias rail and PTS region (red hollow markers) an almost constant efficiency close to 100 % is achieved. The severe decrease in efficiency down to 30 % between the adjoining pixels in y direction is caused by the grounded aluminum bias rail on top of the silicon dioxide.

efficiency map shown in figure 10.15. Instead, the entire active area is subdivided into smaller 2x2 pixel matrices and superimposed to increase the number of entries in the histogram. The resulting efficiency distribution in x and y of such a 2x2 *modulo plot* of a Standard sensor with its individual PTS and an unshielded bias rail is shown in figure 10.16.

By looking at the in-pixel efficiency at varying x, a noticeable dip down to 97 % between the pixel cells is noticeable. The reason for this is the additional charge sharing between four adjoining pixel cells in the corner region below the bias rail. If the shared charge does not exceed at least one of the pixel thresholds, no hit is detected and the event is regarded as inefficient. This effect is more pronounced with thin sensors, in which generally less signal is generated than in thicker ones. The dips within the pixel cell at $x = 50\,\mu m and 150\,\mu m$ are caused by the PTS at the end of the pixels, which collect some of the generated charge and make the pixels less efficient at their position. By excluding the bias rail and PTS region an almost constant efficiency of almost 100 % is achieved. Thus, charge sharing between two pixels within one row does not have a great influence on the performance of the device. In y direction, the efficiency is constantly high along almost the entire pixel cell. Only at its both ends, two dips of the PTS are noticeable. Between the pixels and below the bias rail, however, a significant drop in efficiency down to 30 % is visible. This becomes even more evident by combining these two histograms into a two-dimensional efficiency map and zooming into the bias rail region, which is shown in figure 10.17.

The two bias dots in two of the pixels are clearly visible. While the efficiency between two pixels within the same row barely decreases at all, the area between the rows is clearly affected by a severe efficiency loss, caused by the bias rail. Especially the corner region between four adjacent pixel cells is affected by this problem, due to the additional charge sharing between the four pixels. This behavior of the Standard layout is expected and has already been observed during the beam test of the smaller PS-p light prototypes. This result is the starting point

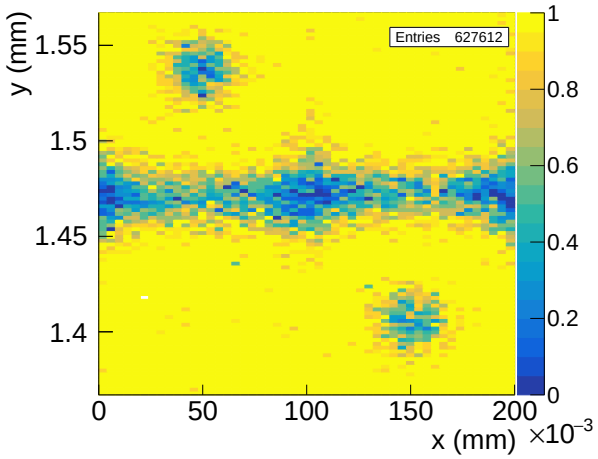


Figure 10.17.: Zoomed modulo efficiency map of a Single MaPSA equipped with a Standard sensor. The two bias dots of the PTS are clearly visible. The area between the two pixel rows is severely affected by the efficiency loss. Particularly low efficiencies are encountered in the corner between four pixel cells, which is most likely caused by the charge sharing effect.

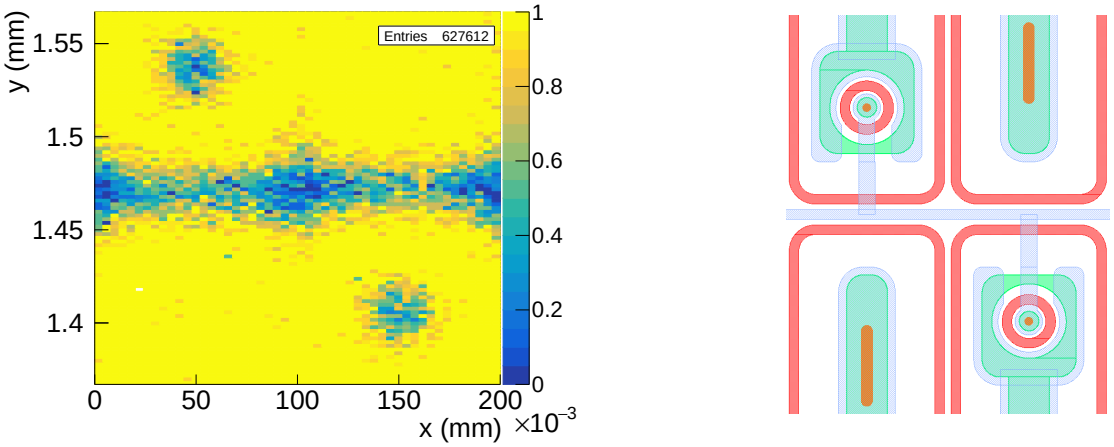
for the sensor design study to find an optimal design for the final PS-p, which reduces the inefficiency in the bias rail region.

10.3.9. Efficiency maps of different sensor layouts

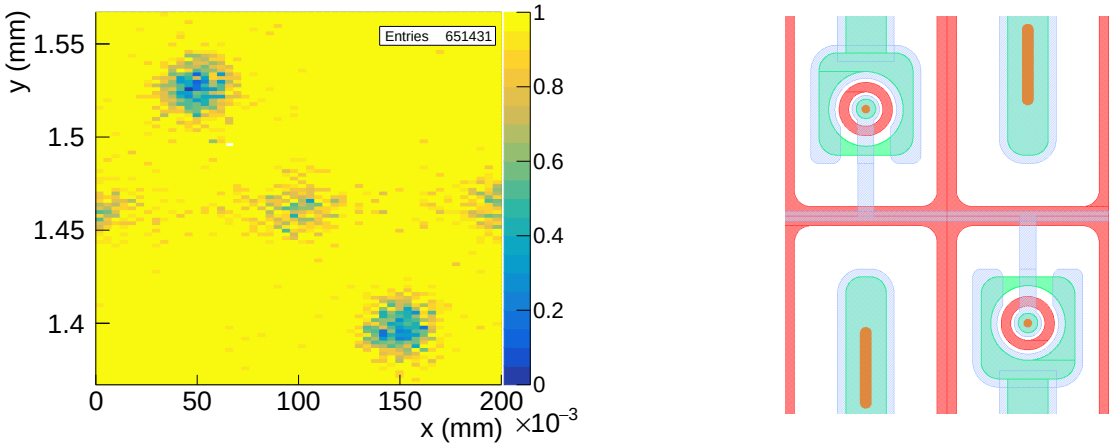
The design study includes four assemblies equipped with four different single PS-p sensor layouts (Standard, PCommon, NoBias and CPT) that have been investigated. These assemblies feature only few or no unconnected pixels compared to the first assembly used at the CERN beam test. All data has been processed by the same analysis chain and only the mask has been adapted to the respective assembly. The individual zoomed modulo efficiency maps of the four different sensor layouts together with their corresponding GDS layout are shown in figure 10.18 and 10.18.

Starting with the Standard layout, both PTS as well as the bias rail region are clearly visible and reduce the overall efficiency of the assembly. By looking at the PCommon layout, the inefficiencies of the PTS are still noticeable, but the bias rail region shows a significant increase in efficiency and only the corner region between four pixel cells shows a small efficiency loss. This is related to charge sharing between the four pixel cells. Nevertheless, the shielding effect of the bias rail by the common p-stop implant, which was predicted by the TCAD simulations in Chapter 7, is confirmed. By substituting the individual PTS, the pixel cells of the CPT layout are fully efficient and only the corner regions with and without a CPT show noticeable efficiency losses. The NoBias sensor with individual p-stop rings and without a bias grid as well as no PTS shows almost no inefficiency at all. Only the corner region is slightly affected by charge sharing but by no means as much as in the other designs. This could indicate that the common p-stop might have an influence on charge sharing in that particular region. Unfortunately, comparison measurements with the Standard layout and its individual p-stop rings are not possible due to the charge collecting bias rail. The quantitative difference in efficiency between these four designs is summarized in table 10.2.

In conclusion, the efficiency analysis of the four different PS-p layouts meets the expectations raised during the design phase of the PS-p prototype wafer. The Standard layout shows the



(a) Standard

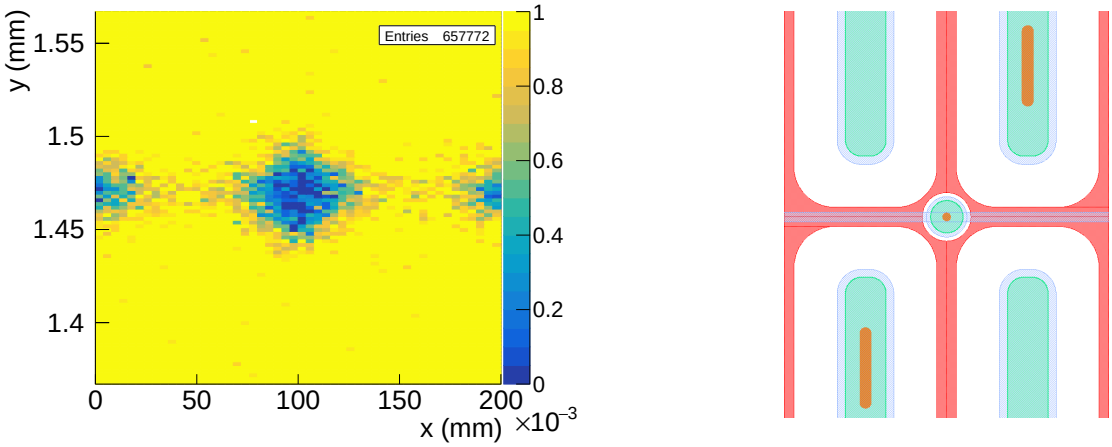


(b) PCommon

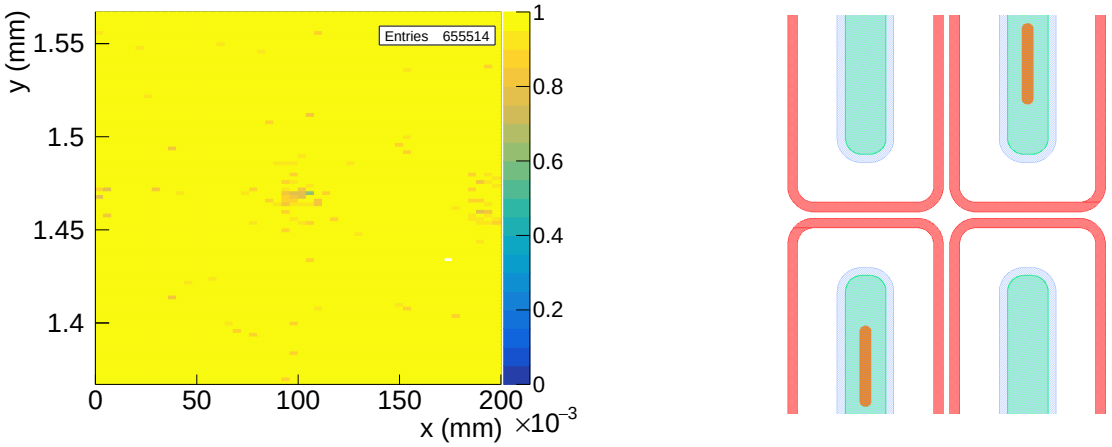
Figure 10.18.: Zoomed modulo efficiency maps of two Single MaPSAs equipped with a Standard or PCommon single PS-p sensor at a bias voltage of 200 V and a threshold of 110 LSB Shielding the bias rail (PCommon) increases the efficiency of the sensor significantly compared to the Standard layout.

Table 10.2.: Efficiency of four different PS-p single sensor designs. All measurements were performed at perpendicular incidence, a bias voltage of 200 V and a threshold of 110 LSB.

	Standard	PCommon	NoBias	CPT
Efficiency [%]	98.35	99.36	99.88	99.50



(c) CPT



(d) NoBias

Figure 10.18.: Zoomed modulo efficiency maps of two Single MaPSAs equipped with a NoBias or CPT single PS-p sensor at a bias voltage of 200 V and a threshold of 110 LSB. Substituting four PTS with one CPT or omitting the bias grid completely (NoBias) increases the efficiency of the sensor significantly compared to the Standard layout.

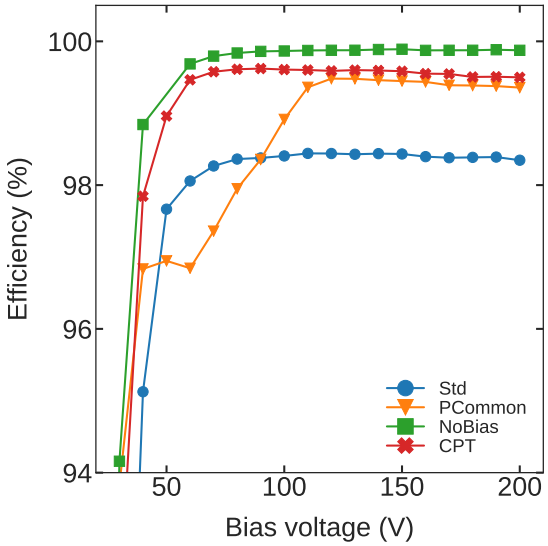


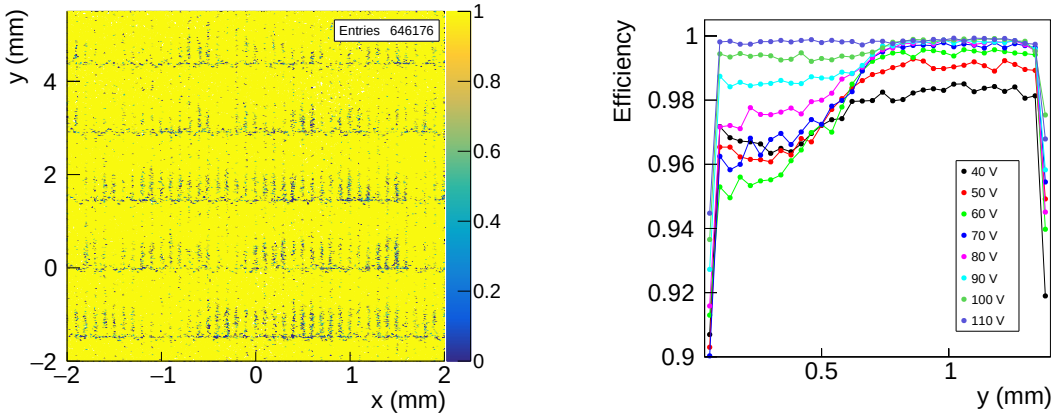
Figure 10.19.: Efficiency of four different PS-p single sensors at various bias voltages. All but the PCommon sensor show a very similar turn-on behavior and a minimum operation voltage around 70 V to 90 V. The PCommon sensor, however, shows an unexpected behavior between 50 V and 100 V.

lowest efficiency, which was expected from the results of the PS-p light beam test and the simulations. The bias rail as well as the individual punch-through structures lead to noticeable inefficiencies at perpendicular incidence. By shielding the aluminum bias rail with a common p-stop, the efficiency of the assembly could be increased by approximately 1 %. By substituting four individual PTS with a common punch-through in the CPT layout, the efficiency could be further increased, while keeping the sensor testable before assembly. Finally, by dropping the bias grid entirely in the NoBias approach, a maximum efficiency of 99.9 % can be achieved. This is the reference value for the maximum achievable efficiency of the PS-p, without changing the width to pitch ratio of the sensor.

10.3.10. Bias scan

In order to find the optimal operating point of the silicon sensor, a bias scan has to be performed for each assembly. At the beginning of the bias ramp, the efficiency of the sensor increases continuously until a point at which the efficiency starts to saturate. This point marks the minimum operating point at which the signal is significantly larger than the threshold of the chip. Since all designs are based on the same wafer material, the minimum operating point of all design variants is expected to be approximately the same. The result of the bias scans of all four designs is shown in 10.19.

As expected, almost all designs follow the same trend in efficiency. Only the PCommon sensor shows an unexpected behavior between 50 V and 100 V, where the efficiency stagnates for a short moment and only then continues to rise again with increasing bias voltage. By looking at the two dimensional efficiency map of the run at 50 V in figure 10.20a, inefficiencies around the lower halves of the pixel cells are noticeable. As the bias voltage increases, the efficiency in this part of the pixel cell first starts to decrease slightly, but then rises continuously and at 100 V equals the efficiency in the upper half of the cell (shown in figure 10.20b). Since every pixel cell is affected by this problem, impacts from the alternating PTS can be excluded at this



(a) (b)

Figure 10.20.: Efficiency of the PCommon sensor at bias voltages below 100 V. The efficiency map (a) reveals that all pixels show severe inefficiencies in the lower half of the pixel cell. By increasing the bias voltage (b), the efficiency first decreases before it fully recovers at a bias voltage of 110 V.

point. The only other difference of the lower and upper half of the otherwise symmetric pixel cell are the bump bond pads that are located only in the upper half of the pixel. However, this is true for all assemblies, independent of their bias rail design. Since only one PCommon sensor was available during the beam test, additional test beam measurements with new PCommon assemblies are required to determine whether the problem is related to this specific assembly or whether the problem is associated with the design of the PCommon sensor.

The minimum operating voltage of all the remaining sensors is located between 70 V and 90 V. This value equals approximately the full-depletion voltage of the sensor that has been determined during the C(V) measurements in laboratory. The nominal operation voltage of 200 V, which has been chosen for this beam test, lies well above the minimum operation voltage and thus, no inefficiency is expected due to under-depletion of the sensor.

10.3.11. Threshold scan

The final efficiency of the assembly does not only depend on the design and the thickness of the silicon sensor, but also on the threshold of the readout chip. A threshold that is too high means that some smaller signals get lost and the efficiency decreases. Too low thresholds, on the other hand, lead to noise hits that would distort the efficiency measurements as well as the track reconstruction later in the experiment. For that reason, a threshold scan is performed to determine the optimal operating point of the readout chip. Similar to the bias scan, increasing thresholds are set in the readout chip and the efficiency at each step is determined. The best threshold value is found at low thresholds close to the noise level, but still high enough to reduce noise hits to a minimum. The result of the threshold scans of all four assemblies is shown in figure 10.21.

At a threshold of around 80 LSB a significant fraction of noise hits is found in the data of the assembly, recognizable by the increased number of hits per event shown in figure 10.22. Even at a threshold of 100 LSB occasional noise hits could be observed in some of the assemblies. For that reason a common nominal threshold of 110 LSB has been chosen for the previous measurements. Again, since all four sensors are based on the same base material, the same amount of charge should be generated in their bulk. Hence a very similar behavior of their threshold scans is expected and observed. At the beginning of the scan, the efficiency stays

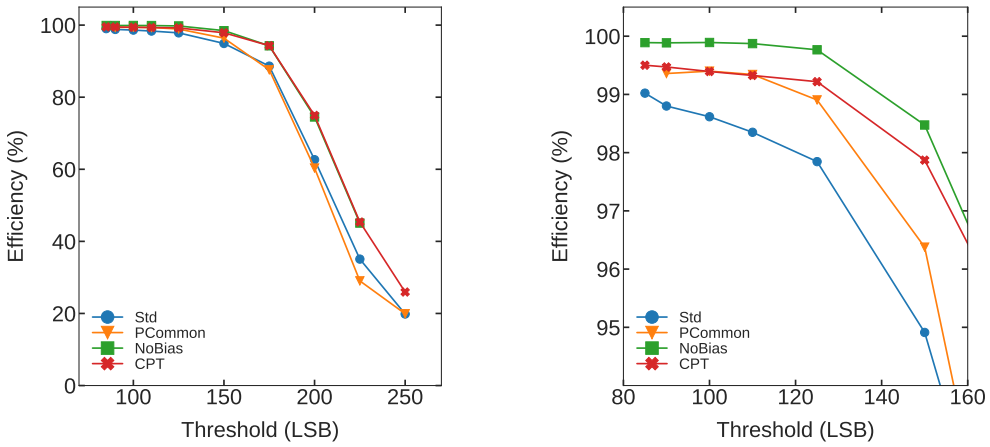


Figure 10.21.: Efficiency of four different PS-p single sensors at various thresholds. All four layouts follow the same course in the threshold scan (a). At low thresholds, efficiencies above 99 % can be achieved. With increasing threshold, the efficiency starts to drop to a minimum of about 20 % at a threshold of 250 LSB. By zooming into the region of low thresholds (b) differences in the various sensor designs become visible.

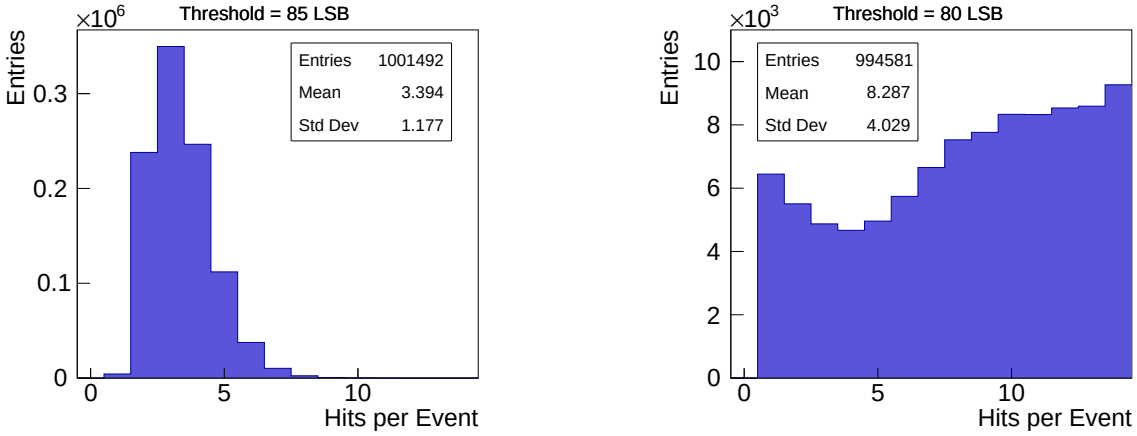


Figure 10.22.: Hit multiplicity per event for two different thresholds in a NoBias sensor. At a threshold of 85 LSB (a) an average hit multiplicity of 3.4 is found in the data. Lowering the threshold to 80 LSB introduces a lot of noise hits, which increases the hit multiplicity in the Single MaPSA assembly to 8.3.

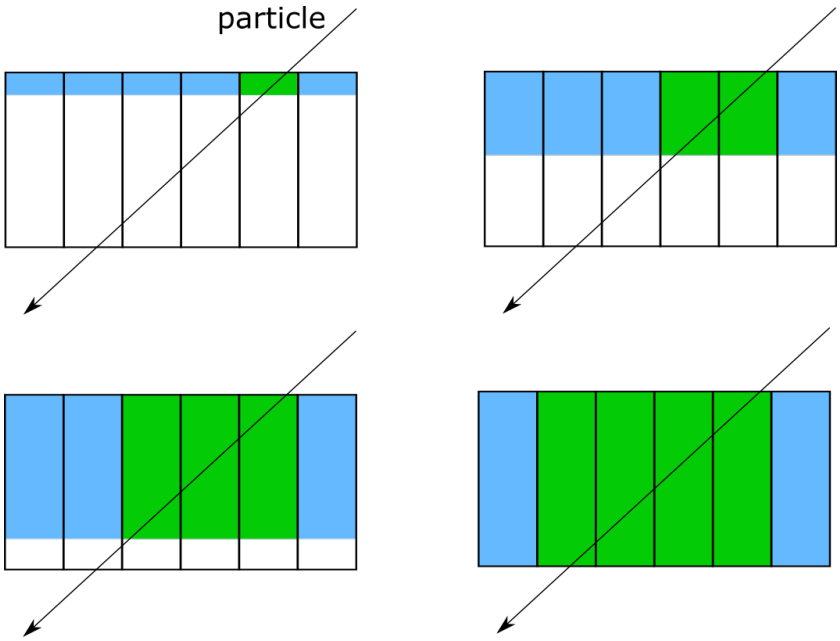


Figure 10.23.: Sketch of a cluster size measurement at high incidence angle. With increasing bias voltage, the sensitive space charge region (blue) grows further to the backside, causing more pixels to be activated (green) by particles with a high angle of incidence to the sensor.

more or less constant over a wide range of increasing thresholds. At a threshold of 150 LSB, the efficiency starts to drop and reaches its minimum of 20 % at a threshold of 250 LSB. A closer look into the range of 80 LSB to 150 LSB reveals that the maximum achievable efficiency is still dominated by the sensor layout. Unsurprisingly, the order in efficiency within the different layouts is still the same as for the bias scan. The threshold scan also reveals that all sensors except the NoBias sensor would benefit of even lower threshold values than the nominal one of 110 LSB. Especially the Standard layout could gain 0.5 % to 1 % in efficiency if the threshold would be set to 80 LSB. However, in order to still maintain a small safety margin to the noise level, the minimal possible threshold value should be set to at least 85 LSB or even 90 LSB.

10.3.12. Cluster size over bias voltage at a high incidence angle

The last measurement that was performed with one of the assemblies was dedicated to the additional step in the C(V) measurements that was observed during the laboratory measurements in Section 9.1.5. Up to now, every measurement that was performed indicates that the effect is most likely related to an immediate insulation of the guard and bias ring in the periphery. Nevertheless, in order to exclude any effects on the backside, a cluster size analysis at a high incidence angle of the particle at different bias voltages has been performed. The principle of this measurement is shown in 10.23.

When the incoming particle passes the sensor at a high angle of incidence, it creates clusters with a large number of activated pixels. The exact number, however, depends on the size of the space charge region (SCR). The bigger the SCR, the bigger the cluster size. Therefore performing a bias scan leads to a continuous increase in the cluster size until the bulk is fully depleted. The result of such a bias scan of one assembly at a particle incidence angle of 50° together with its C(V) characteristics is shown in Figure 10.24.

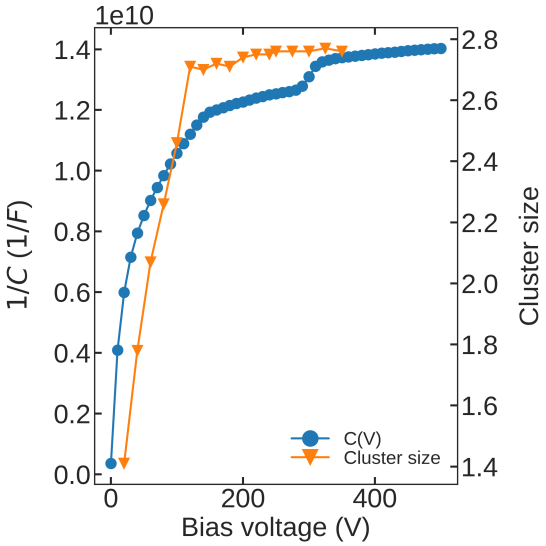


Figure 10.24.: Results of a cluster size measurement at an angle of incidence of 50°. At bias voltages below 200 V the course of the cluster size over the bias voltage roughly follows the course of the C(V) measurement in the laboratory. The saturation point at 130 V approximately matches the full-depletion voltage of 140 V. No additional step in the course of the cluster size could be observed.

The course of the cluster size over the bias voltage approximately resembles the course of the C(V) measurement in the laboratory. The cluster size starts to saturate at a bias voltage of 70 V, which is consistent with the full-depletion voltage that is determined by the bias scan of the beam test and the capacitance-voltage characteristics. However, no evidence of an increased cluster size at bias voltages around 300 V, where the step in the C(V) measurement was encountered, was observed. Thus, the assumption of an additional depletion of the backside can be further excluded at this point.

10.4. Beam test of irradiated assemblies

Up to now, only unirradiated sensors have been tested in the laboratory and in the test beam. These measurements were important to determine the quality of the material and to verify the initial design optimizations of the various single sensors. However, as soon as the detector will be operated in the CMS experiment, it will be exposed to radiation, which will affect the performance of the silicon sensor and the readout chip quite considerably. For this reason, eight additional assemblies have been built at KIT (two of each sensor variant), which have been irradiated with 23 MeV protons (hardness factor $\kappa = 2$) at the Zyklotron AG (ZAG) in Eggenstein-Leopoldshafen, Germany. Each design variant has been irradiated to fluences of $6 \times 10^{14}\,\mathrm{n_{eq}/cm^2}$ and $1 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$. The latter corresponds to the highest expected fluence in the PS region after 10 years of operation at the HL-LHC [CMS18]. The gap between the sensor and the readout chip on these assemblies has been filled with an EPO-TEK ® 301-2 underfill to avoid sparking between the high voltage on the sensor edge and the grounded readout chip at bias voltages above the expected breakdown voltage of 240 V (see Section 5.6.3). The functionality of the assemblies has been tested before and after irradiation before they have been shipped to DESY for a third beam test in August 2018.

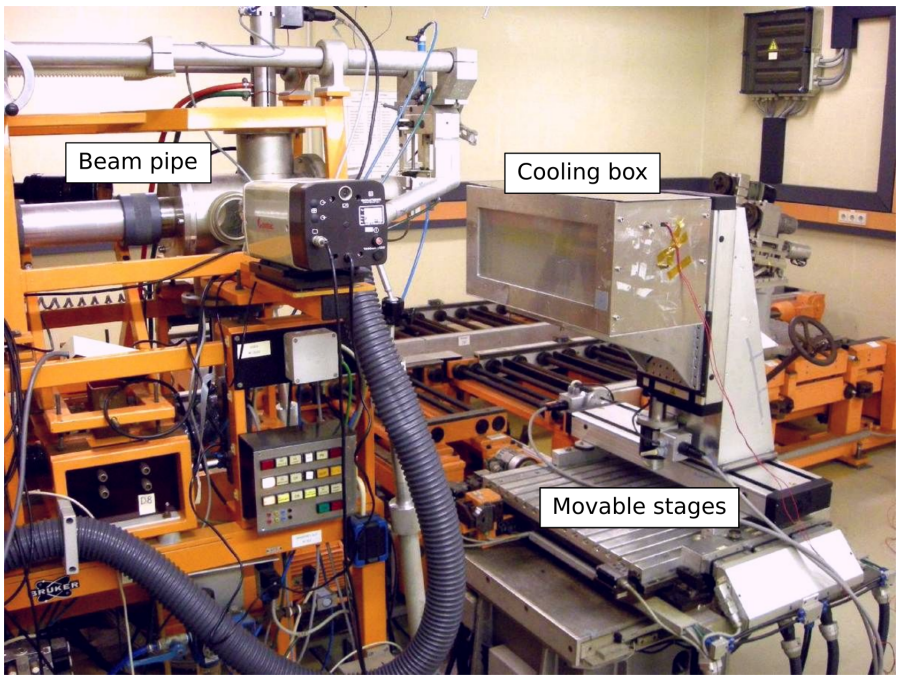


Figure 10.25.: The irradiation facility at the Zyklotron AG (ZAG) in Eggenstein-Leopoldshafen. The protons that come from the Kompaktzyklotron (KAZ) exit the beam pipe from the left. The samples are mounted on a frame that is placed inside the cooling box, which is flushed with dry air. The box is mounted on multiple stages to move the box inside the beam for a homogeneous irradiation of one or multiple samples [Ins19].

10.4.1. Karlsruher irradiation facility

As mentioned before, all assemblies have been irradiated at the Zyklotron AG in Eggenstein-Leopoldshafen, which operates several cyclotrons on the premises of KIT. The one used for silicon detector R&D is the Karlsruher Kompaktzyklotron (KAZ), which is capable of providing protons with a maximum energy of 40 MeV and a maximum current of 100 µA [ZAG19]. For the irradiation of silicon detectors, however, proton energies of 23 MeV at the sample and a maximum proton current of 2 µA are chosen. In order to irradiate the assemblies, they are mounted on an aluminum frame that is fixed in a box that is flushed with cold nitrogen gas. Since the proton beam only has a diameter of 4 mm to 8 mm, the whole box is placed on movable stages to steer and irradiate multiple assemblies homogeneously in the beam [Ins19]. The final setup of the irradiation facility at the ZAG is shown in figure 10.25.

10.4.2. The test beam setup

The test setup that is used for the irradiated assemblies is basically the same as before. The only difference is an additional cooling block below the carrier board of the Single MaPSA, which is connected to an ethanol chiller that cools the coolant down to −25 °C. Allen screws in the cover plate of the box that encloses the carrier board allow to apply pressure on the carrier board in order to press it against the cooling block and establish a proper cooling contact. This is necessary to reduce the leakage current of the irradiated sensors while operating them above their expected depletion voltage of 600 V or even 1 kV without driving them into thermal runaway. The surrounding box is flushed with dry air, keeping the dew point low and preventing condensation on the samples. Unfortunately though, changes in the setup due to the additional

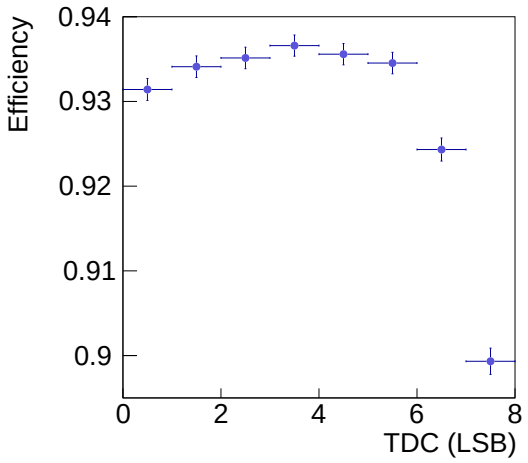


Figure 10.26.: Efficiency of an irradiated assembly at different TDC values in level sensitive mode. The efficiency varies strongly within a clock cycle due to the reduced signal height in irradiated sensors and the resulting shorter time period in which the signal stays above the threshold.

cooling block and the corresponding cooling pipes took up more space in the telescope frame, preventing the two telescope arms from being moved closer to the DUT. This worsened the telescope resolution and the pixel structures could no longer be resolved as well as before. By fitting an error function to the edges of one of the residual distributions a standard deviation of about 18 µm was determined. This means that the resolution is more than twice as bad as during the beam test of the unirradiated assemblies.

10.4.3. Measurements of irradiated Single MaPSAs

In total, seven out of eight assemblies have been tested at the second DESY beam test. One of the assemblies, equipped with a CPT sensor and irradiated to $6 \times 10^{14}\,\mathrm{n_{eq}/cm^2}$, could not be operated in the test beam since its sensor showed ohmic behavior and thus could not be biased properly. If not stated otherwise all assemblies have been operated at 600 V, which corresponds to the expected operation voltage of the silicon sensors in the Outer Tracker at the end of their lifetime. The nominal threshold has been set to a slightly lower threshold of 105 LSB compared to previous measurements. Again, only perpendicular incidence of the particles has been investigated. After calibrating the bias blocks and trimming the individual pixel cells, a latency scan is performed similar to the previous beam tests. However, while the plateau of the latency scan of the unirradiated assemblies was spread over multiple clock cycles in level sensitive mode, the plateau becomes quite narrow for irradiated assemblies. In fact, the efficiency already starts to decrease within one clock cycle. This is caused by the smaller signal that is generated in irradiated sensors, compared to the unirradiated one. As a consequence, the signal exceeds the threshold only for a very short period of time and does not remain above it for long. Figure 10.26 shows the resulting efficiency as a function of the particle arrival within the clock phase of an exemplary run with an irradiated Single MaPSA. The maximum is located within the clock cycle, which indicates that the correct latency is found. However, the efficiency decreases with increasing or decreasing TDC values. In the CMS Tracker, this effect is taken into account by adjusting the clock phase of each individual module depending on its distance to the interaction point. As a result, the clock is synchronized with the expected particle arrival of the collision products and only one or few TDC bins would be filled in this

kind of plot. Therefore, it is appropriate to only consider events with a TDC value that offers the highest efficiency in the analysis. However, since all other events would be discarded, only about 13 % of the recorded events would remain for the analysis. For that reason and due to the relatively slow decrease in efficiency, not only the maximum TDC but also its two neighboring bins are included in the final analysis (e.g. bins 3, 4 and 5 in figure 10.26). The final data is processed by the same analysis chain that was used for the unirradiated assemblies before. The reduced number of events, however, increases the statistical uncertainty of the measurement that is given as

$$\sigma_{\text{stat}} = \sqrt{p \cdot (100 - p) / N} \tag{10.6}$$

with the number of tracks N and the probability p to find a hit in close proximity on the DUT, which is best approximated by the average efficiency of the assembly [Mue18]. Although most of the statistical uncertainties are well below 0.1 % and are therefore normally not visible within the graphs, error bars have been added to the following results.

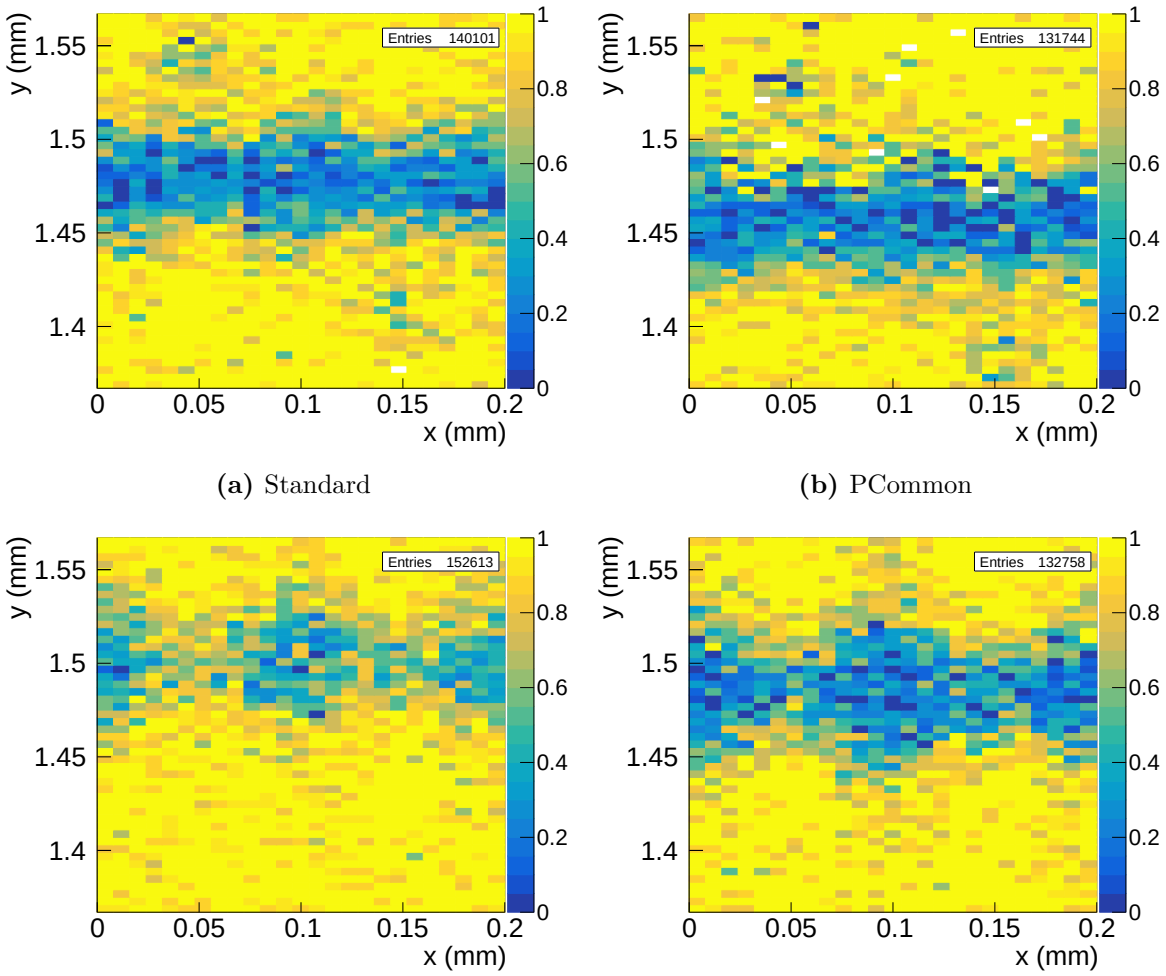
The asymmetric systematic uncertainty that is introduced by including more than the most efficient TDC bin in the efficiency analysis is hard to estimate due to the non-Gaussian distribution of the efficiency within the clock phase. By comparing the efficiency measurements that include three or only the maximum TDC bin, an average efficiency increase of 0.1 % can be achieved for all assemblies at reasonable thresholds and bias voltages at which the detector will be operated in the experiment.

10.4.4. Efficiency maps

The efficiency analysis is performed in the same way as the previous beam test analysis. Only tracks with a reference hit are taken into account and all unconnected and noisy pixels are masked in advance. The whole efficiency map has been reduced to a 2x2 pixel matrix and then superimposed to increase the number of entries in the modulo plot. The results of the four different assemblies that have been irradiated up to a fluence of $\Phi_{\text{eq}} = 10^{15}\,\text{n}_{\text{eq}}/\text{cm}^2$ are shown in figure 10.27.

Due to the reduced telescope resolution, the punch-through structures in the Standard and PCommon layout are only barely visible. A slight shift of about 20 µm along the long edge of the NoBias sensor is noticeable as well, but does not impact the global efficiency of the assembly. The first thing that is immediately noticeable is that the differences between the four irradiated assemblies are less pronounced compared to the unirradiated ones. Especially the inefficiencies in the bias rail region are visible in all four design variants. Only the NoBias sensor seems to be slightly more efficient in that particular part of the sensor than the others. The inefficiency between the pixel rows on all design variants is most likely dominated by charge sharing between the pixel cells and the reduced signal in the sensor after irradiation. As a consequence, the shielding of the bias rail becomes less important and the inefficiencies are mostly dominated by the charge sharing effect.

The global efficiency of the four unirradiated and the remaining seven irradiated assemblies for two different bias voltages are summarized in figure 10.28. Unirradiated assemblies are always operated at a bias voltage of 200 V. Irradiated sensors are operated at the target operating voltage of 600 V and the possible increased value of 800 V in the Outer Tracker [CMS18]. Plotting the efficiency over the fluence provides information on how the performance of the detector evolves over its runtime at the LHC. Regardless of the sensor variant, the efficiency drops by up to 4 % after irradiating the assembly to $\Phi_{\text{eq}} = 6 \times 10^{14}\,\text{n}_{\text{eq}}/\text{cm}^2$ and another 1 % after irradiating the assemblies further to $\Phi_{\text{eq}} = 10^{15}\,\text{n}_{\text{eq}}/\text{cm}^2$. Occasional pixel failures during multiple runs indicate that the Standard assembly which has been irradiated to $\Phi_{\text{eq}} = 6 \times 10^{14}\,\text{n}_{\text{eq}}/\text{cm}^2$ might have been equipped with a malfunctioning MPA, which could have impaired the results of that



(a) Standard **(b)** PCommon

(c) NoBias **(d)** CPT

Figure 10.27.: Zoomed modulo efficiency maps of four different assemblies that were irradiated to $\Phi_{eq} = 10^{15}\,n_{eq}/cm^2$. All assemblies show a severe efficiency loss in the bias rail region. Punch-through structures are only barely visible in the Standard (a) and PCommon (b) layout. The NoBias sensor still shows the highest overall efficiency, due to the missing bias grid (c). The CPT (d) sensor without individual PTS shows only a slightly better performance as the Standard or PCommon layout.

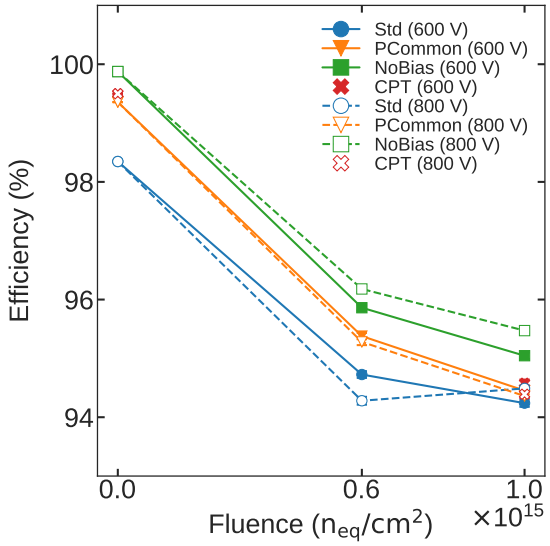


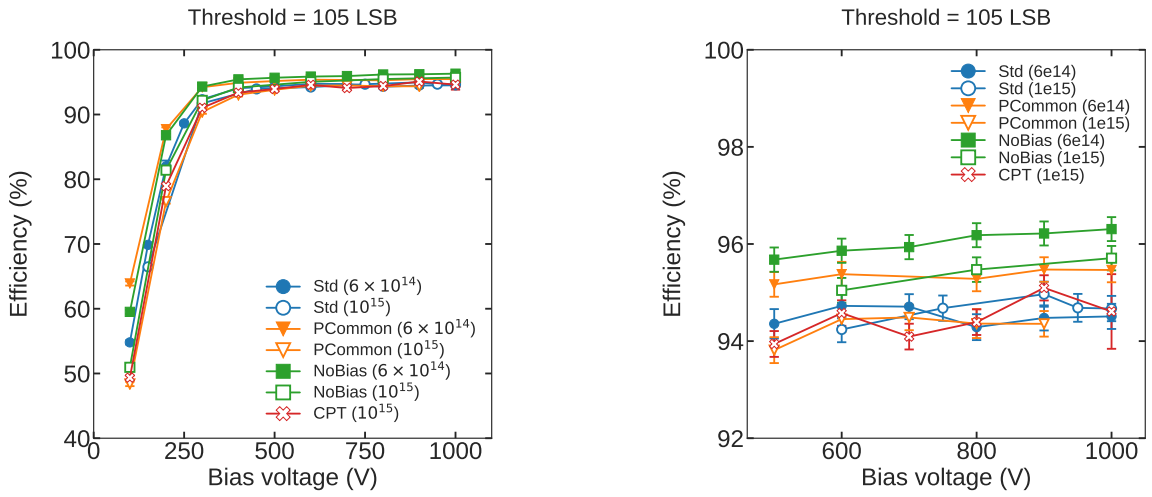
Figure 10.28.: Efficiency of all eleven assemblies for two different bias voltages. A nominal threshold of 110 LSB and 105 LSB has been chosen for non-irradiated and irradiated assemblies, respectively. The efficiency drops by up to 4 % after irradiating the assembly to $\Phi_{eq} = 6 \times 10^{14}\,n_{eq}/cm^2$. Irradiating the samples further to $\Phi_{eq} = 10^{15}\,n_{eq}/cm^2$, leads to another loss of 1 % in efficiency. The efficiency increases only slightly, if at all, when the bias voltage is raised from 600 V to 800 V (hollow markers)

particular assembly. Either way, increasing the bias voltage from 600 V to 800 V only results in a very small increase or even a reduction in efficiency of less than 1 % for most assemblies. This small effect might not be worth the additional drawbacks such as the increased power consumption of the detector and the risk of sparking between the sensor and the grounded readout chip. Careful consideration should therefore be given to whether it is worth operating the sensors at such high bias voltages.

10.4.5. Bias scans

Performing a bias scan of irradiated assemblies is probably even more important than for unirradiated ones. First and foremost the bias scan is used to find the optimal operation voltage of the sensor, and second, to estimate the gain in efficiency by increasing the bias voltage beyond the target operating voltage of 600 V in the Outer Tracker. While unirradiated sensors only gain little by over-depleting the sensor, irradiated sensors on the other hand might benefit quite a lot, as trapping of charge carriers becomes less probable, resulting in higher signals in the end. The results of all seven bias scans are summarized in figure 10.29. All seven sensors follow a similar course in the bias scan. This is mainly due to the identical base material, and therefore the same number of charge carriers that are generated in their bulk. After a steep increase up to bias voltages of 300 V to 500 V the efficiency starts to saturate and only increases slowly from then on. This means that increasing the bias voltage at this point will only lead to a slight increase in efficiency. However, this also comes with the drawback of a higher power consumption as mentioned before.

By looking more closely in the region 500 V to 1000 V, differences in the various sensor variants and the fluences become visible. Ignoring the badly performing assembly with a



(a) **(b)**

Figure 10.29.: Efficiency of seven irradiated assemblies at various bias voltages and a nominal threshold of 105 LSB. The fluence of each assembly is mentioned in parentheses and given in units of n_{eq}/cm^2. The course of all seven bias scans is quite similar (a) due to the fact that all sensors are based on the same base material. Full-depletion of all sensors is reached around 300 V to 500 V bias voltage. The NoBias sensor is the only sensor variant that clearly shows better performance than the others (b). At fluences of $\Phi_{eq} = 1 \times 10^{15}\,n_{eq}/cm^2$, the differences between the other three designs become marginal.

Standard sensor that was irradiated to $\Phi_{eq} = 6 \times 10^{14}\,n_{eq}/cm^2$, higher fluences always lead to lower efficiencies, which has already been shown in figure 10.28. Although the order in efficiency of the different sensor variants is quite obvious for certain bias voltages, no general rule can be found for the entire bias scan. Nevertheless, the following trend can be identified: first, the most efficient assembly is always equipped with a NoBias sensor. This was already seen on unirradiated assemblies and is related to the non-existing bias grid. Second, after a fluence of $\Phi_{eq} = 6 \times 10^{14}\,n_{eq}/cm^2$ the PCommon layout shows efficiencies that are still about 1 % higher than for the Standard layout. And finally, after irradiating the assemblies to $\Phi_{eq} = 1 \times 10^{15}\,n_{eq}/cm^2$, the differences between the Standard, the PCommon and the CPT layout become quite marginal and only the NoBias sensor still stands out significantly.

10.4.6. Threshold scans

The final measurement is the threshold scan of the irradiated assemblies that is used to verify the operating point of the readout chip. The results of all threshold scans at bias voltages of 200 V for unirradiated and 600 V for irradiated assemblies, are shown in figure 10.30.

The pedestals of all assemblies have been trimmed to a threshold of 77 LSB. First noise hits start to occur at a threshold of about 80 LSB. In contrast to the unirradiated assemblies, no constant plateau at thresholds between 85 LSB and 150 LSB is forming for neither of the irradiated assemblies. Instead, the efficiency starts to drop almost immediately as the threshold value exceeds the reduced signal of irradiated sensors quite early during the threshold scan. The fact that the signal in the sensor decreases with increasing fluence is also the reason why the assemblies that have been irradiated to $\Phi_{eq} = 6 \times 10^{14}\,n_{eq}/cm^2$ show slightly higher efficiencies than the assemblies that have been irradiated to $\Phi_{eq} = 10^{15}\,n_{eq}/cm^2$. Similar to

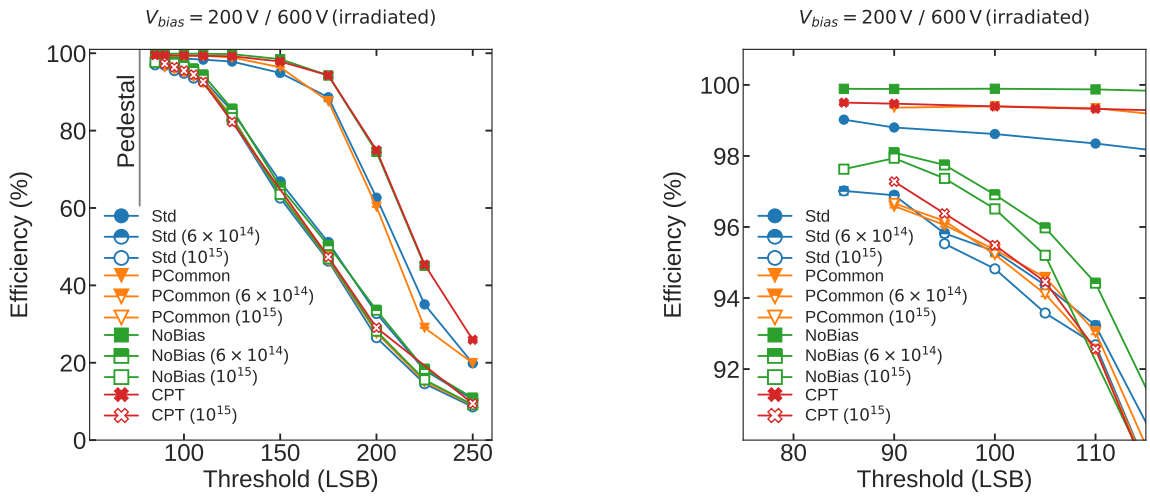


Figure 10.30.: Efficiency of all eleven tested assemblies at various thresholds. The fluence of the irradiated assemblies is mentioned in parentheses and given in units of n_{eq}/cm^2. None of the irradiated assemblies shows a plateau at thresholds close to the pedestal. The efficiency starts to drop almost immediately and reaches its minimum of about 10 % at a threshold of 250 LSB (a). By zooming into the region of low thresholds (b) differences in the various designs become visible. The order in efficiency of the four sensors variants stays roughly the same before and after irradiation. By decreasing the threshold from the nominal setting of 105 LSB down to 90 LSB an increase of up to 2 % in efficiency can be expected.

the order in efficiency during the bias scan, only assemblies equipped with a NoBias sensor show significantly higher efficiencies. Between the others only small differences are noticeable.

However, the most important result of the threshold scan is the fact that the nominal threshold of 105 LSB that was chosen as nominal value for the bias scan was probably slightly too high. Lowering the threshold to 90 LSB would have lead to efficiencies of 96.5 % in case of the PCommon sensor and even more than 98 % for the assembly equipped with a NoBias sensor. This would correspond to an increase of about 2 % for all irradiated assemblies. However, lowering the threshold below 90 LSB is not recommended, as most of the assemblies that were tested during this beam test had to deal with a lot of noise hits at a threshold of 80 LSB.

10.5. Conclusion of the test beam measurements

In this chapter the results of three beam tests of unirradiated and irradiated Single MaPSAs, equipped with various sensor variants have been presented. The first beam test at CERN was conducted in close cooperation with the chip and firmware developers and was the first time a full-size MPA was operated in a test beam environment. All the experience gathered during this beam test has been used to conduct additional test beam measurements for the sensor design study. The results of the subsequent beam test of four different unirradiated assemblies at DESY confirmed the expectations raised by the simulations and the beam test results of the MaPSA light. The assembly which is equipped with a Standard sensor reaches an efficiency of about 98.4 % and shows the expected inefficiencies of the punch-through structures and the bias rail. Forming a common p-stop below the bias rail does effectively shield the rail, leading to a slight increase of the total efficiency of about 1 % at perpendicular incidence of the particle. Substituting four individual PTS with one CPT results in fully efficient pixel cells. Only the corner region of four adjoining pixels still suffers from the charge sharing effect below the aluminum rail and the common p-stop. The NoBias sensor without any bias grid shows the highest efficiency of almost 99.9 %.

The third beam test of irradiated assemblies revealed that the beneficial effect of the common p-stop below the bias rail vanishes after irradiation, since the inefficiency in the region between the pixel rows is most likely dominated by charge sharing of the signal in irradiated sensors, which is already lower than in unirradiated ones. For that reason, differences in the design variants become more and more marginal with increasing fluence. Only assemblies that are equipped with a NoBias sensor still show slightly better results as their counterparts. The latest beam test also revealed that a chip threshold of 105 LSB is most likely too high for irradiated assemblies, as the efficiency for all assemblies increases by up to 2 % if the threshold is set to 90 LSB. Decreasing the threshold even further would result in even higher efficiencies but would also lead to additional noise hits that could impair the performance of the device. To estimate the electron equivalent of these thresholds, a test pulse calibration with one of the assemblies has been conducted after the beam test. Therefore, several threshold scans with increasing test pulse amplitudes and a small subset of pixels have been performed. By plotting the midpoints of the resulting S-curves, over the injected signal, the conversion factor between electrons and LSB is determined. The linear response behavior of 118 pixels on one of the assemblies is shown in figure 10.31. With an average slope of $(107 \pm 2)\,e^-/\text{LSB}$ and the trim target of 77 LSB, a threshold of 105 LSB corresponds to about 3000 electrons, which is approximately three times the value that is targeted during operation [CMS18]. Thus, a more realistic threshold value of about 90 LSB should be chosen as nominal value for future bias scans.

The highest efficiency of 98 % is only achieved by the most efficient NoBias assembly and not by any of the others. This means that modules whose sensors are positioned more or

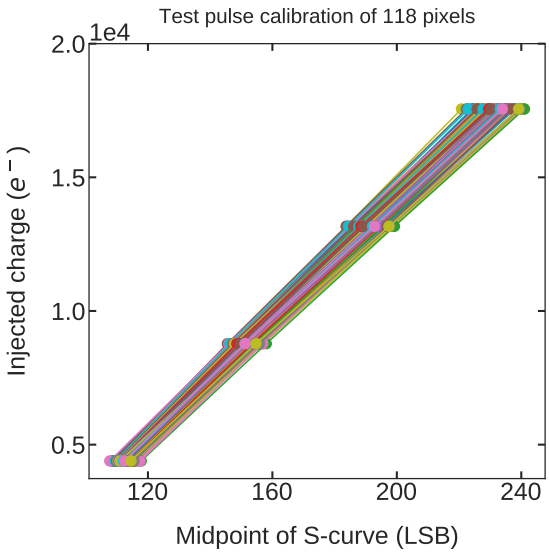
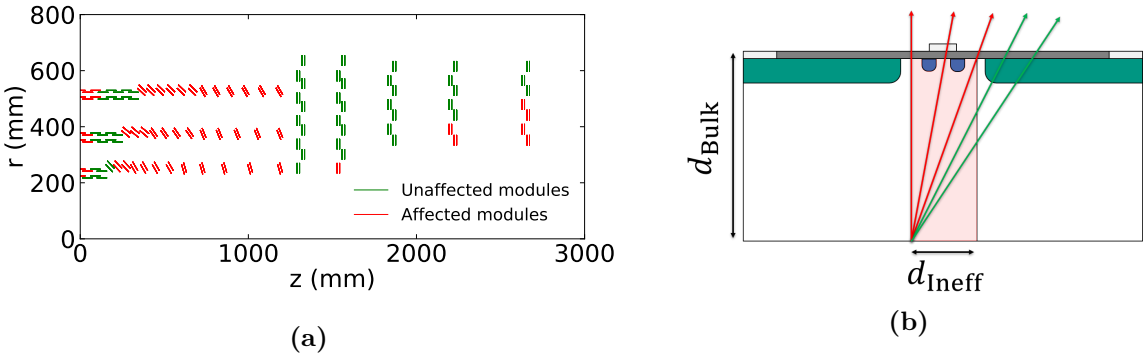


Figure 10.31.: Test pulse calibration of 118 pixels on one exemplary assembly. All pixels show a linear response behavior. The average slope of all 118 pixels is $(107 \pm 2)\,\mathrm{e^-}/\mathrm{LSB}$.

less perpendicular to the interaction point will suffer from efficiency losses in the future CMS Outer Tracker. However, as the incidence angle of the particles gets shallower, more charge is generated in the sensor, which increases the efficiency in the bias rail region and the PTS significantly. For that reason, additional measurements with rotated assemblies have to be performed to simulate different positions of the PS module along the beam pipe in the Outer Tracker. Nevertheless, it is still possible to roughly estimate how many modules will be affected by inefficiencies of the bias rail. Assuming that half the distance between two adjoining pixel implants below the bias rail is inefficient ($d_{\mathrm{Ineff}} = 37.5\,\mu\mathrm{m}$) and that the collision products follow a straight line in the rz-plane of the Tracker, a module is defined as "affected" if a particle can pass the sensor within the inefficient area, illustrated as red arrows in figure 10.32b. If the incidence angle is higher than the diagonal passage through the inefficient area, at least one of two pixels will register a hit (green arrow) and the module is defined as unaffected. Taking all module positions and tilt angles into account, about 46 % of the 5616 PS modules in the Outer Tracker are affected by a loss in efficiency. A quarter section of the CMS Tracker with all affected (red) and unaffected (green) modules is shown in figure 10.32a. The fact that almost half of the PS modules could be affected by the inefficiencies below bias rail, underlines the need for additional efficiency measurements of rotated assemblies even more.

Concluding the efficiency analysis, the Standard layout of the full-size PS-p still remains the least efficient, but also one of the most robust design choice that was implemented on the PS-p wafer. The PCommon variant convinces by a slightly better performance due to the shielding effect of the bias rail, which is noticeable up to a fluence of $\Phi_{\mathrm{eq}} = 6 \times 10^{14}\,\mathrm{n_{eq}/cm^2}$ or about $1800\,\mathrm{fb}^{-1}$ of recorded data at the HL-LHC. comes with a more drastic design change compared to the PCommon layout and is therefore less likely to be implemented on the final sensor. The NoBias sensor seems to be the best performing design that would increase the efficiency of the detector by up to 2 % compared to the Standard layout. However, due to the lack of a bias grid, the NoBias sensor comes with the drawback that it cannot be tested before assembling it with its readout chip. For these reasons, the PCommon sensor remains the preferred design choice as it offers a slight increase in efficiency over the Standard layout by simply creating a



(a) (b)

Figure 10.32.: PS modules in one quarter of the CMS Tracker that are affected (a, red) or unaffected (a, green) by an efficiency loss below the bias rail. A module is defined as affected, if a particle can pass the sensor solely within the inefficient area (b, red arrows) below the bias rail. If the particles always pass the efficient area of the sensor, the module is regarded as unaffected (b, green arrow). About 46 % of the PS modules are affected by an efficiency loss.

common p-stop out of the individual p-stop rings of the pixel cells. However, the unexpected behavior of the unirradiated PCommon assembly during the bias scan still raises cause for concern and should be checked with a second assembly in an upcoming beam test.

Part IV.

Summary and Outlook

11
Summary and Outlook

In the course of upgrading the LHC to the High Luminosity LHC (HL-LHC), the entire CMS Tracker will be replaced by a new detector to cope with the increased number of particle tracks in the detector volume caused by the higher luminosity of the collider. For that reason, new detector modules with radiation hard silicon sensors have to be developed that are able to withstand the increased particle fluence. Furthermore, since current triggering criteria of the L1-trigger will become inefficient with the increased number of highly energetic particles in the detector volume, it is also necessary to include track information of the Outer Tracker into the Level-1 (L1) trigger system of CMS. However, in order to limit the data that has to be sent to the trigger system at the brunch-crossing frequency of the accelerator, only a small fraction of hits in the modules have to be selected and prepared for the readout. To achieve this, all modules of the future Outer Tracker will be equipped with two closely spaced silicon sensors, which enables the possibility to discriminate charged particles with low and high transverse momentum. Only the latter are used for a fast online track reconstruction, which serves as input for the L1 trigger decision. While the outer part of the Outer Tracker will consist of 2S modules, which are equipped with two strip sensors, the inner part, closer to the pixelated vertex detector, will be composed of PS modules, which comprise a strip and a macro-pixel sensor instead of the second strip sensor, to deal with the higher track density closer to the interaction point and to provide additional z information to the tracking algorithms.

This work is dedicated to the pixelated sensor for the PS modules and the development of the first full-size macro-pixel prototype: the PS-p. This includes the entire development process from the smaller PS-p light prototype with 48×6 pixels, up to the full-size PS-p prototype, including the full 944×16 pixel matrix, which covers an active area of approximately $96\,\text{mm} \times 47\,\text{mm}$. This thesis is split into two parts. While the first part is dedicated to the PS-p light prototype and the introduction of the tools and the measurement methods applied in both parts of this thesis, the second one is devoted to the design and characterization of its full-size successor and some additional prototypes.

For the electrical characterization of the PS-p light, several laboratory measurements, such as I(V) and C(V) as well as multiple inter-pixel measurements have been conducted and revealed good results, which meet the requirements for their use in the future Outer Tracker of CMS. Some of these sensors have been assembled with prototypes of the future readout chip for the PS-p and have been tested in an electron beam at the DESY test beam facility. This study revealed that particles which pass the center of the pixel can be detected with almost 100 % efficiency, whereas particles that hit the sensor between two pixel rows close to the bias rail structure mostly pass the assembly undetected.

In order to understand the mechanism behind these areas with reduced detection efficiency and to further improve the existing design, detailed TCAD simulations have been conducted. Three different bias rail approaches and several p-stop distances have been investigated to find the optimal combination for an optimized PS-p. To determine the breakdown behavior and the performance of the sensors, the simulations include studies on the maximum electric field in the silicon bulk as well as a time resolved simulation of the charge collection process after a particle hit. The latter is used to determine the charge collection efficiency of the various

devices as a function of the particle hit position. The results of these simulations revealed that a common p-stop configuration below the aluminum bias rail promises higher efficiencies in this particular region while simultaneously reducing the maximum electric field in the bulk compared to the Standard layout with an atoll-shaped p-stop structure.

Based on the experience with the PS-p light and the outcome of the simulation study, the first full-size PS-p prototype wafer has been designed. While the layout of the pixel matrix for the full-size sensor has remained almost unchanged compared to the PS-p light, several smaller single sensors with different bias grid configurations have been implemented to experimentally confirm the simulation results. These single sensors are designed such that all their pixel cells can be connected with only one readout chip, instead 16 like the full-size PS-p. Besides the Standard layout three additional design variants have been implemented on the eight available single sensors on the wafer. The PCommon layout, which corresponds to the optimized design that was extracted from the simulations, a common punch-through (CPT) design in which four individual punch-through structures (PTS) have been substituted by a single CPT structure between four pixel cells and a NoBias variant, which does not include any biasing scheme at all. The latter approach reduces the inefficiencies in the pixel matrix to a minimum, but also has the disadvantage that the sensor cannot be tested until it has been assembled with a readout chip. The prototypes are based on 200 µm thinned silicon wafers which have been processed by Hamamatsu Photonics K.K.

A basic characterization of the full-size and the single sensors was performed on one of the custom-made probe stations at KIT. The initial I(V) and C(V) characteristics of almost all sensors show the expected results and meet the requirements set by the Outer Tracker sensor community. Only the CPT sensor shows an early breakdown, which has already been observed by Hamamatsu. A significant and unexpected drop in capacitance at voltages around 300 V during the C(V) measurement was traced back to an insufficient isolation of the bias and the guard ring at low bias voltages. Fortunately, this effect does not affect the performance of the device and could most likely be eliminated by adding an additional p-stop ring between the bias and the guard ring. However, strong evidence has been found that the 200 µm thick material is susceptible to scratches on their backside that already occur after the first measurements on the probe station despite handling the sensor with utmost care. These sensors start to breakdown once the sensor reaches its full-depletion and thus when the space charge area reaches the backside of the sensor. Additional measurements with a protected sensor backside as well as some diodes whose backside have been intentionally scratched confirm this hypothesis. While no early breakdown has been observed on sensors with a protected backside, diodes of two different prototype wafers of the same base material almost immediately break down as soon as the first scratches are introduced to their backside. Finally, an unexpected humidity dependence of the I(V) and breakdown characteristics was observed. By examining one of the single sensors with an infrared camera and operating it above its breakdown voltage, multiple spots with high current density along the guard and bias ring as well as at some PTS have been observed. These spots, however, vanish with decreasing humidity and thus mark areas that are affected by the ambient humidity. Since the tracking volume will be flushed with dry nitrogen during operation [CMS18], this effect should be negligible in the final detector. Nevertheless, especially the increased current density at the PTS at an ambient humidity of 34 % give cause for concern and should be kept in mind during the qualification process of future PS-p prototypes.

Most of the tested single sensors have been subsequently equipped with one of the first MPA prototypes, using the gold-stud bump bonding technique at KIT. These Single MaPSAs are used to determine the efficiency of the individual sensor variants at perpendicular incidence of particles. A total of eleven assemblies, both unirradiated and irradiated, have been investigated at several beam tests at CERN and DESY. The results obtained with these unirradiated

assemblies confirm the expectations from the simulation and the previous beam test of the MaPSA light. The efficiency analysis of the PCommon layout, for example, shows that the predicted shielding effect of the bias rail works and that the efficiency can be increased by 1 % to 2 % compared to the assembly that is equipped with a Standard sensor at perpendicular incidence of the particles. By choosing one of the other two designs, the efficiency of the assembly can be increased even further and can reach 99.9 % in case of the NoBias variant. The results of a second beam test at DESY with a set of irradiated assemblies revealed that the benefits of the individual designs become marginal at the maximum expected fluence of $\Phi_{\mathrm{eq}} = 10^{15}\,\mathrm{n_{eq}/cm^2}$ after 10 years of operation in the PS region at the HL-LHC. Only the NoBias sensor still stands out and reaches an efficiency that is approximately 1 % to 2 % higher than for the Standard sensor. Increasing the bias voltage from the target operation voltage of 600 V up to 800 V also has only a minor effect and can increase the efficiency of all assemblies by less than 1 %, but comes with a penalty in leakage current and is not recommended for operation. Instead, the threshold scan revealed that it is more important to choose a low but reasonable threshold value in the chip. A threshold of 105 least significant bits (LSB), which was chosen as nominal value for the bias scan at the beam test, already reduces the efficiency of all assemblies by up to 2 % compared to a threshold of 90 LSB. This value was chosen to keep the measurements of the unirradiated and the irradiated assemblies comparable. In order to further increase the efficiency of irradiated assemblies, lowering the threshold below 90 LSB and simultaneously masking the first pixels that start to introduce noise into the data set should be considered as a valid option for the next test beam measurements. Nevertheless, all design variants are still able to surpass the current Standard layout in terms of their efficiency at perpendicular incidence. A rough geometric estimate of the Outer Tracker revealed that nearly 50 % of the PS modules in the Outer Tracker are hit at a critical angle at which the particles solely pass the bias rail region and thus may benefit from one of the improved designs. Otherwise, up to 4 % of the particles could pass the irradiated sensor undetected, which would lead to a lack of hits for the p_T discrimination and could ultimately impair the track reconstruction of the entire CMS experiment. In the end, the PCommon layout prevailed as the preferred design choice, as it can be tested without a readout chip and only requires small design changes compared to the Standard layout.

Since the second batch of PS-p wafers is expected to arrive soon, new sensor studies are already in preparation. This batch will include 20 additional wafers that are based on the well-known 320 µm thick material, which has been used in many of the previous studies in the CMS community. Sensors that have been processed on this material in the past neither showed problems with the backside nor a strong humidity dependence that was observed on the 200 µm thick material. The upcoming sensor study will again consist of a full characterization of the full-size and the single sensors in the laboratory as well as another beam test at DESY to determine the efficiency of the assemblies with the new sensor material. Again, several sensor layouts will be investigated to confirm the results of the previous measurements and to examine how the sensor thickness affects the performance of the various devices. Especially during the threshold scan a more pronounced plateau at high efficiencies and low threshold values is expected. In addition, thicker sensors also lead to a reduced critical angle below the bias rail at which the particle can pass the sensor undetected. In this case, the geometric estimation reveals that only about 34 % of the PS modules would still be affected by the inefficiency between the pixel rows. Nevertheless, measurements with rotated assemblies are foreseen to be included in the next beam test as well, which will provide more detailed information about the efficiency losses in the various PS modules in the Outer Tracker of CMS.

Overall, the developed macro-pixel sensors that have been designed in the course of this thesis have shown excellent performance in lab-based and beam test studies and exceed the required radiation tolerance for operation in the CMS Outer Tracker at the HL-LHC. Only the sensitive

backside and the observed humidity dependence of the sensors would require increased caution during the measurements and the assembly procedure. However, these problems will most likely disappear with the 320 µm thick material, which has not shown any of these problems in the past. The next submission is already being processed and will serve as a last ingredient to finalize the choice of material thickness and exact sensor layout to ensure an efficient operation of the PS modules in the future CMS Outer Tracker over their full lifetime of 10 years at the HL-LHC.

Part V.

Appendix

A

Sentaurus Device Simulation

Configuration file for the Sentaurus Device Simulation tool that is used to define all necessary physics models and boundary conditions for the bias rail simulation. All static quantities, such as the electric field as well as the combined heavy ion and transient simulation are defined in this file.

```
1  Device raw {
2
3          Electrode
4          {
5                  {Name = "contactRail" voltage=0.0}
6                  {Name = "contactImplant1" voltage=0.0}
7                  {Name = "contactImplant2" voltage=0.0}
8                  {Name = "contactBackplane" voltage=0.0}
9          }
10
11         File
12         {
13                 Grid     = "@tdr@"
14         }
15
16         Physics
17         {
18                 Temperature = 293
19                 Fermi
20                 Mobility
21                 (
22                         DopingDep
23                         eHighFieldSaturation
24                         hHighFieldSaturation
25                         CarrierCarrierScattering (ConwellWeisskopf)
26                 )
27                 Recombination
28                 (
29                         SRH
30                         (
31                         DopingDependence
32                         TempDependence
33                         ElectricField(Lifetime=Hurkx
                               DensityCorrection=none)
34
35                  )
36                  CDL
37                         Auger
38                         eAvalanche (vanOverstraeten Eparallel)
39                         hAvalanche (vanOverstraeten Eparallel)
40                 )
```

```
41                  EffectiveIntrinsicDensity(Slotboom)
42
43                  HeavyIon
44                  (
45                          Direction=( !(puts [expr (sin(2*3.14*@angle@/360.0
                                ))])!,
46                          !(puts [expr (cos(2*3.14*@angle@/360.0))])! )
47                          Location=(@xi@,0)
48                          Time=1e-9
49                          Length=[0 0.001 200 200.001]
50                          Wt_hi= [1 1 1 1]
51                          LET_f= [0 1.2e-5 1.2e-5 0]
52                          Gaussian
53                          PicoCoulomb
54                  )
55          }
56
57          Physics (MaterialInterface = "Silicon/SiO2")
58          {
59                  Traps( FixedCharge Conc=@N_ox@)
60          }
61  }
62
63  System {
64
65          raw biasRail ( "contactBackplane"=bg
66                         "contactImplant1"=i1
67                         "contactImplant2"=i2
68                         "contactRail"=rail )
69          Vsource_pset v (bg 0) {dc = 0}
70
71          Resistor_pset r1s (i1 0) {resistance = 50}
72          Resistor_pset r2s (i2 0) {resistance = 50}
73
74  }
75
76  File    {
77          Output  = "@log@"
78          Plot = "@tdrdat@"
79          Current = "@plot@"
80          }
81
82
83  Plot    {
84                  eCurrent/Vector hCurrent/Vector Current/vector
85                  eDensity hDensity
86                  ElectricField ElectricField/Vector
87                  eEparallel hEparallel
88                  Potential SpaceCharge
89                  Doping DonorConcentration AcceptorConcentration
90                  Auger eAvalanche hAvalanche AvalancheGeneration
91                  eMobility hMobility
92                  SRHRecombination
93                  eInterfaceTrappedCharge
94                  hInterfaceTrappedCharge
95                  eTrappedCharge
```

```
96                  hTrappedCharge
97                  HeavyIonCharge HeavyIonGeneration
98          }
99
100 Math
101 {
102         Method = pardiso
103         Number_of_Threads = 35
104         Extrapolate
105         Derivatives
106         RelErrControl
107         Digits=4
108         Notdamped=50
109         Iterations=25
110         RecBoxIntegr (5e-3 50 5000)
111 }
112
113 Solve
114 {
115         Coupled (iterations=50 notdamped=55) { Poisson}
116         Coupled (iterations=50 notdamped=55) { Poisson Electron Hole}
117
118         QuasiStationary
119         (
120                 InitialStep = 1e-5
121                 Minstep   = 1e-10
122                 MaxStep   = 0.05
123                 Increment = 1.5
124                 Decrement = 2
125                 Goal { Parameter =v.dc voltage = @V_Bias@}
126         )
127         {
128                 Coupled
129                 {
130                         Poisson
131                         Electron
132                         Hole
133                 }
134
135         }
136
137         NewCurrentPrefix ="trans_"
138
139         Transient
140         (
141                 InitialTime = 0
142                 FinalTime = 2e-8
143                 MinStep = 1e-18
144                 MaxStep = 2e-10
145         )
146         {
147                 Coupled
148                 {
149                         Poisson
150                         Electron
151                         Hole
```

```
152                     }
153                     Plot (FilePrefix="@tdrdat@"
154                   Time=(1e-9;2e-9;3e-9;4e-9;5e-9;1e-8)
155                   NoOverwrite)
156             }
157
158 }
```

B

Macro Framework Example

Example JSON configuration file that is used as input for the python macro framework in KLayout. The following example configuration file defines the parameter set of one inner pixel of the Standard pixel layout for the full-size PS-p. All lengths are given in nanometers. In order to create a full pixel matrix, multiple instances of these pixels are generated and organized in a grid.

```
1  {
2      "Global": {
3          "symmetrical": 0
4      },
5
6      "Implant": {
7          "layer": 4,
8          "x" : 25e3,
9          "y" : 1307.5e3,
10         "r" : 10e3,
11         "x0" : 0,
12         "y0" : 27e3
13     },
14
15     "PunchThrough": {
16         "cutX": 0,
17         "cutY": 0,
18         "cutX0": 0,
19         "cutY0": 0,
20         "x0" : 0,
21         "y0" : -652e3
22     },
23
24     "Metal": {
25         "layer" : 20,
26         "overhang" : 4.5e3
27     },
28
29     "PStop": {
30         "layer" : 8,
31         "x" : 81e3,
32         "y" : 1425e3,
33         "width" : 6e3,
34         "rIn" : 25e3,
35         "x0" : 0,
36         "y0" : 1.75e3
37     },
38
39     "Via": {
40         "layer" : 15,
```

```
41          "x" : 7e3,
42          "y" : 8e3,
43          "nX" : 1,
44          "nY" : 13,
45          "dX" : 0e3,
46          "dY" : 100e3,
47          "x0" : 0,
48          "y0" : 0
49      },
50
51      "BumpPad": {
52          "layer" : 20,
53          "diameter" : 76e3,
54          "x0" : [0,0],
55          "y0" : [-58.46e3, 258.46e3]
56      },
57
58      "PassOpening": {
59          "layer" : 30,
60          "diameter" : 70e3
61      },
62
63      "Bias": {
64          "layer" : 20,
65          "x" : 12e3,
66          "y" : 35e3,
67          "x0" : 0,
68          "y0" : -705.5e3
69      }
70  }
```

C

List of utilized software packages

MeasurementControl

`https://gitlab.cern.ch/kit-cms/measurementcontrol/measurementcontrol`

A general purpose measurement control framework developed and maintained by the Institute of Experimental Particle Physics (ETP) at KIT. The software package is used to control one of the custom-made probe stations at KIT.

EUTelescope

`https://github.com/eutelescope/eutelescope`

A generic pixel telescope data analysis framework used for track reconstruction during the test beam analysis.

EUDAQ

`https://github.com/eudaq/eudaq`

A data acquisition framework used to control the test beam setup, including the EUDET telescopes at the test beam facility at CERN and DESY.

MPA Test Software

`https://gitlab.cern.ch/PS-Module_FE-ASICs/MPA_Test`

The MPA test software, developed and maintained by the chip designers. The software package is used for calibrating the chip as well as the data acquisition during the test beam measurements.

PyLayout

`https://gitlab.cern.ch/kit-cms/sensors/pylayout`

Python based design framework within the macro environment of KLayout, developed and used at KIT to create the wafer layout for the PS-p prototype.

MPA-Analysis

`https://gitlab.cern.ch/dschell/mpa-analysis`

Software package used for the Single MaPSA test beam efficiency analysis, developed at KIT.

Outer Tracker inefficiency estimator

`https://gitlab.cern.ch/kit-cms/sensors/cms-tracker-inefficiency-estimator`

Script to estimate the number of modules in the CMS Outer Tracker that are affected by inefficiencies in their active area.

List of Figures

List of Tables

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Declaration

I declare that the work in this dissertation was carried out in accordance with the requirements of the University's Regulations and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Work done in collaboration with, or with the assistance of, others is indicated as such.

Karlsruhe, April 2019

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