Product Overview

Voltage Translation Application Quick Reference

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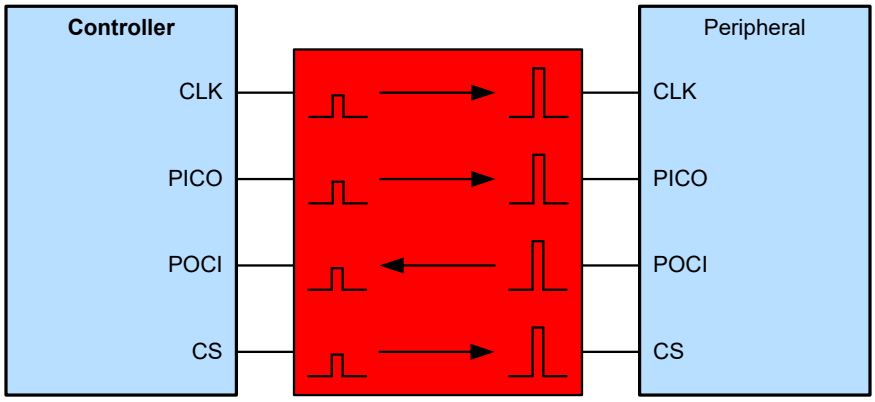
Electronic system designs are becoming more complex as systems designers strive for developing systems that are smarter, smaller, power efficient and more interconnected. Electronic system design trends are driving system designers to incorporate a wide array of microprocessors, FPGAs, and peripheral devices in order to achieve feature sets and system functionality needed by the market. As systems designers try to interconnect the different integrated circuits together, they are often confronted by the design challenge of having to connect two devices operating at two different I/O (input/output) voltage levels. Voltage level mismatches are becoming more prevalent as processor, FPGA, and microcontrollers move to lower core voltage nodes which results in their I/O voltage also scaling down to below common voltage nodes of peripheral devices. The data and control interfaces of devices on different voltage rails cannot be simply connected together and then expected to interoperate. System designers can resolve I/O voltage level differences by level shifting (level translation) the I/O of two devices to common voltage levels so that the devices can interoperate as expected.

Integrated level translation devices provide system designers an easy and cost-effective solution for resolving their system's I/O level mismatch challenges without having to compromise on performance, power, or size. Integrated level shifting solutions are available in a wide array of I/O types, bit widths, data rate ranges, current drive capabilities, and package options. Texas Instruments' portfolio of level shifter devices contains many different types of level translation functions that collectively is able to address almost any application requirement. TI's level translation portfolio includes Auto Directional, Direction Controlled, Fixed Direction, and Application Specific Level Translators in Industrial and Automotive ratings. For a list of recommended level translation devices for common interface types please see Table 1-1. For More information on all of TI's level translation solutions please visit TI's level translation landing page at www.ti.com/translation.

Table 1-1. Recommended Translator by Interface

	Translation Level	
Interface	**Up to 3.6 V**	**Up to 5.5 V**
FET Replacement	2N7001T	SN74LXC1T45 / TXU0101
1 Bit GPIO/Clock Signal	SN74AXC1T45	SN74LXC1T45 / TXU0101
2 Bit GPIO	SN74AXC2T245	SN74LXC2T45 / TXU0102
2-Pin JTAG/UART	SN74AXC2T45	SN74LXC2T45 / TXU0202
I2C/MDIO/SMBus	TXS0102 / LSF0102	TXS0102 / LSF0102
IC-USB	SN74AVC2T872 / TXS0202	NA
4 Bit GPIO	SN74AXC4T245	TXB0104 / TXU0104
UART	SN74AXC4T245	TXB0104 / TXU0204
SPI	SN74AXC4T774 / TXB0104	TXB0104 / TXU0304
JTAG	SN74AXC4T774 / TXB0104	TXB0104 / TXU0304
I2S/PCM	SN74AXC4T774 / TXB0104	TXB0104 / TXU0204
Quad-SPI	TXB0106	TXB0106
SDIO/SD/MMC	TXS0206 / TWL1200	NA
8 Bit GPIO/RGMII	SN74AXC8T245	SN74LXC8T245

1 Translate Voltages for SPI



Example SPI Voltage Translation Block Diagram

See more about this use case in the *Logic Minute* video *Voltage Translation for SPI*.

Design Considerations

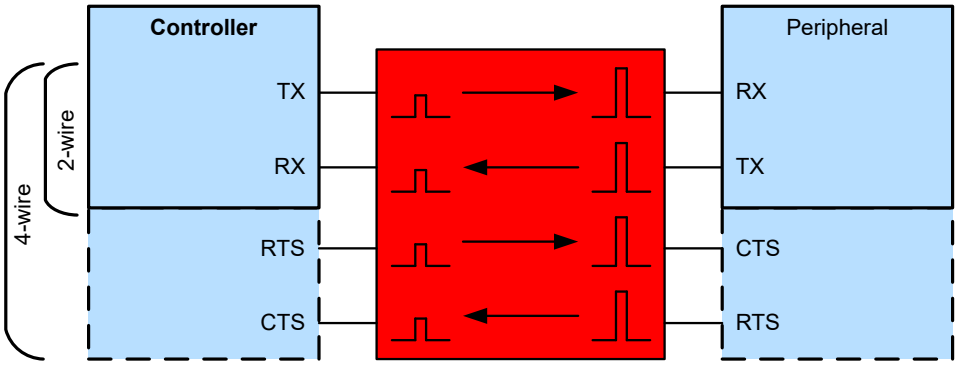
- Translators enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Protect controller while peripheral is not connected
- [FAQ] What are the power sequencing requirements for the translation device?
- [FAQ] What should be done with unused I/O pins of the level translator devices?
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*

Recommended Parts

Part Number	AEC-Q100	Voltage Translation Range	Features
TXU0304		1.1 V–5.5 V	Schmitt-trigger inputs Integrated pulldown resistors V_{CC} Isolation and V_{CC} Disconnect
TXU0304-Q1	✓		
SN74AXC4T774		0.65 V–3.6 V	Direction controlled Glitch-free power supply sequencing V_{CC} Isolation
SN74AXC4T774-Q1	✓		

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

2 Translate Voltages for UART



Example UART Voltage Translation Block Diagram

See more about this use case in the *Logic Minute* video *Voltage Translation for UART*.

Design Considerations

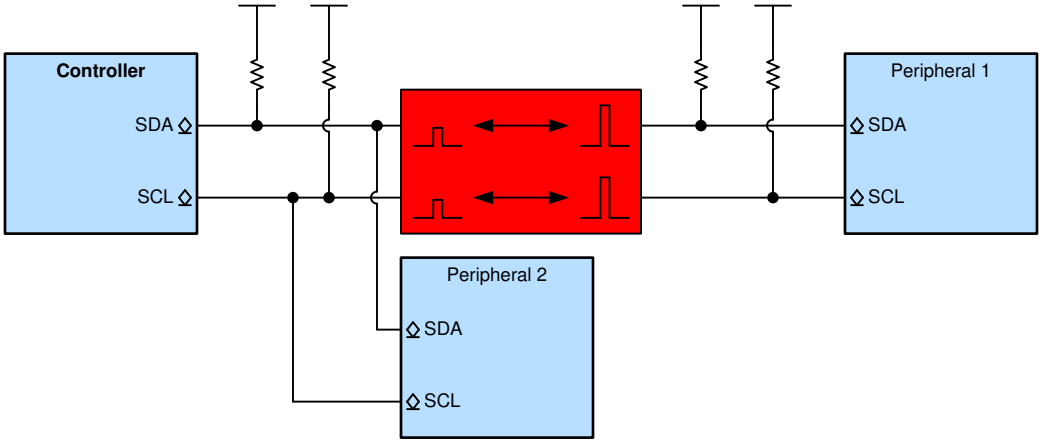
- Some devices support up to 5 Mbps UART communication; most are limited to 115 kbps or less
- Translators enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Protect controller while peripheral is not connected
- [FAQ] What are the power sequencing requirements for the translation device?
- [FAQ] What should be done with unused I/O pins of the level translator devices?
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*

Recommended Parts

Part Number	AEC-Q100	Supported UART Topology	Voltage Translation Range	Features
TXU0204		2-wire and 4-wire	1.1 V–5.5 V	Schmitt-trigger inputs Integrated pulldown resistors V_{CC} Isolation and V_{CC} Disconnect
TXU0204-Q1	✓			
SN74AXC2T245		2-wire	0.65 V–3.6 V	Direction controlled Glitch-free power supply sequencing V_{CC} Isolation
SN74AXC2T245-Q1	✓			
SN74AXC4T245		2-wire and 4-wire		
SN74AXC4T245-Q1	✓			

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

3 Translate Voltages for I²C



Example of Using Voltage Translation With an I²C Communication Bus

Design Considerations

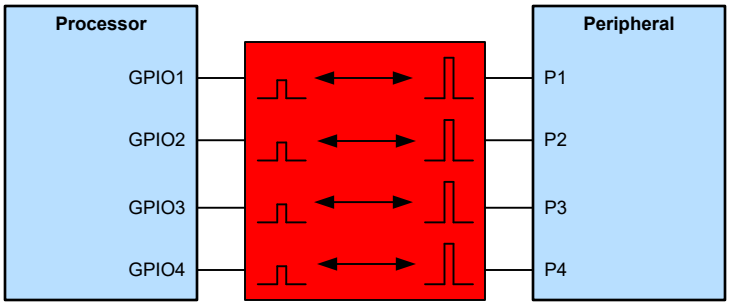
- Typical data rates can range from 100 kpbs – 3.4 Mbps
- Certain I²C modes have minimum rise time requirements that may be violated due to the edge-rate acceleration feature in the TXS family
- Enable communication when devices have mismatched logic voltage levels.
- Prevent damage to devices that cannot support higher voltage inputs.
- Improve data rates over discrete translation solutions.
- [FAQ] Why are the TXS01xx VIH/VIL specifications so stringent?
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*.

Recommended Parts

Part Number	AEC-Q100 Qualified	Voltage Translation Range	Features
LSF0102		0.95 V – 5 V	Over-voltage tolerant I/O Low R_{ON} for less signal distortion
LSF0102-Q1	✓		
TXS0102		1.65 V – 5.5 V	Edge-rate acceleration Supports Partial-Power-Down applications Integrated pull-up resistors
TXS0102-Q1	✓		

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

4 Translate Voltages for GPIO



Example GPIO Voltage Translation Block Diagram

Design Considerations

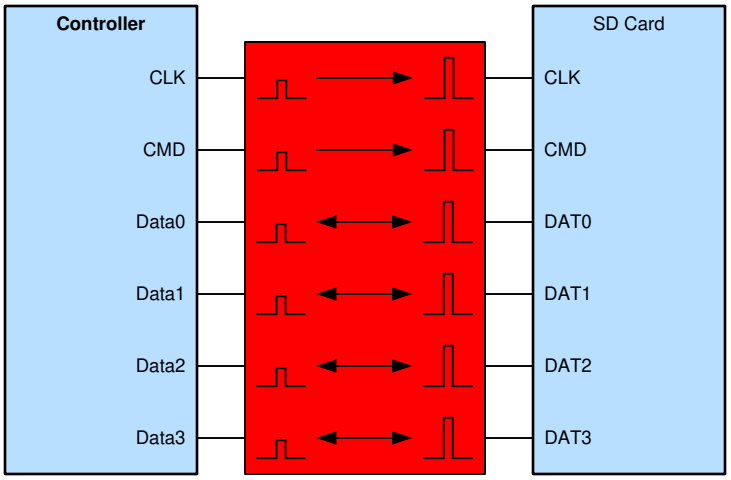
- Translators enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Protect controller while peripheral is not connected
- [FAQ] What are the power sequencing requirements for the translation device?
- [FAQ] What should be done with unused I/O pins of the level translator devices?
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*

Recommended Parts

Part Number	AEC-Q100	Bits	Voltage Translation Range	Features
SN74LXC8T245		8	1.1 V–5.5 V	Schmitt-trigger inputs Dynamic pulldowns on I/O V_{CC} Isolation and V_{CC} Disconnect
SN74LXC8T245-Q1	✓			
TXU0104		4	1.1 V–5.5 V	Schmitt-trigger inputs Integrated pulldown resistors V_{CC} Isolation and V_{CC} Disconnect
TXU0104-Q1	✓			
SN74AXC2T45		2	0.65 V–3.6 V	Direction controlled Glitch-free power supply sequencing V_{CC} Isolation
SN74AXC2T45-Q1	✓			
SN74AXC1T45		1		
SN74AXC1T45-Q1	✓			

For more devices, browse through the *online parametric tool* where you can choose between the three types of translators.

5 Translate Voltages for SDIO



Example of Using Voltage Translation With an SD Card Communication Bus

Design Considerations

- Enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Protect controller while SD Card is not connected
- [FAQ] Are there voltage level translation / level shifter device recommendations for the industry standard interfaces like GPIO, SPI, UART, I2C, MDIO, RGMII, I2S?
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*

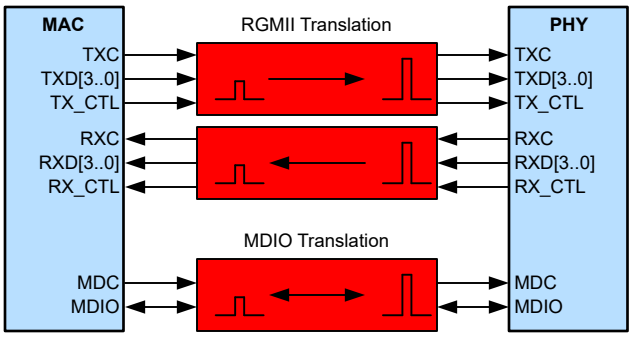
Recommended Parts

Part Number	Voltage Translation Range	Maximum Data Rate (Mbps)	Features
TXS02612	1.1 V–3.6 V	120	Enables a single SDIO port to be interfaced with two SDIO peripherals 8-kV System-level (IEC 61000-4-2) ESD protection
TXS0206	1.1 V–3.6 V	60	Auto-bidirectional Integrated EMI Filtering 8-kV System-level (IEC 61000-4-2) ESD protection
TXS0206-29	1.1 V–3.6 V	60	Auto-bidirectional Integrated 2.9 V LDO regulator 8-kV System-level (IEC 61000-4-2) ESD protection
SN74AVCA406	1.2 V–3.6 V	52	MMC, SD, Memory Stick, Smart Media, and XD-Picture Card Voltage Translation Transceiver 15-kV System-level (IEC 61000-4-2) ESD protection

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

6 Translate Voltages for RGMII

RGMII is a high-bandwidth data bus protocol with very strict timing considerations. The following device recommendations are provided as a suggested solution as they can support the data rates required for RGMII interfaces; however, because the RGMII specification is defined without consideration for voltage level translation, board-level assessment of key timing parameters and assessment of performance within the system is encouraged.



Example of Using Voltage Translation with RGMII

Design Considerations

- Board layout is critical to the success of RGMII translation; we recommend using signal integrity simulations and prototyping for any design
- Use active translators for maximum data rate
- Use one device for all TX signals and one for all RX signals to minimize channel-to-channel skew
- See *Low Voltage Translation For SPI, UART, RGMII, JTAG Interfaces* for details regarding the performance of SN74AXC8T245 in RGMII applications
- Place translators closest to the low-voltage device, if possible, to improve signal integrity
- Consider source-terminating signals if sent over 12 cm (4700 mil) or longer traces
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*

Recommended Parts

Part Number	Automotive Qualified	RGMII Voltage Translation Range	Device Maximum Data Rate (Mbps)	Features
SN74AXC8T245		2.5 V to 3.3 V	380 Mbps	Glitch-free power supply sequencing Outputs are disabled when either supply is 0 V Active translation architecture
SN74AXC8T245-Q1	✓			
SN74AVC8T245		1.8 V to 3.3 V	320 Mbps	Active translation architecture
SN74AVC8T245-Q1	✓			

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

7 Translate Voltages for MDIO

Management Data Input or Output (MDIO) is a control protocol designed primarily for use with ethernet PHY devices. It typically utilizes an unidirectional 2.5 MHz clock signal (MDC) and bidirectional data bus line (MDIO). See *Translate Voltage for RGMII* for details on the accompanying RGMII translation.

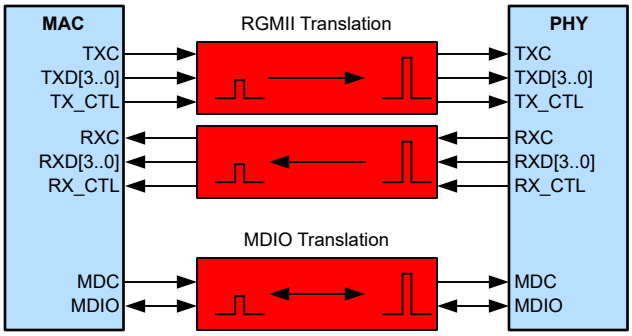


Figure 7-1. Example MAC to PHY Voltage Translation Block Diagram

See more about auto-bidirectional voltage translation in *Translation Between Communication Modules and System Controllers*

Design Considerations

- Translators enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Use a fixed-direction translator for the clock (MDC) if higher speeds are required; some newer devices use a clock as high as 50 MHz
- Open-drain compatible translators are required for the data line; although the protocol is not open-drain, pull-up resistors are required on the MDIO signal bus because there are times when the bus is not actively driven
- See answers to our most frequently asked technical questions on *[FAQ] Voltage Translators*
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*

Recommended Parts

Part Number	AEC-Q100 Qualified	Voltage Translation Range	Features
SN74AXC1T45		0.65 V – 3.6 V	Glitch-free power supply sequencing Outputs are disabled when either supply is 0 V Active translation architecture Up to 500 Mbps for 1.8 V to 3.3 V translation
SN74AXC1T45-Q1	✓		
TXS0102		1.65 V – 5.5 V	Auto-bidirectional Open-drain compatible Integrated pull-up resistors
TXS0102-Q1	✓		

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

8 Translate Voltages for a SIM Card

Subscriber Identity Modules, commonly called SIM cards, are used to store secure information in mobile devices for use in communications. This type of voltage translation applies to SIM, USIM, and UICC.

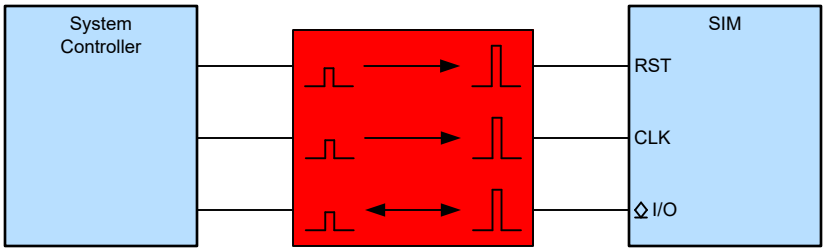


Figure 8-1. Example SIM Card Voltage Translation Block Diagram

Design Considerations

Design Considerations

- Clock signals can be up to 5 MHz
- Translators enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Protect controller while peripheral is not connected
- [FAQ] How does a slow or floating input affect a CMOS device?
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*

Table 9-1. Recommended Parts

Part Number	Automotive Qualified	Supported Card Types			Features
		Class A 5 V	Class B 3 V	Class C 1.8 V	
TXS0104E		✓	✓	✓	Auto-bidirectional voltage translation for all channels Supports all voltages and frequencies for SIM/UICC Increased ESD protection on B ports
TXS0104E-Q1	✓	✓	✓	✓	
TXS4555			✓	✓	Complete SIM/UICC translator solution Integrated LDO regulator Increased ESD protection on card-side
TXS02326A			✓	✓	Complete dual SIM/UICC translator and multiplexer solution Dual integrated LDO regulators I^2C communication with baseband processor Increased ESD protection on card-side

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

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