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Frequency Multipliers Based on a Dual-Gate Graphene FET with M-Shaped Resistance Characteristics on a Flexible Substrate

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Abstract: Frequency multipliers are essential components in communication systems, and graphene's exceptional electrical properties make it highly promising for flexible electronics. This paper addresses the technical challenges of multi-frequency multipliers based on graphene field-effect transistors (GFETs) and introduces a novel fabrication method using graphene as the channel material and metals with different work functions as the top gate. By employing Ti and Pd with distinct work functions, we develop a dual-gate GFET device that exhibits stable M-shaped resistance characteristics on a flexible polyethylene naphthalate (PEN) substrate. We demonstrate frequency doubler, tripler, and quadrupler on the flexible substrate. The results show that the GFET-based frequency multiplier offers advantages such as low operating voltage (<1 V), high voltage conversion efficiency (up to 8.4% for tripler and 6% for quadrupler), and high spectral purity (up to 88% for tripler and 76% for quadrupler). The intrinsic maximum operating frequency of the frequency quadrupler reaches 54 GHz. The use of a monolayer graphene channel, dual-metal gate control enabling an M-shaped transfer curve, and flexible characteristics all contribute to its superior performance compared to conventional devices.

Keywords: dual-gate graphene FETs; M-shaped resistance characteristics; frequency multipliers; flexible substrate

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1. Introduction

Graphene, a single-atom-thick, two-dimensional material with strong C-C covalent bonds and sp^2 hybridization, exhibits exceptional electrical and thermal properties, including ultra-high carrier mobility (2×10^5 $cm^2/V{\cdot}s$) [1], high saturation velocity (5.5×10^7 cm/s) [2], large threshold current density (2×10^8 A/cm^2) [3], and high thermal conductivity (3080–5150 W/m·K) [4]. These properties make it ideal for RF, millimeter-wave, and terahertz applications. Over the past 20 years, significant advancements have been made in graphene-based RF field-effect transistors [5], inductors [6], transmission lines [7], and analog/RF circuits (including mixers [8], amplifiers [9], and receivers [10]). Given its outstanding performance, graphene is a promising candidate for high-performance frequency multipliers. Frequency multipliers, which increase the frequency of low-frequency signals by an integer multiple to generate high-frequency signals (such as local oscillators in microwave mixers), are crucial for applications in communication, radar, imaging, and high-speed signal processing [11–15].

Frequency multipliers typically use nonlinear devices, such as diodes or field-effect transistors. A key issue with traditional multipliers is the low purity of the output spectrum; for example, a tripler's purity is often below 15% [14–18]. To extract high-order harmonic

components, expensive filters are needed to suppress unwanted harmonics. Additionally, achieving higher harmonics usually requires a multi-stage multiplier structure, increasing circuit complexity [17–21]. Output signal waveforms can also experience significant distortion and delays over a wide frequency range [15,16]. For instance, in a voltage-controlled oscillator-based multiplier, the output waveform may take several microseconds to stabilize [15].

Flexible electronic devices have made significant advances in materials, manufacturing processes, and application scenarios, providing innovative solutions for sustainable Internet of Things (IoT) systems, wearable devices, and bioelectronics [22–25]. One promising development is paper-based electronics (Papertronics), which use paper as both the substrate and dielectric layer, enabling the creation of low-power, high ON/OFF ratio transistors. This innovation opens up new possibilities for biodegradable and eco-friendly electronics [26–28]. Additionally, advances in Direct Laser Writing (DLW) have streamlined material synthesis, patterning, and device fabrication, particularly through Laser-Induced Graphene (LIG), which offers excellent conductivity and mechanical stability. LIG has been successfully applied in flexible micro-supercapacitors (MSCs) and sensing devices [29,30]. However, despite these breakthroughs, flexible electronic devices still face significant challenges in applications within the radio frequency, millimeter wave, and terahertz frequency bands.

To address these challenges, researchers have explored graphene-based frequency multipliers [31–39]. The unique bipolar properties of graphene lead to a Λ-shaped resistance curve in graphene field-effect transistors (GFETs), which can be used for frequency doubler [33,35–39]. Recent advances have been made in frequency multipliers (third and fourth harmonics) using GFETs [32,34,40,41], but their performance is still limited by high input voltage, low output voltage amplitude, and difficulties generating fourth harmonics. Kabir and Salahuddin proposed a frequency multiplier using bipolar GFETs with a simple circuit structure and no signal distortion that was verified through DC/AC simulations [15]. Wang et al. [33] demonstrated a frequency doubler with up to 90% spectral purity, though it required a higher operating voltage due to back-gated GFETs, resulting in lower voltage conversion efficiency. Later, Wang et al. [35] improved this by using top-gated GFETs, achieving a frequency doubler with low operating voltage, high conversion efficiency, and high output spectral purity. To generate higher-order harmonics, Chen and Appenzeller [34] used side-gate electrostatic doping to construct GFETs with W-shaped transfer curves, demonstrating a frequency tripler with 70% spectral purity. Cheng et al. [37] achieved third and fourth harmonic generation using double-gated GFETs with asymmetric top and back gates, with output spectral purities of 79% and 50%, respectively. The above work highlights the significant potential of graphene for frequency multipliers, including triplers and quadruplers. However, current graphene-based frequency multipliers face several challenges, such as high operating voltages (>4 V) [34,37,40], low output voltage amplitudes (~15 mV) [40], and insufficient spectral purity. A multigate paper-based FET was successfully developed, featuring a unique architecture where the paper simultaneously serves as the substrate, dielectric, and charge storage layer. It exhibits low power consumption, high stability, and multifunctional programmability; however, the environmental stability of the paper, consistency of mobility, asymmetrical structure, and manufacturing scalability still need to be optimized [25]. These limitations hinder the practical application and further development of graphene-based frequency multipliers.

Our research team previously observed an M-shaped resistance versus gate voltage (R-V_g) curve in a back-gate graphene field-effect transistor (GFET) without intentional doping [42]. This led to the experimental demonstration of frequency doublers and a tripler using the M-shaped R-V_g curve. Simulations also predicted that a frequency quadrupler could be achieved using a single back-gated GFET with a symmetrical M-shaped R-V_g curve

without requiring additional filters. However, several challenges limit the practical use of these multi-frequency multipliers: (1) Difficulty controlling the R-V_g curve shape: The output spectral purity depends on the R-V_g curve, and controlling its shape is challenging, making it difficult to achieve ideal purity for triplers or quadruplers. (2) Large input voltage amplitude: Due to weak gate control in back-gate transistors (with 100 or 300 nm SiO_2), the input voltage for the tripler is around 10 V and for the quadrupler it is 21.8 V. (3) Small output voltage amplitude: The frequency tripler output is less than 10 mV. (4) Limited back-gate structure: The back-gate configuration is global, making integration difficult. This work addresses these issues and proposes a solution: a dual-gate GFET structure with stable M-shaped resistance characteristics, enabling a multi-frequency multiplier on a flexible substrate.

In this work, we study a frequency multiplier based on graphene field-effect transistors (GFETs). The GFETs with M-shaped resistance characteristics, which are controllably achieved using dual gates with different work functions, form the basis of the device. A high-performance graphene frequency multiplier is realized on a flexible substrate using these GFETs. The circuit operates at a low voltage (<1 V), demonstrates high voltage conversion efficiency (frequency tripler: 8.4%; frequency quadrupler: 6.0%), and achieves high output spectral purity (frequency tripler: 88%; frequency quadrupler: 76%).

2. Experimental

In this work, graphene film was synthesized as the channel material for field-effect transistors (GFETs) using chemical vapor deposition (CVD) on polycrystalline copper foil (25 μm thick, 99.8% purity, Alfa Aesar) with a hydrogen, argon, and methane mixture at 1040 °C. By controlling the methane concentration (0.005 sccm) and growth time (~90 min), we obtained a uniform, wafer-scale (2 inches) monolayer graphene film (Figure S1a). Figure S1b presents the typical Raman spectra from random positions on the graphene surface at the wafer scale, characterized using optical microscopy (Olympus BX51 (Olympus, Tokyo, Japan)) and Raman spectroscopy with a 532 nm excitation wavelength. The ratio of the 2D peak to the G peak (I_{2D}/I_G) is approximately 3. The 2D peak is symmetric and can be fitted with a single Lorentzian curve, yielding a full width at half maximum (FWHM) of around 34 cm^{-1} [43,44]. These Raman features confirm that the graphene at points 1 and 2 is a monolayer. Furthermore, no significant D-peak, which would indicate defects, is observed, suggesting the graphene films are nearly defect-free.

Raman mapping was performed in the block area shown in Figure S1c, with the results presented in Figure S1d. The I_{2D}/I_G values across all points in the area range from 2.5 to 3.4. Additionally, the FWHM values of the 2D peak for each imaging point, shown in Figure S1e, range from 30 cm^{-1} to 38 cm^{-1}. These characterizations confirm that the graphene used in this work is a uniform monolayer graphene film.

The graphene was transferred to a flexible substrate using the wet transfer method with PMMA film. Polyethylene naphthalate (PEN) was chosen as the flexible substrate for GFET devices. PEN is a flexible, transparent organic polymer with outstanding chemical resistance capable of withstanding temperatures up to 200 °C and exhibiting a shrinkage rate of less than 25 ppm at 150 °C. This makes PEN ideal for flexible electronics substrates [45,46]. Flexible GFETs on PEN substrates have demonstrated high electron and hole mobilities exceeding 20,000 $cm^2V^{-1}s^{-1}$, along with excellent mobility stability. Even after over a year in ambient conditions, the mobility remains high at 7500 $cm^2V^{-1}s^{-1}$ [45].

An Al_2O_3 dielectric layer was evaporated onto the PEN surface, forming an Al_2O_3/PEN composite layer. This Al_2O_3 layer also served as an etching barrier during graphene patterning with O_2 plasma, effectively protecting the PEN substrate from damage. Figure 1 illustrates the preparation process for top-gate and dual top-gate graphene

field-effect transistors (GFETs) on flexible substrates. The fabrication process of top-gate GFETs is shown in Figure 1a–d. A single layer of graphene is transferred to the Al_2O_3/PEN composite substrate using a wet transfer method. The active region of the device is defined using electron beam lithography and oxygen plasma etching, where the graphene channel width is set between 5 μm and 10 μm and the channel length is 3 μm (Figure 1a). Next, the source and drain electrode contact areas are defined by electron beam lithography. A Pd/Au (10 nm/45 nm) metal layer is then evaporated via electron beam deposition, with excess metal removed using the lift-off process to form the source and drain contact electrodes (Figure 1b). Following this, a 3 nm layer of yttrium (Y) is evaporated and the sample is heated on a hot plate for 30 min to oxidize the yttrium into a Y_2O_3 gate dielectric layer that is approximately 5 nm thick (Figure 1c). Finally, a gate metal (Pd/Au or Ti/Au) is evaporated onto the substrate. The typical thickness of the metal layer is 10 nm for Pd or Ti and 50 nm for Au (Figure 1d).

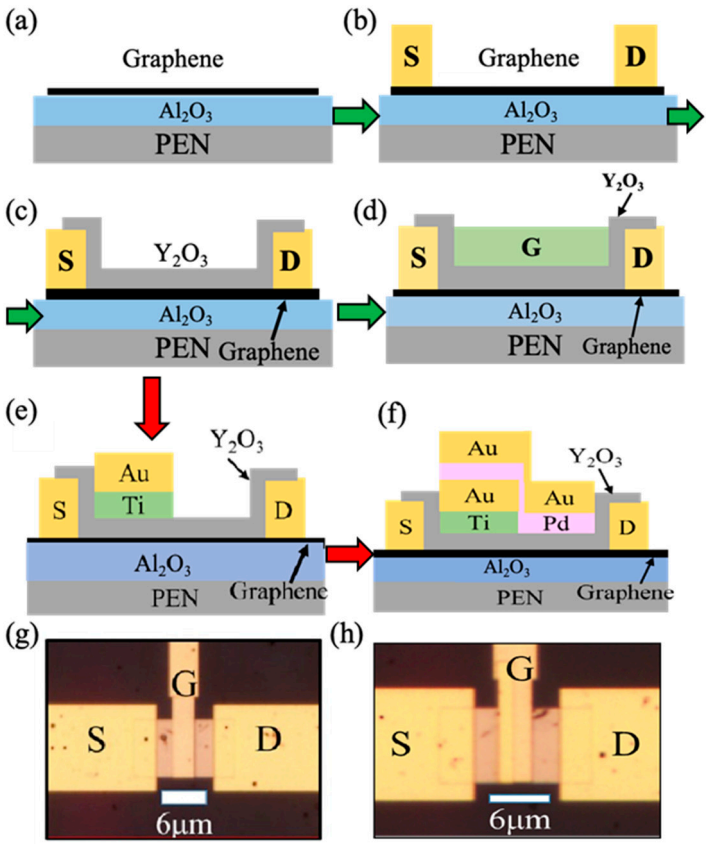

Figure 1. Schematic diagram of the process for fabricating top-gate and dual top-gate graphene field-effect transistors on a flexible substrate. (**a**) Transfer and patterning of graphene onto a flexible polyethylene naphthalate (PEN) substrate. (**b**) Fabrication of source and drain electrodes. (**c**) Deposition of the gate dielectric layer. (**d**) Evaporation of the top gate metal. Process of preparing dual top-gate graphene field-effect transistors on a flexible substrate. (**e**) Preparation of the Ti/Au top-gate electrode. (**f**) Preparation of the Pd/Au top-gate electrode. (**g**) Optical microscope image of the fabricated flexible graphene field-effect transistor. (**h**) Optical microscope images of the fabricated bimetallic gate graphene field-effect transistors (GFETs).

The fabrication process of dual top-gate GFETs is similar to the above process, with key differences in the preparation of the top gate. The graphene channel, top gate dielectric, and gate metal fabrication steps are identical to those for the flexible graphene FET, as shown in Figure 1a–c. The bimetallic gate is created using a two-step photolithography and metal evaporation process. First, the channel area is locally patterned by photolithography,

followed by the evaporation of a Ti/Au (10 nm/50 nm) layer, as shown in Figure 1e. Ti, with a work function of 4.3 eV, provides the low-work-function metal for the gate, while Au serves to prevent oxidation of the Ti layer upon exposure to air. In the second step, the entire channel area is patterned by photolithography again, followed by the evaporation of Pd/Au (10 nm/50 nm), as shown in Figure 1f. Pd, with a work function of 5.1 eV, provides the high-work-function metal for the gate, while Au increases the thickness of the gate electrode, ensuring good contact during electrical testing. Typical optical microscope images of the prepared top-gate and dual top-gate GFETs are shown in Figure 1g,h.

The morphology of the dual top-gate GFETs was characterized using optical microscopy and atomic force microscopy (AFM) (BRUKEN, León, Mexico). DC measurements were taken using a DC probe station (MPI, TS150) (MPI Corporation, Taiwan, China) and a Keysight B1500A Semiconductor Parameter Analyzer (Keysight Technologies, Santa Rosa, CA, USA). Frequency response characteristics were evaluated by biasing the GFET with an Agilent E3631A DC power supply (Agilent, Santa Clara, CA, USA), and the frequency response was measured with an Agilent 33521A function generator and Rigol DS1102CA (Beijing, China). All measurements were conducted at room temperature and atmospheric conditions.

3. Results and Discussion

3.1. Controllable Fabrication of GTETs with M-Shaped Resistance Characteristics

Controllable fabrication of graphene GFETs with M-shaped resistance characteristics (R-V_g) is essential for frequency multiplier realization. In this section, we selected a Ti and Pi dual-metal gate structure and designed GFETs with a graphene channel width-to-length ratio of 2:1 to 3:1. Let us explore how to control this fabrication process. Graphene's bipolar behavior results in GFETs typically displaying Λ-shaped resistance characteristics [38]. When two GFETs are connected in series, their output resistance is the sum of their individual Λ-shaped curves, with the resistance peaks corresponding to their Dirac points. As shown in Figure 2a, connecting two GFETs with separate Dirac point voltages in series creates an M-shaped curve. However, the following conditions must be met. (1) Dirac Point Separation: To form an M-shaped curve (Figure 2b), the Dirac point voltages of the two GFETs must be sufficiently separated. If the separation is too small, the peaks merge into a single resistance peak, resulting in a Λ-shaped curve (Figure 2c). (2) Similar Resistance Peak Heights: The resistance peaks of both GFETs should be of similar magnitude. If one peak is too small, it will have little effect on the total resistance and the curve will remain Λ-shaped (Figure 2d).

The peak resistance can be controlled by adjusting the relative lengths of the GFET channels, as resistance is proportional to the ratio between channel width and length. Therefore, the key challenge in fabricating GFETs with M-shaped resistance characteristics is generating two GFETs with separate Dirac point voltages and controllably adjusting the distance between them. In essence, controlling the position of the Dirac point voltage is crucial for achieving M-shaped resistance characteristics in GFETs.

A common approach to adjusting the Dirac point voltage of GFETs is doping the graphene channel [47–51], which modulates graphene's Fermi level and controls the Dirac point voltage. However, doping faces three key challenges: (1) Reduced carrier mobility: Doping lowers graphene's carrier mobility, impairing the high-frequency performance of devices [47]. (2) Unstable performance: Surface doping can cause performance instability and unreliability [52]. (3) Complex process: Current doping techniques are intricate and lack precision for local control [53]. In silicon-based transistors, the threshold voltage is regulated by the gate metal work function. Given the analogy between the Dirac point voltage in GFETs and the threshold voltage in silicon-based transistors, it is hypothesized

that adjusting the gate metal's work function can similarly control the Dirac point voltage of GFETs.

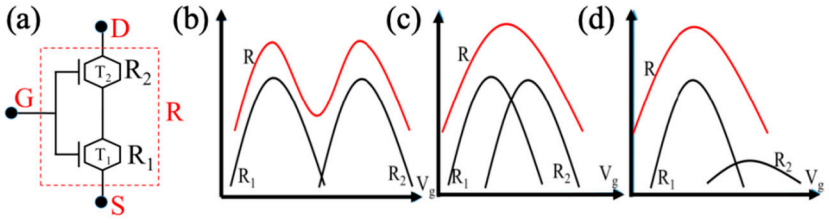

Figure 2. Schematic of two GFETs with Λ-shaped resistance-gate voltage (R-V_g) curves connected in series to form an M-shaped electrical characteristic curve. (**a**) Equivalent circuit diagram of series-connected GFETs, where R_1 and R_2 represent the resistances of the two GFETs with separated Dirac point voltages and R is their total series resistance. (**b**) Two GFETs with separated Dirac points connected in series to create an M-shaped R-V_g curve. (**c**) Insufficient separation between Dirac points of series-connected GFETs. (**d**) One of the resistance peaks in the series-connected GFETs is too small.

To verify the hypothesis, graphene field-effect transistors (GFETs) with different metal top gates were fabricated on the same flexible substrate. The top gate metals used were 10 nm thick Ti or Pd. To prevent oxidation and improve conductivity, both metals were capped with 50 nm thick Au. Figure 3a illustrates a schematic of the flexible GFET structure, with the detailed fabrication process outlined in Figure 1.

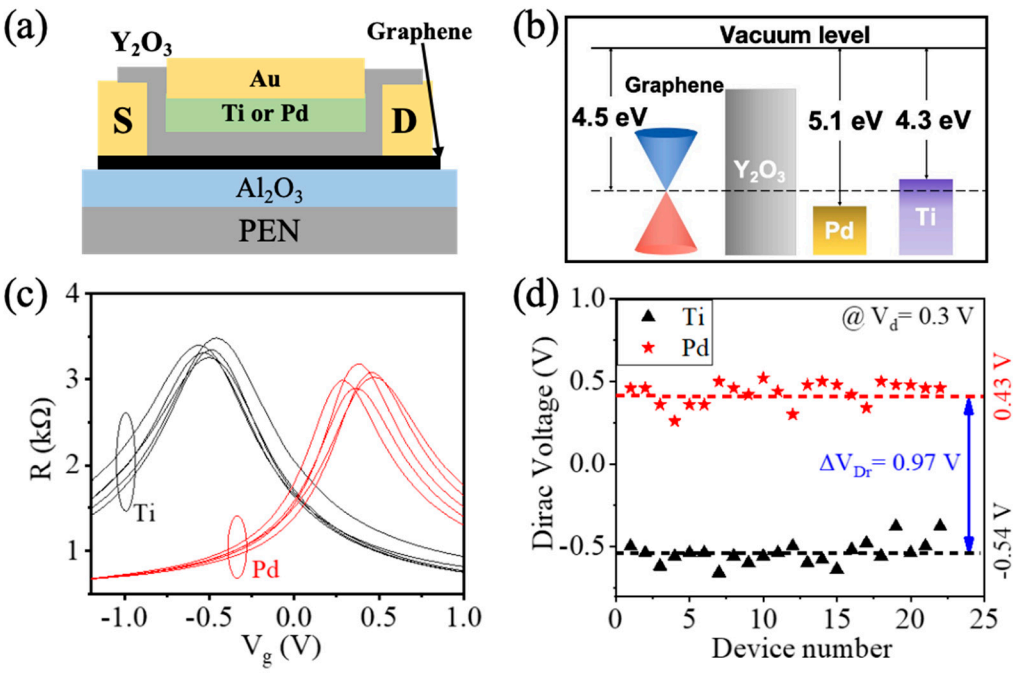

Figure 3. GFETs with metal top gates of varying work functions on a flexible substrate. (**a**) Structure of the metal gate GFET. (**b**) Work function distribution for graphene, gate oxide, Ti, and Pd. (**c**) R-V_g curves comparison of Ti and Pd top gate metals (gate length: 3 μm, width: 5 μm, V_d: 0.3 V). (**d**) Dirac point voltage statistics for GFETs with Ti and Pd gate metals.

Figure 3c presents a comparison of the transfer characteristics (R-V_g) curve of graphene field-effect transistors (GFETs) with top gate metals of 10 nm Ti and Pd, both covered with a 50 nm thick Au layer. Each device was tested five times. The Dirac point voltage of Ti metal gate devices is negative, while for Pd metal gate devices, it is positive, with a clear separation between the two. Figure 3d shows the Dirac point voltage distribution for Ti/Au

and Pd/Au metal gate devices. The average Dirac point voltages for Ti and Pd metal gate GFETs are −0.54 V and +0.43 V, respectively, with a difference ($|\Delta V_{dr}|$) of 0.97 V.

The work function of Ti is 4.3 eV, which is smaller than that of graphene (4.5 eV [52]), implying that the Fermi level of graphene is lower than that of Ti. As a result, using Ti as the metal gate for the graphene channel induces electron accumulation in the channel, as shown in Figure 3b. In contrast, the work function of Pd (5.1 eV [52]) is higher than that of graphene, meaning the Fermi level of graphene is higher than that of Pd. When Pd is used as the metal gate, hole accumulation occurs in the graphene channel. Therefore, the Pd metal gate induces hole accumulation, while the Ti metal gate induces electron accumulation in the graphene channel. This explains the experimental observation that the Dirac point voltage for Pd metal gate GFETs is located at a more positive voltage compared to that for Ti metal gate GFETs.

It is now established that an M-shaped resistance characteristic curve can be generated by connecting two Dirac point voltage-separated GFETs in series. But how can we achieve this connection? When two independent transistors are connected in series, there are four contact resistances (two source and two drain resistances). The contact resistance between graphene and metal is typically high (up to 1000 Ω·μm [54]). Furthermore, even with the same contact metal, the contact resistance can fluctuate significantly. For example, with Pd as the contact metal, the contact resistance ranges from 69 to 1000 Ω·μm [55–57].

To achieve the M-shaped resistance–gate voltage (R-V_g) curve while minimizing the impact of contact resistance, this study introduces a dual-gate GFET structure. By using two different metal gates with different work functions, the Dirac point voltages of the graphene channels are separated, producing the desired R-V_g curve. Unlike series-connected GFETs, this structure reduces the number of contact resistances to two (one source and one drain), significantly improving device performance. The schematic diagram of the dual-gate device is shown in Figure 4a.

The dual top gate was fabricated using Ti and Pd, with gate lengths denoted as L_{Ti} and L_{Pd}, respectively. The fabrication process is provided in Figure 1. The deposition of 10 nm Ti and 50 nm Au films was first performed, followed by the deposition of 10 nm Pd and 50 nm Au films (Figure 4b). Ti serves as a low-work-function gate, Pd as a high-work-function gate, and Au prevents Ti oxidation while enhancing gate thickness for reliable probe contact during electrical testing. A typical optical microscope photo of the dual-gate GFET is shown in Figure 4c.

The dual-gate GFET device can be modeled as two GFETs with different metal gates connected in series. The total resistance is given by $R = R_{Ti} + R_{Pd} + 2R_c$, where R_{Ti} and R_{Pd} are the channel resistances under the Ti and Pd gates, respectively, and R_c is the constant contact resistance between the graphene and the source or drain electrode (unaffected by the gate voltage). R_{Ti} and R_{Pd} are proportional to the channel lengths under the respective gates, allowing R to be tuned by adjusting these lengths.

To investigate this, we fabricated dual-gate GFETs with three length ratios of L_{Ti} (Ti gate) to L_{Pd} (Pd gate): 2 μm/1 μm, 1 μm/2 μm, and 1.5 μm/1.5 μm. Atomic force microscopy (AFM) images and height profiles (showing electrode thickness and length) are presented in Figure 4d,f,h. The corresponding R-V_g curves, shown in Figure 4e,g,i, display M-shaped resistance characteristics for all devices but differ in peak heights and symmetry: (1) L_{Ti}/L_{Pd} = 2 μm/1 μm: Asymmetrical curve with a higher resistance peak on the Ti side (Figure 4e). (2) L_{Ti}/L_{Pd} = 1 μm/2 μm: Asymmetrical curve with a higher resistance peak on the Pd side (Figure 4g). (3) L_{Ti}/L_{Pd} = 1.5 μm/1.5 μm: A symmetrical curve with comparable peak heights on both sides is shown in Figure 4i.

These results demonstrate that dual-gate technology not only enables GFETs to exhibit M-shaped resistance curves but also allows precise control over curve symmetry through

gate length adjustments. By varying the gate length, the curve's shape and symmetry can be fine-tuned, improving the spectral purity of both the tripler and quadrupler outputs. Thus, dual-gate GFETs with M-shaped resistance characteristics provide a structural foundation for graphene-based frequency multipliers.

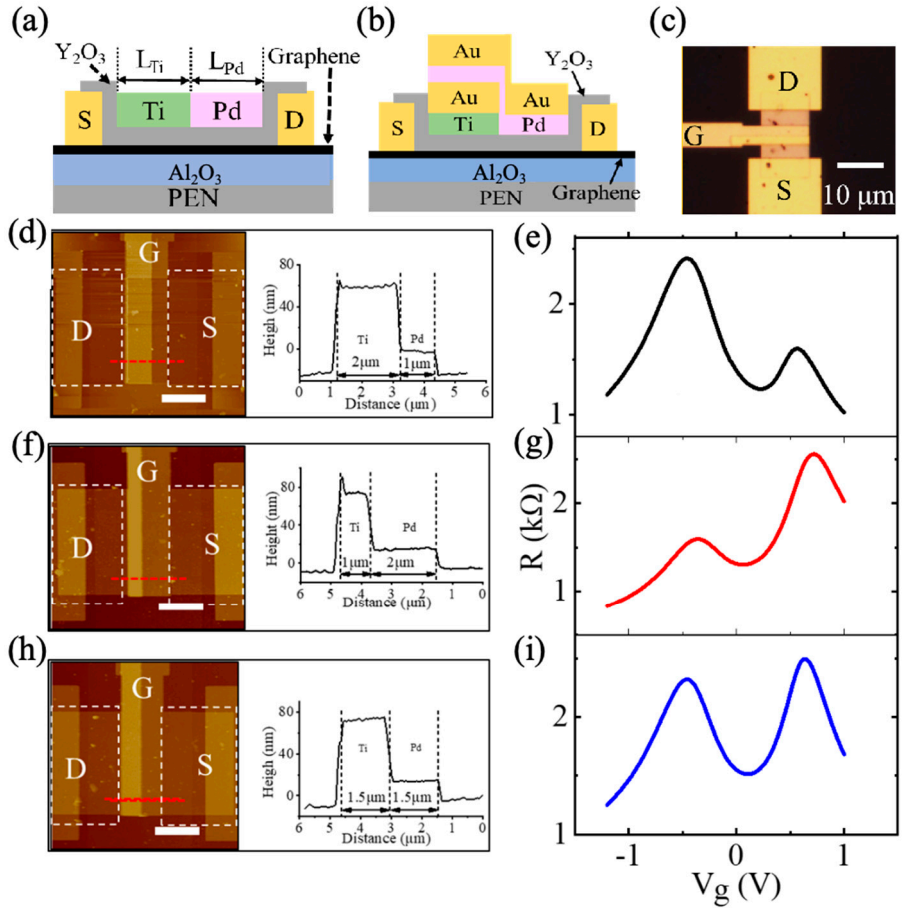

Figure 4. Dual-gate flexible GFETs and their electrical characteristics. (**a**) Simplified structure of the dual-gate GFET, with L_{Ti} and L_{Pd} representing the lengths of the Ti and Pd top grids. (**b**) Full structure of the dual-gate GFETs. (**c**) Optical microscope image of a typical device. (**d**,**f**,**h**) AFM images of three devices with different L_{Ti} to L_{Pd} ratios (scale: 3 μm), showing height profiles along the red line. (**e**,**g**,**i**) Resistance curves of devices with varying L_{Ti} to L_{Pd} ratios, where D, S, and G represent the drain, source, and gate electrodes, respectively.

3.2. Stability of M-Shaped R-V_g Curves in Dual-Gate GFETs on a Flexible Substrate

The stability of dual-gate graphene field-effect transistors (GFETs) under substrate bending is crucial for developing high-performance multifrequency devices on flexible substrates. To evaluate this, we tested the electrical properties of dual-gate GFETs on a flexible PEN substrate. The substrate, with an array of GFETs, was attached to half-cylinders of varying radii and placed on a DC probe station for electrical measurements (Figure 5a). All tests were performed at room temperature under ambient conditions.

We chose dual-gate GFETs with equal Ti and Pd gate lengths of 1.5 μm (L_{Ti}/L_{Pd} = 1.5 μm/1.5 μm) due to their superior spectral purity in generating frequency multipliers with symmetrical M-shaped resistance curves [42]. The bending direction was aligned parallel to the GFET channel (Figure 5b) to maximize the mechanical strain effect and evaluate the strain tolerance of the devices [45,58].

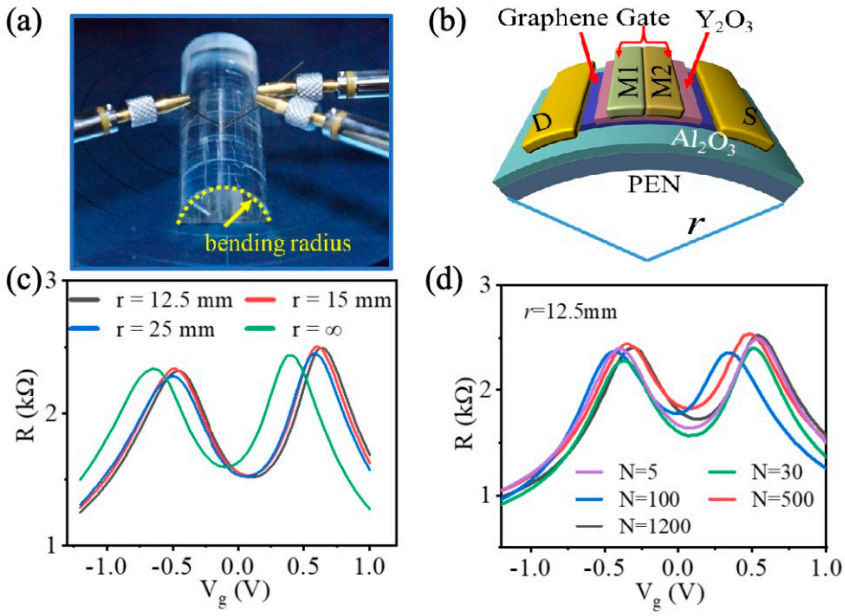

Figure 5. Effect of flexible substrate bending on the electrical characteristics of dual-gate GFETs. (**a**) Photos of flexible substrate with GFET array attached to a semi-cylindrical surface for electrical testing. (**b**) Schematic of device bending, with r representing the bending radius and M1 and M2 indicating the two top-gate metal layers. (**c**) Effect of bending radius on the electrical characteristics (R-V_g curve, V_d = 0.3 V). (**d**) Effect of bending cycles (N) on the electrical characteristics of GFETs (R-V_g curve V_d = 0.1 V).

Figure 5c shows the impact of various bending radii on the R-V_g curves of dual-gate GFETs. When the bending radius was reduced to 12.5 mm, the devices continued to function properly. The strain induced by bending can be calculated as $\delta = (d_1 + d_2)/2r$, where δ is the strain, d_1 is the substrate thickness, d_2 is the device thickness, and r is the bending radius [59]. Given that the GFET thickness is negligible compared to the 125 µm PEN substrate, the tensile strain at a 12.5 mm radius was approximately 0.5%. This strain level is well within the range suitable for flexible device applications [45,60]. Furthermore, bending caused only a slight peak shift in the dual resistance values without significantly altering the shape of the R-V_g curve, demonstrating that dual-gate-GFET-based multipliers retain their characteristic symmetrical M-shaped resistance curves under bending.

The shift in the I-V curve after bending may result from tensile strain applied to the graphene when the substrate bends outward. This strain modifies the π-bonding and band structure, shifting the Dirac point toward positive gate voltages and inducing p-type behavior [61,62]. Additionally, the strain affects gate coupling, altering electrostatic gating efficiency and further shifting the Dirac point and I-V curve.

The effect of repeated bending cycles on the electrical properties is shown in Figure 5d. After 1200 bending cycles with a 12.5 mm radius, the devices remained fully operational. Even under extensive bending fatigue tests, the symmetrical M-shaped R-V_g curves persisted, with only minor shifts in the peak positions. These results confirm that dual-gate GFETs maintain stable performance and functionality after at least 1200 bending cycles.

3.3. Performance of Frequency Multiplier Using Dual-Gate GFETs on Flexible Substrates

Next, we fabricated frequency multipliers using the prepared dual-gate flexible GFETs and evaluated their electrical performances. The testing setup, illustrated in Figure 6a, involved a function generator supplying an input signal of amplitude Am and frequency f_0, along with a DC bias voltage, V_{bias}. A load resistor R_L was connected in series with the drain terminal to a DC power supply (VC), while the source terminal was grounded. Real-

time input (gate) and output (drain) signals were monitored using a dual-channel digital oscilloscope. All tests were conducted at room temperature and atmospheric pressure, with the device subjected to a bending radius of 12.5 mm (~0.5% tensile strain). For high spectral purity, we selected dual-gate GFETs with L_{Ti}/L_{Pd} = 1.5 μm/1.5 μm for the demonstration. The test method and DC bias voltages (V_g) for frequency multiplier testing are outlined in Figures S3–S5.

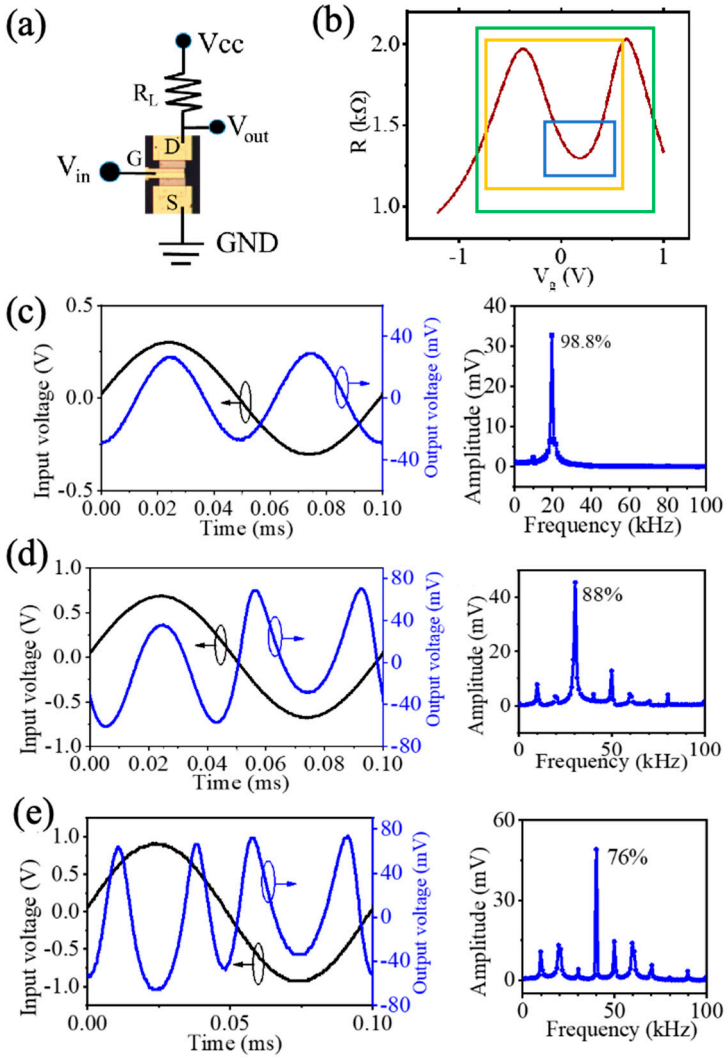

Figure 6. High-performance frequency multipliers using dual-gate flexible GFETs. (**a**) Schematic of the test circuit. (**b**) R-V_g curve of the selected GFET device. The blue, yellow, and green boxes respectively show one operating regions for the second, third, and fourth harmonics. (**c**) Input/output voltage curves and frequency spectrum of the doubler. (**d**) Input/output voltage curves and frequency spectrum of the tripler. (**e**) Input/output voltage curves and frequency spectrum of the quadrupler.

3.3.1. Second Harmonic Generation

The device's R-V_g curve (Figure 6b) reveals an M-shaped resistance profile, distinct from conventional GFETs with Λ-shaped R-V_g curves [35,38]. This M-shaped curve features three operating regions: two peaks and one valley. When the device operates in the valley region (blue box in Figure 6b), the input–output characteristics and output frequency spectrum (Figure 6c,d) show a second harmonic spectral purity of 98.8%. If operating in the peak regions, second harmonic purities of 93.7% and 95.5% are observed (Supplementary Information: Figure S3d,h). Notably, the valley output signal is 180 degrees out of phase with the peak outputs (Figure S3c,e,g), a unique behavior not

previously reported [31,38]. This dual-mode capability—producing either in-phase or out-of-phase outputs—offers significant potential for future communication circuits requiring frequency or phase modulation.

3.3.2. Frequency Tripler Generation

Operating the device in the purple square region in Figure 6b, including a resistance peak and valley, produces triple-frequency generation; the input–output and frequency spectrum curves are shown in Figure 6d. The spectral purity of the third harmonic reaches 88%. This tripler functionality is achievable in two distinct regions (Supplementary Figure S4b), with one region delivering an 84% spectral purity (Supplementary Figure S4f). As with the second harmonic, the third harmonic also exhibits two working modes (in-phase and out-of-phase outputs) based on the operating region, as demonstrated in Supplementary Figure S4c,e. This marks the first experimental demonstration of a graphene-based GFET tripler with two distinct operating modes [34,37,40].

3.3.3. Fourth Harmonic Generation

The quadrupler, which relies on two peak resistance values, has a single operating region (green box in Figure 6b). The test results in Figure 6e confirm that the input signal is converted into four output signals, achieving quadruple-frequency generation. The fourth harmonic spectral purity reaches 76%, significantly exceeding previously reported values of 50% [37].

Eleven dual-metallic-gate flexible GFETs with symmetrical M-shaped R-V_g curves were selected for frequency multiplier tests (Figure S2). The R-V_g curves exhibited a slight drift (<0.5 V) in the double peaks. The spectral purity ranges we measured for the second, third, and fourth harmonics were 99–93%, 94–84%, and 72–76%, respectively.

3.3.4. Characteristics of Frequency Multiplier Using Dual-Gate GFETs on Flexible Substrate

Graphene's exceptionally high carrier mobility and saturation velocity enable the dual-gate flexible GFET frequency multiplier to achieve high-frequency operation. As shown in Figure 7a, the output signal amplitude remains stable (approximately 50 mV) for input frequencies below 20 kHz in quadrupler mode. However, when the input frequency (f_0) surpasses 20 kHz, the output amplitude begins to drop sharply, eventually reaching about 3.3 mV at 1 MHz. This decline is primarily due to the capacitance of the test cable used with the DC probe station.

The equivalent output circuit (Figure 7b) comprises the gate capacitance ($C_g \approx 0.3$ pF), the GFET output resistance ($R \approx 2$ kΩ), and the test cable's parasitic capacitance (C_{para}). A 4 m cable, with a capacitance of about 0.1 nF/m, contributes approximately 0.4 nF of parasitic capacitance. Figure 7c compares the measured amplitude–frequency responses (black dots) of the fourth harmonic with simulated results based on the equivalent circuit (solid red line). The close agreement confirms that parasitic cable capacitance (C_{para}) limits the test results and masks the device's intrinsic maximum operating frequency.

The intrinsic maximum operating frequency is given by the 3 dB cut-off frequency (f_c), which depends on the output resistance and gate capacitance: $f_c = 1/2\pi RCf$ [35–37,40]. Excluding cable parasitics and using $C = C_g \approx 0.15$ pF, the estimated f_c is around 0.54 GHz. Reducing the channel length lowers both R and C_g, significantly boosting f_c. For instance, if the gate length is shortened from 3 μm to 300 nm, R decreases to approximately 0.2 kΩ, C_g drops to about 0.015 pF, and fc increases to roughly 54 GHz. These findings highlight the potential of dual-gate flexible GFET frequency multipliers for RF, microwave, and terahertz applications.

However, to achieve accurate high-frequency measurements and fully exploit these enhanced f_c values, it is essential to minimize the impact of parasitic capacitance. Several

strategies can be employed to mitigate these effects. For example, shortening test cables or using low-capacitance cables can reduce parasitic capacitance, while on-chip compensation circuits can help counteract these effects. Additionally, improving grounding and shielding is critical for reducing noise and interference, particularly at higher frequencies, ensuring reliable performance in high-speed applications.

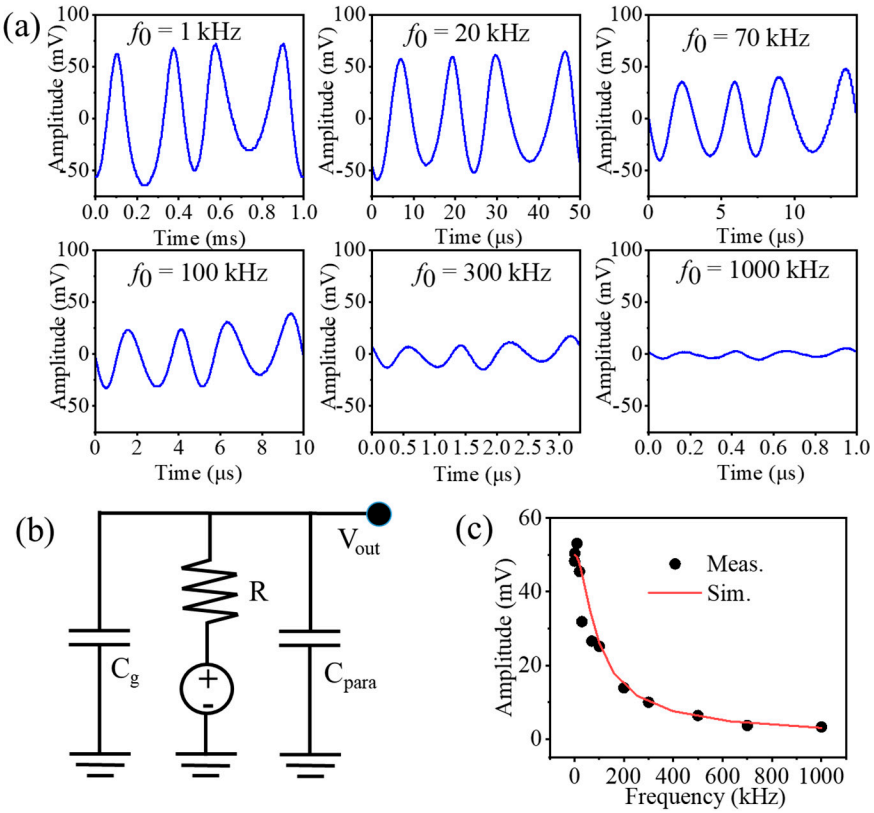

Figure 7. Frequency response of multiple frequency multipliers limited by cable capacitance. (**a**) Output signal variation with input frequency in quadrupler mode. (**b**) Equivalent circuit. (**c**) Comparison of amplitude-frequency response (black dots) and simulation results (solid line) for the quadruple frequency output signal.

Finally, we analyzed the characteristics and advantages of dual-gate flexible GFETs for multifrequency conversion. Key performance metrics were compared against previously reported graphene-based multipliers, as summarized in Table 1.

Frequency Doublers: Compared to traditional doublers based on Λ-shaped resistance (R-V_g) GFETs [33,35,45], the dual-gate flexible GFET doubler presented here offers three selectable operating regions and three optimal gate bias points, providing greater flexibility. When operating in the middle resistance valley region, the doubler's output waveform is out of phase with the input, producing two distinct modes (in-phase and out-of-phase output) that were not previously reported.

Frequency tripler and quadrupler: The dual-gate flexible GFET-based harmonic generators provide three notable advantages over earlier works [34,37,40,41]: (1) Adjustable R-V_g Curve Shape: By altering the dual-gate lengths, the R-V_g curve shape can be adjusted, resulting in higher spectral purity. The fourth harmonic generator in this work achieved 76% spectral purity, far exceeding the previously reported maximum of 54.3%. (2) Top-Gate Device Benefits: This is the first demonstration of a top-gate frequency multiplier. It operates at low voltages (<1 V) and delivers high output amplitudes (46 mV for the third harmonic, 53 mV for the fourth harmonic), as well as superior output-to-input voltage ratios (8.4% for the third harmonic, 6% for the fourth harmonic). (3) Ease of Integration and

Flexibility: The top-gate structure enables straightforward integration, and this work is the first to realize GFET-based frequency multipliers on a flexible substrate.

Table 1. Performance comparison of GFET-based frequency multipliers.

Device Structure	Substrate	Multiplication Type	Amplitude of V_{in}	Amplitude of V_{out}	Spectrum Purity	References
Bottom gate	SiO_2/Si	Doubler	~8 V	<40 mV	94%	[33]
Top gate	PEN	Doubler	0.3 V	~62.5 mV	96.6%	[45]
Top gate	SiO_2/Si	Doubler	0.4 V	<20 mV	>90%	[35]
Bottom gate	SiO_2/Si	Tripler	4 V	-	70%	[34]
Bottom gate	SiO_2/Si	Tripler	6.5 V	~15 mV	94%	[40]
Dual gates	SiO_2/Si	Tripler Quadrupler	7 V 10 V	- -	79% 50%	[37]
Bottom gate	SiO_2/Si	Tripler Quadrupler	10 V 21.8 V	<10 mV <15 mV	80% 39.9%	[42]
Top gate	SiO_2/Si	Double	0.3 V	20 μV	98.2%	[6]
Top gate	SiO_2/Si	Double Tripler Quadrupler	0.25 V	-	60.65% 56% 54.3%	[8]
Dual gate metals, top gate	Plastic (PEN)	Doubler Tripler Quadrupler	0.3 V 0.7 V 0.9 V	~33 mV ~46 mV ~53 mV	98.8% 88% 76%	This work

4. Conclusions

This work addresses the challenges of multi-frequency multipliers based on graphene field-effect transistors (GFETs) and introduces a novel fabrication method that uses graphene as the channel material and metals with different work functions as the top gate. A Ti/Pd dual-gate structure on a flexible PEN substrate, with an optimized gate length ratio, enables the creation of GFET devices that exhibit stable M-shaped resistance characteristics and can withstand repeated bending (1200 cycles, strain ~0.5%). Frequency doubling, tripling, and quadrupling are demonstrated on this flexible substrate. The graphene-based frequency multiplier offers several advantages: low operating voltage (0.3–0.9 V), high output voltage amplitude (up to 46 mV for the tripler and 53 mV for the quadrupler), high voltage conversion efficiency (up to 8.4% for the tripler and 6% for the quadrupler), and high spectral purity (up to 88% for the tripler and 76% for the quadrupler). The intrinsic maximum operating frequency of the frequency quadrupler reaches 54 GHz.

Additionally, the dual-gate flexible GFETs provide multiple operating regions (three for doublers and two for triplers) and allow flexible tuning of the optimal gate DC bias point. The frequency doubler and tripler also offer two operational modes with the input: in-phase or reverse-phase. This work demonstrates not only high performance but also excellent stability and reproducibility. The bimetallic-gate GFET devices maintain consistent performance even after repeated bending cycles, and the spectral purities for the second, third, and fourth harmonics (99–93%, 94–84%, and 72–76%, respectively) further confirm their stability across multiple tests and devices. Overall, this GFET-based flexible frequency multiplier offers high-performance signal processing in lightweight, adaptable devices, making it a promising solution for wearable electronics and portable systems.

Supplementary Materials: The following supporting information can be downloaded at: https://www.mdpi.com/article/10.3390/electronics14040803/s1, Figure S1: The Raman spectral characterization of graphene; Figure S2: Symmetrical M-shaped R-V_g curves for frequency multiplier testing in dual-gate graphene FETs on a flexible substrate; Figure S3: Multi-area operation mode of frequency doubler; Figure S4: Multi-area operation mode of frequency tripler; Figure S5: Bias stress testing data.

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