Design Strategy for Barrel Shifter Using Mux at 180nm Technology Node

Vaibhav Neema, Pratibha Gupta

Abstract— The reversible logic has the promising applications in emerging computing paradigm such as quantum computing, quantum dot cellular automata, optical computing, etc. In reversible logic gates there is a unique one-to-one mapping between the inputs and outputs. Barrel shifter is an integral component of many computing systems due to its useful property that it can shift and rotate multiple bits in a single cycle. The design methodologies considered in this work targets 1.) Reversible logical right shifter, 2.) Reversible universal right shifter that supports logical right shift, arithmetic right shift and the right rotate, 3.) Reversible bidirectional logical shifter, 4.)Reversible bidirectional arithmetic and logical shifter, 5) Reversible universal bidirectional shifter that supports bidirectional logical and arithmetic shift and rotate operations.

Index Terms— Low power, Power Dissipation.

I. INTRODUCTION

Reversible logic is a logic design style in which there is a one to one mapping between the input and the output vectors. Each design is a compromise between gate count and critical path latency. In an attempt to reduce both, the proposed designs utilize a number of innovative design techniques. The techniques can be divided into two categories: those addressing uni-directional result computation and those providing the logic necessary to implement all operations with uni-directional hardware support. Barrel shifter is an integral component of many computing systems due to its useful property that it can shift and rotate multiple bits in a single cycle. Barrel shifter and rotate perform many logical operation which are useful in designing of digital signal processors and others type of processors.

II. DESIGNING OF MULTIPLEXER CIRCUIT

A. Nmos 2:1 mux

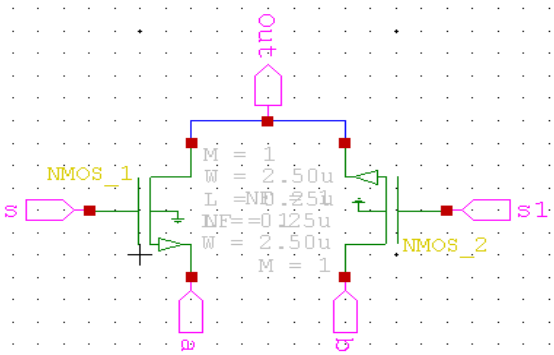

Figure 1 Schematic of NMOS 2:1 MUX

The above figure 1 shows schematic of NMOS 2:1 MUX. The select lines are s and s1, and inputs are a and b. Select lines are connect to gate.

B. Cmos 2:1 mux

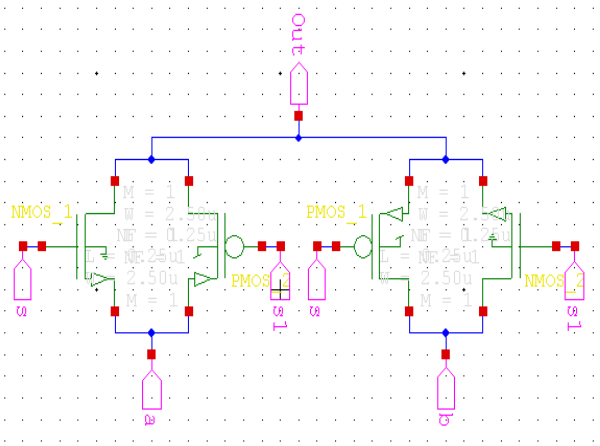

Figure 2 Schematic of CMOS 2:1 MUX

The above figure 2 shows schematic of CMOS 2:1 MUX based Double Pass Transistor Logic [4] which eliminates some of the inverter stages required for complementary pass transistor logic by using both N and P channel transistors, with dual logic paths for every function. While it has high speed due to low input capacitance, it has only limited capacity to drive a load [4].The select lines are s and s1, and inputs are a and b. Select lines are connect to gate. It consist two pair of NMOS and PMOS are connecter.

C. Msl 2:1 mux

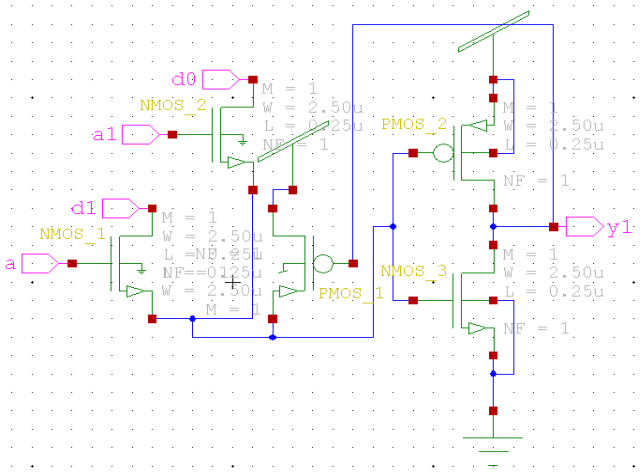

Figure 3 Schematic of MSL 2:1 MUX

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Figure 3 shows MSL 2:1 mux, MSL stands for multiplexer single with level restoration block. One problem with the CPL or DPL circuits is the requirement of both non-inverting and inverting signals, which leads to a large wiring area [6], [12]. A new logic design based on CPL like circuit called MSL arises, which uses only the non-inverting output of the original CPL multiplexer circuit appended by a p-latch inverter which is the heart of this circuit [2], [8].For this circuit output is y1, a and a1 are select line, d1 and d0 are data input.

D. Md 2:1 mux

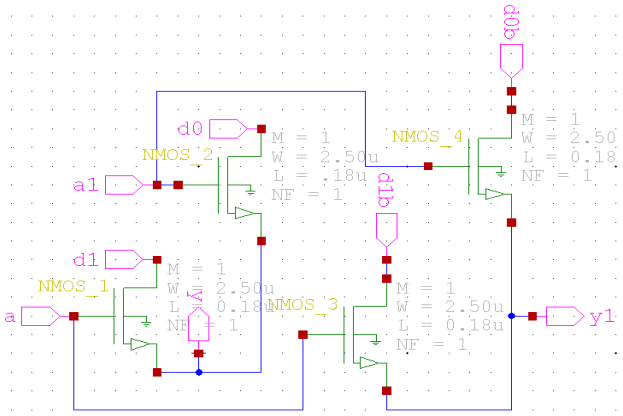

Figure 4 Schematic of MD 2:1 MUX

The above figure 4 shows the circuit of MD 2:1 mux, the MD means for Multiplexer Double [6]. In this circuit a and a1 are select lines, d1 and d0 are data input lines and y and y1 are output and its inverted output respectively. Because we get output and its inverted output its name is MD.
Figure 2.6 Circuit diagram of MD 2:1 MUX.

E. Mdl 2:1 mux

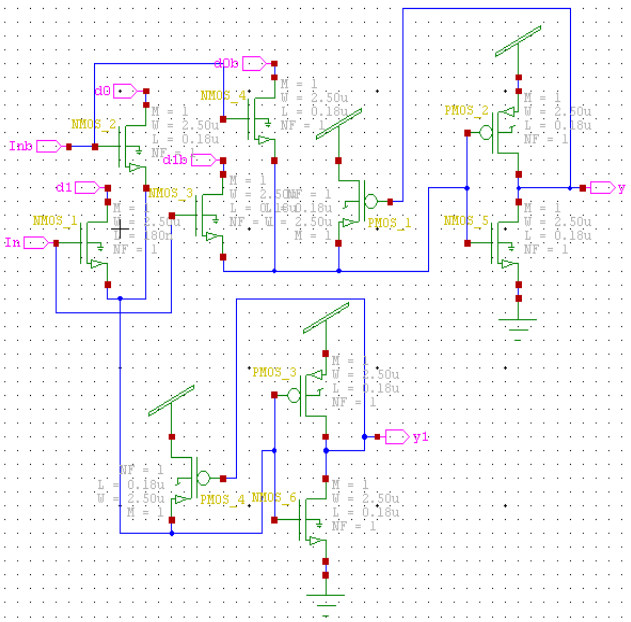

Figure 5 Schematic of MDL 2:1 MUX

Figure 5 is of MDL 2:1 mux circuit. MDL stands for multiplexer double with level restoration block. The restoration block can avoid swing problems this is the main advantage of this circuit. This circuit contains large number of MOS device so it consumes high power and required high-area [2], [4].

F. Dcvsl 2:1 mux

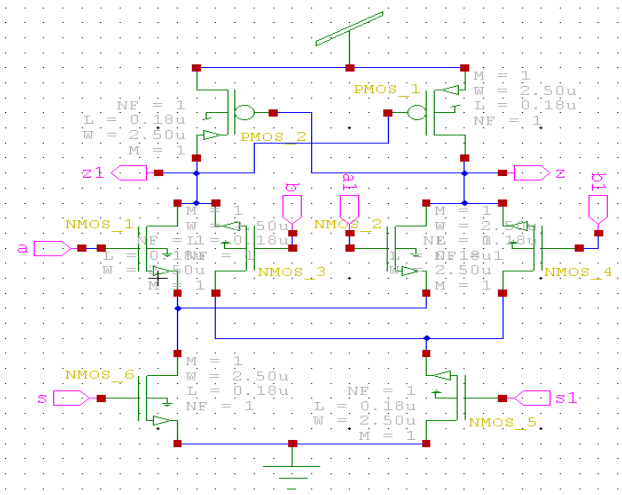

Figure 6 Schematic of DCVSL 2:1 MUX

The above figure is of DCVSL 2:1 mux, it consist s and s1 select line, a and b data inputs, a1 and b1 are inverted data inputs, and z and z1 are output and its complement respectively. When select line s is high then output will be a and when select line s is low then output will be b. larger power consumption(static and dynamic) and area in implementation are disadvantage of this circuit as the large number of MOS devices are used [6], [4].

G. MDCVSL 2:1 MUX

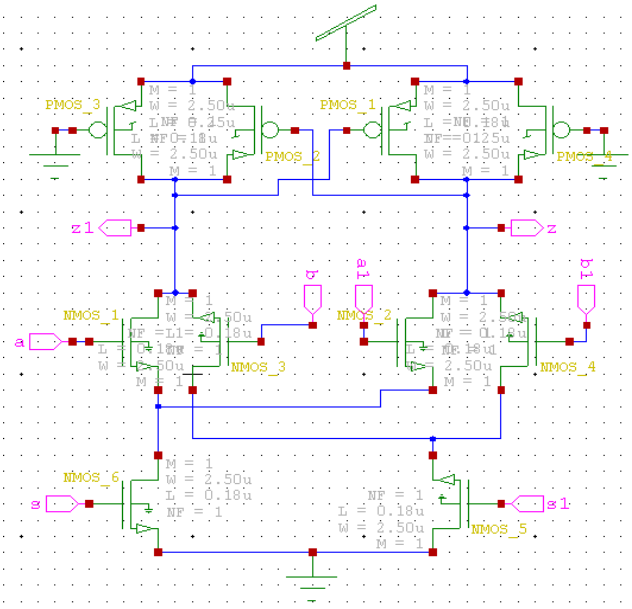

Figure 7 Schematic of MDCVSL 2:1 MUX

Figure 7 shows that MDCVSL 2:1 mux which consist s and s1 select line, a a
nd b data inputs, a1 and b1 are inverted data inputs and z and z1 are output and its
complement respectively.

III. SIMULATION ANALYSIS

A. Simulation environment

All the circuits have been simulated using TSMC18 180 nm technology on Tanner EDA tool.

B.Performance analysis

Figure 8 shows comparison of dynamic power dissipation and figure 9, 10 shows comparison of static power dissipation. Figure 11comparison of average static power dissipation, figure 12 and 13 shows comparison of Delay of all 2:1 MUX circuit for 1.8v vdd.2:1 MD MUX is used for designing 8 bit logical barrel right shifter. Figure 14 shows symbol of 2:1 MD MUX.

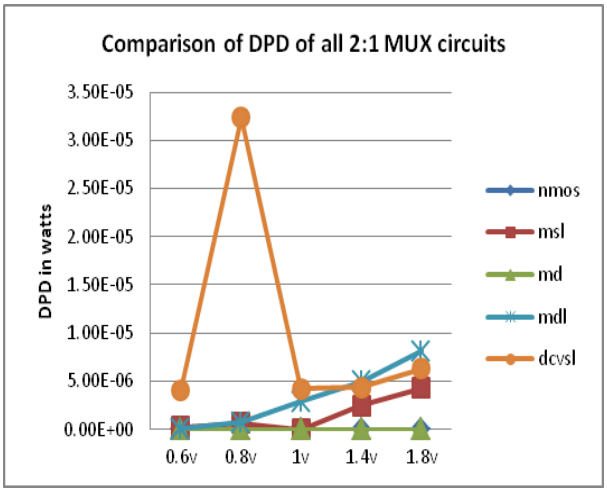

Figure 8 Comparison of DPD

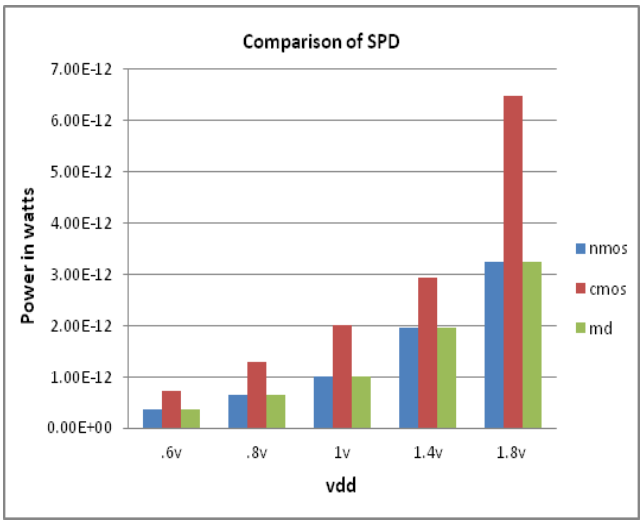

Figure 9 Comparison of static power dissipation in NMOS, CMOS and MD 2:1 MUX circuit

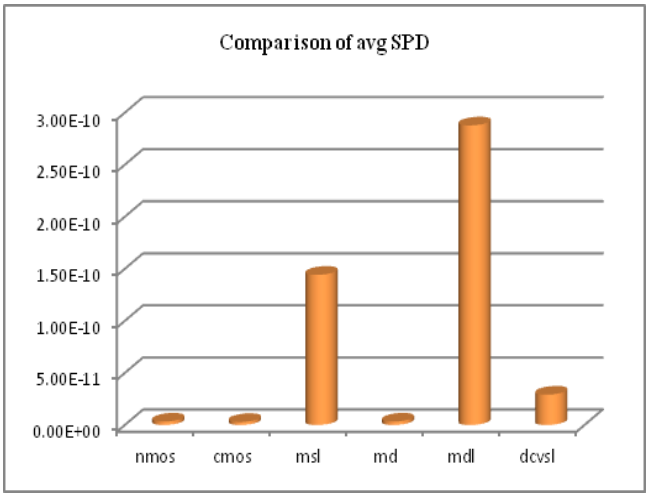

Figure 10 Comparison of average static power dissipation in NMOS, CMOS, MD, MSL, MDL and DCVSL 2:1 MUX circuit

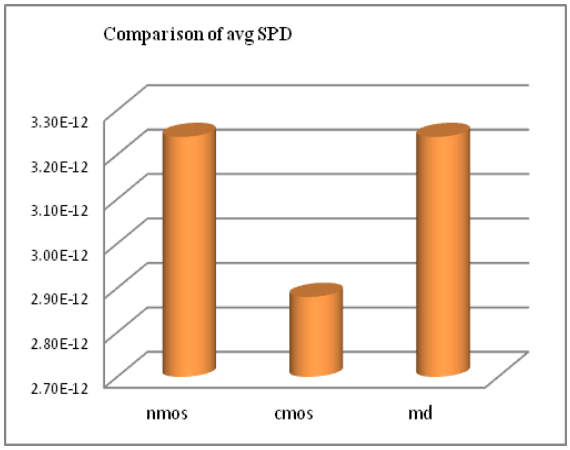

Figure 11 Comparison of average static power dissipation of NMOS, CMOS and MD 2:1 MUX circuit

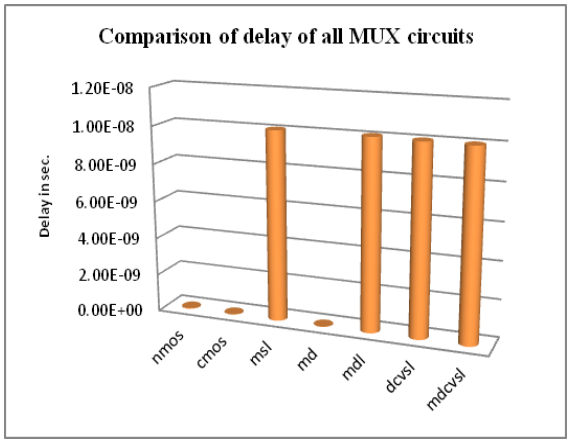

Figure 12 Comparison of Delay of all 2:1 MUX circuit for 1.8v vdd

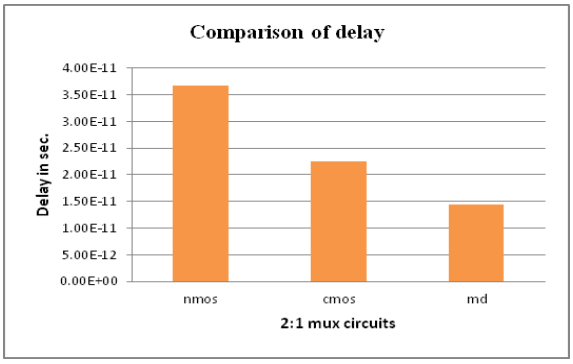

Figure 13 Comparison of Delay of NMOS, CMOS and MD 2:1 MUX circuit for 1.8v vdd

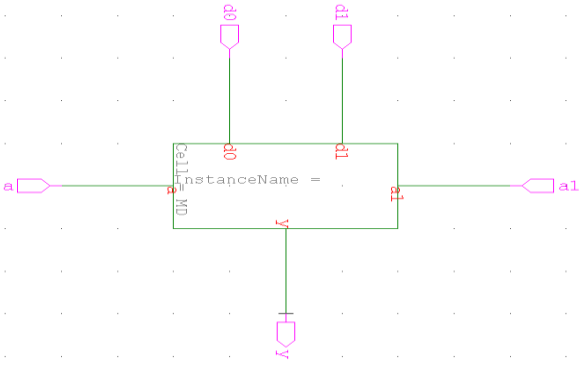

Figure 14 Symbol of MD 2:1 MUX

The symbol of MD 2:1 MUX is created because it will be required for designing of barrel shifters and/or rotators.

IV. IMPLEMENTATION OF 8-BIT LOGICAL RIGHT SHIFTER

An n-bit logarithmic barrel logical right shifter uses $\log_2(n)$ stages[6]. Each bit of the shift amount, $b_2b_1b_0$ controls a different stage of the shifter. Figure 15 shows the schematic diagram of 8-bit logical right shifter, which uses three stages with 4-bit, 2-bit and 1-bit shifts. Here we have shown output wave form only for opcode$b_2b_1b_0$ value 011,101 and 111 in figure 16, 17 and 18 respectably. Table 1 summarized output of 8 bit logical right shifter.

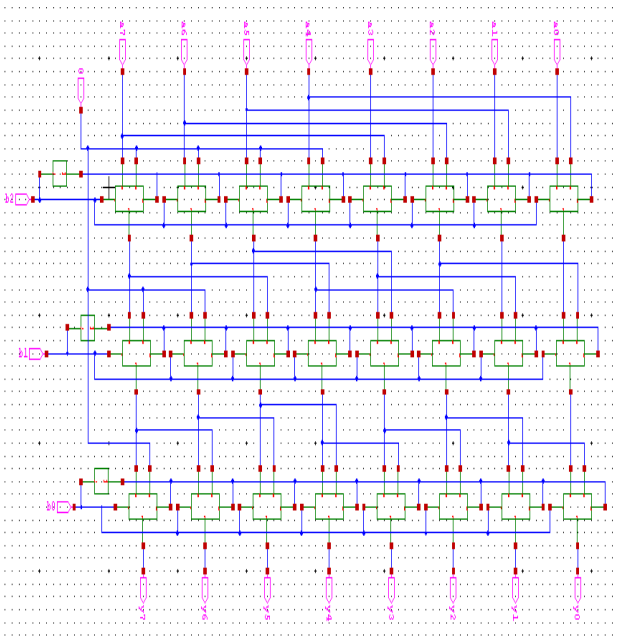

Figure 15 Schematic of 8 bit logical right shifter

Control bits			Output							
b2	b1	b0	y7	y6	y5	y4	y3	y2	y1	y0
0	0	0	0	1	0	1	1	1	0	1
0	0	1	0	0	1	0	1	1	1	0
0	1	0	0	0	0	1	0	1	1	1
0	1	1	0	0	0	0	1	0	1	1
1	0	0	0	0	0	0	0	1	0	1
1	0	1	0	0	0	0	0	0	1	0
1	1	0	0	0	0	0	0	0	0	1
1	1	1	0	0	0	0	0	0	0	0

Table 1 Output of 8 bit logical right shifter

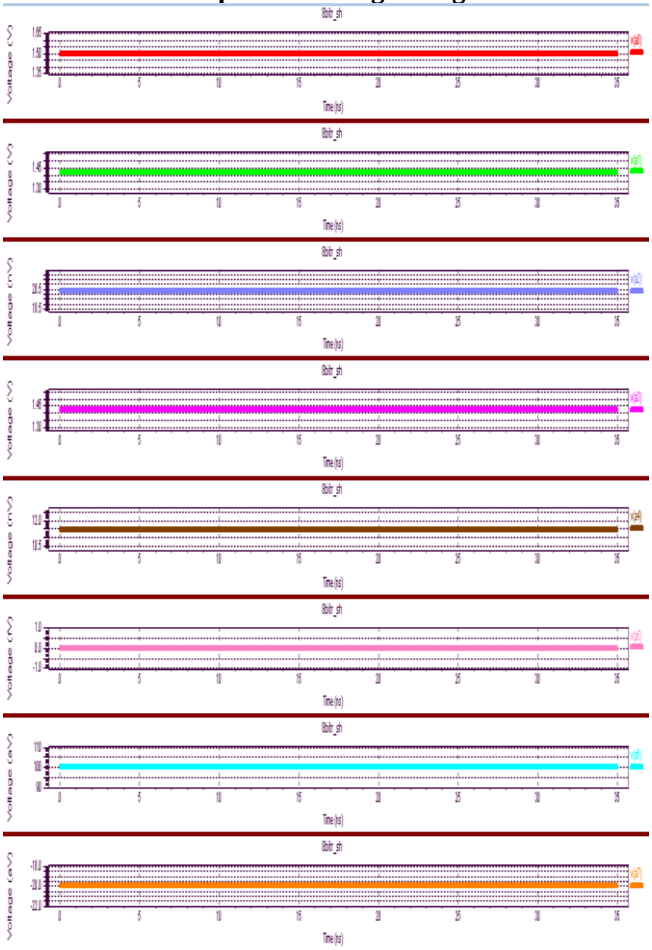

Figure 16 Output wave form of 8 bit logical right shifter with control input $b_2b_1b_0$=011

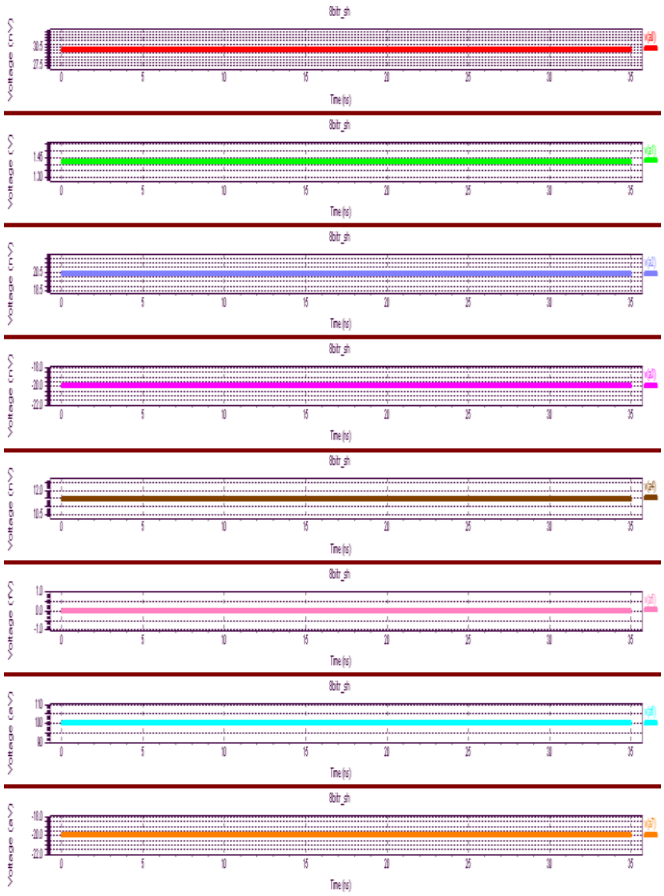

Figure 17 Output wave form of 8 bit logical right shifter with control input $b_2b_1b_0$=101

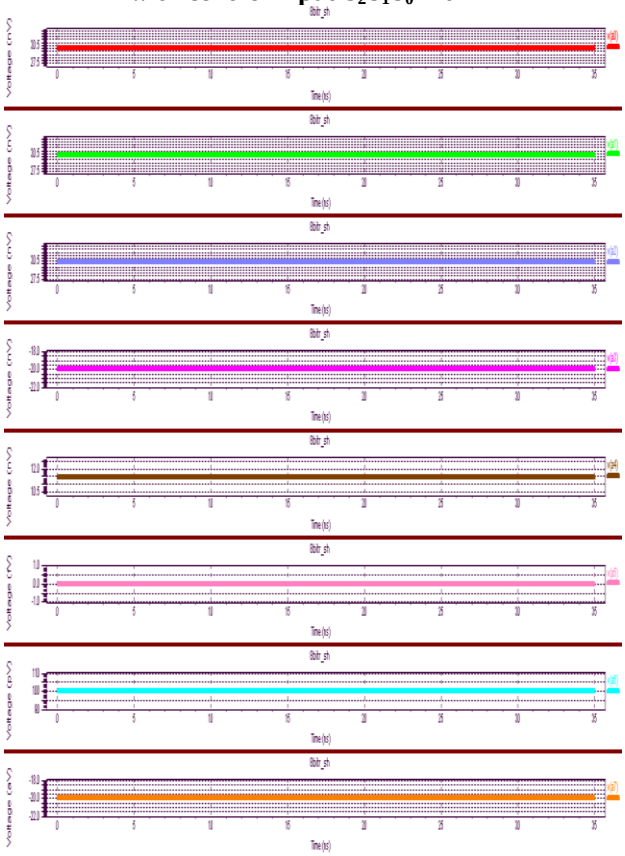

Figure 18 Output wave form of 8 bit logical right shifter with control input $b_2b_1b_0$=111

V. CONCLUSION

In every era of VLSI designing speed and power consumption is the main concern. This paper give the best 2:1 MUX for designing barrel shifter and/or rotators, which is basic building block of microprocessor CPU which can typically specify the direction of shift (left or right), the type of shift (circular, arithmetic, or logical), and amount of shift typically 1 to n-bits, but sometimes 1 to n bits [9]. Barrel shifter was used in processor till Pentium 3. The Athlon and K5 use barrel shifters [9].From all figures 8, 9, 10 ,11, 12 and 13 that is comparison of static & dynamic power dissipation and delay of all 2:1 MUX circuit for 1.8v and other lower vdd's, we can easily say that the MD 2:1 MUX is best in term of static, dynamic power dissipation and delay. So for designing barrel shifter and/or rotator we take MD 2:1 mux as basic building block.

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Mrs. Pratibha Gupta She is pursuing Master in Engineering in Digital Instrumentation under the supervision of Dr. Vaibhav Neema from Institute of Engineering and Technology, Devi Ahilya University, Indore (MP). She has having more than 6 years of teaching experience with various prestigious University/Institutes of India, development in area of Low Power CMOS Digital Circuit design is area of interest.