Comparative Study and Approach to Enhanced the Range and Power Requirement for Basic Memory Segment Analog Design

Naveen Kumar

Abstract—Now a day, analogy designing with dynamic range in high in demand. The minimum dissipation for power factor can be achieved only with improved range of system. Current mirror component is being researched from mainly of the years to achieve it's grated extend voltage level for power consumption. To comparative study of various current mirror with enhanced technology top design analogy circuit of most extend. This paper comes with achieve a logic for the communication system to achieve such a system which can be run over low power and low voltage supply. This paper also includes the theorem and result table by which it is easy to access the need of such a technology. CMOS S-RAM design is the basic element of memory design which can be achieved and comparative study is also given to minimize future works.

Index Terms—VMS , Low Voltage Low Power Current Mirror , Basic Current Mirror

I. INTRODUCTION

The current mirror is one of most common building blocks both in anlog and m ixed mode VLSI circuits. Current mirror is a core structure for almost all analog and mixed circuits[1-4] .It determines the performance of analog structures, which largely depends on their characteristics [5, 6]. The design philosophy of analog circuits is now moving towards implementing them in the form of standard building blocks, called analog signal processing (ASP) cell rather than the desecrate circuits. The ASP cells, which consists of several basic analog circuit structures and have voltage mode or current mode circuits are described as the circuits whose input and output signal are in form of currents and their complete circuit function are described through the currents signal rather than the voltages signals. The analog signal processing deal with converting signals from one analog domain to another. The basic building blocks generally use more than one transistor and perform only one function. The current mirror is a current controlled current source .The motivation behind a current mirror is to sense the current from a "reference current source "and duplicate this reference current source to other locations, or generate an output current equal to input current multiplied by desired current gain factor, current mirror is also called current copier.

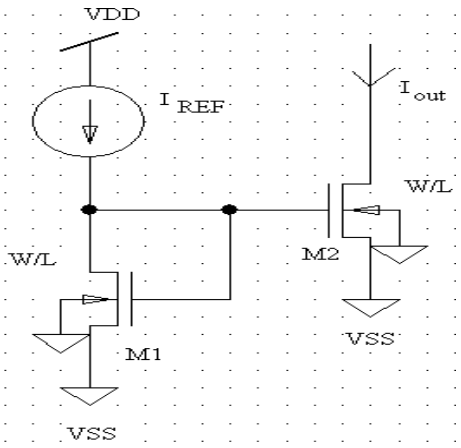

Figure 1: Basic Current Mirror [2]

II. APPLICATION OF CURRENT MIRROR

Current mirror is an essential structure in most of the analog circuit applications, where the gain of the MOS can be expressed as product of its effective transconductance (g_m) and the output impedance (r_o). Due to continuous downscaling of MOS technology the device size is shrinking fast to enable higher unity gain frequencies. However, it reduces the gain of the MOS due to lowering of transconductance (g_m) and increase in output conductance ($1/r_o$) [1 & 2]. The speed and accuracy of analog circuit structures are determined by its settling behavior. Fast settling demands high unity gain frequency and a single pole frequency response, whereas accurate settling requires high d.c. gain. In Figure 2 the block diagram of the application of current mirrors in analog circuits is shown. Current mirrors are essential blocks of analog circuits and mixed circuit like op amp, oscillator, and regulator. Some of important applications are discussed below:

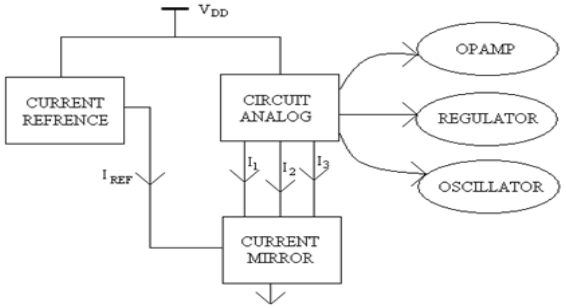

Figure 2: Application of Current Mirror

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Mr. Naveen Chhikara , Department Of Electronics and Communication Engineering Acme College Of Engineering, Palwal, Haryana ,India

III. HIGH SPEED AND LOW POWER

As the feature size of CMOS which processes reduces, which includes supply voltage has to be reduced for the reduction of power dissipation by per unit cell. Which results from device scaling. However, the circuit's performance goes down by degrading this current mirror . The reduction in supply voltage leads to degraded circuit performance in terms of available bandwidth and voltage swing Supply voltage reduction guarantee the reliability of devices as the lower electrical fields inside layers of a MOSFET produces minimum risk to the thinner oxides. By scaling down the threshold voltage of the MOSFETs reduces the performance loss (degraded bandwidth, low voltage swing etc.) somewhat but it has its own disadvantages i.e. the increase in the static power dissipation. On other hand, The non-zero current of MOSFETs in OFF state in digital circuits

- A Short-circuit power consumption due to the current flowing during the lapse of time when both NMOS and PMOS transistors are in the on state.

The dynamic power expenditure has been increasing quickly along with the progress in the processing technology of CMOS, which raises the ambient temperature and minimize the device performance and the circuit performance is less stable. By reducing power supply voltage is the most efficient method in reducing power dissipation of a chip. The dynamic power dissipation is given by

$$P = \alpha . C_L . V_{DD}^2 . f_{CLK} \quad (1)$$

where α is the probability of the logic gate output to change from 0 to1 and hence its value ranges from 0 to 1 and is called the switching activity. C_L is the load capacitance, and f_{CLK} is the clock frequency[15, 20].

Due to enhanced demands on the system performance, the clock frequency increases. By which Power dissipation can be reduced by reducing the switching activity and the output load capacitance. The previous can be reduced via proper circuit and system designs and the latter can be by reducing device dimensions or reduced by an advanced CMOS technology . But the reduction in power dissipation is most effective when V_{DD} is lowered. The static power consumption depends on the OFF state current (I_{off}) and equals

$$P_{static} = I_{off} V_{DD} \quad (2)$$

For conventional CMOS technologies with high threshold voltages, this contribution is too low. In case of analog circuits it is the main contributor for power dissipation as the devices are biased permanently in saturation modes.

During switching in CMOS, both PMOS and NMOS are simultaneously active for a short period of time and an instantaneous short-circuit current (I_{SC}) flows from the power supply directly to ground. So the power consumption due to I_{SC} is given by

$$P_{SC} = I_{SC} V_{DD} \quad (3)$$

This term can be neglected if the signals have short rise and fall times as compared to duration of the signal. Thus, the total power consumption is as given

$$P_{total} \approx N C_{eq} V^2 + I_{off} V_{DD} \quad (4)$$

overall performance of digital circuits is improved by scaling but the analog cells, because minimum size transistors cannot be used due to noise and offset requirements which benefit marginally .

In today's design techniques the aim is to achieve high speed and high integration on chip with a large range of operation . One of the factors, which affect such parameters, is power dissipation in the circuit. There are few major sources of power dissipation listed with [1, 7].

- It is given as Dynamic power consumption caused by it charging and discharging of (usually parasitic) capacitance;

On othe hand Static power consumption due to the biasing current in the analog circuits or to

Lowering power dissipation is also important for a high-performance system. Increase in power dissipation, increases the temperature which worsens the electro-migration reliability problems for the system . The low power and low voltage operation complicates the design of the circuits. To achieve better performance simple topologies requiring less number of MOSFETs can give better performance due to lower device and stray capacitances [1, 7 & 11].

For the low voltage high performance analog circuit design current mode design technique, which offer voltage independent high bandwidth analog circuit, is a good alternative. In current mode design the designer is more concerned with current levels for the operation of the circuits. The voltage levels at various nodes are immaterial [1].

All conventional analog circuits are voltage mode circuits (VMCs) where the circuit performance is determined in terms of voltage levels at various nodes including the input and the output nodes example amplifiers . But all these circuits includes from the following disadvantages

- Usually it is not easy to change the output voltage instantly when there is a sudden change in the input voltage due to stray and other circuit capacitances and stray .
- Due to finite unity gain Bandwidth of the op amp based circuits is usually low because of finite .
- Basically slew rate is dependent on the time constants associated with the circuit.
- Circuits can't contain have high voltage swings.
- The main demand is require higher supply voltages for better SNR (signal to noise ratio).

Therefore, voltage mode circuits (VMCs) are not suitable for use in high frequency applications. In current mode circuits (CMCs) the complete circuit response is determined by the currents and the input/output signals are primarily currents. The voltage levels are irrelevant in determining the circuit performance. Resultant nodes inside CMCs are low impedance nodes, where the resultant voltage swings are also small. The low impedance converts them into low time constant circuits and the bandwidth is quite high. By which slew rate is also high if the rate of output changing is high. The CMCs have simple architecture and their operations do not depend on the supply voltages.

The operation is not directly depend on the power supply. The analog circuits should have output voltage swing capability for high SNR (signal to noise ratio) and rail-to-rail input, which can be received using the CMCs. CMC structure is current conveyor (CC) [11].

- Very high output impedance (high R_{out} and low C_{out}). As a result the output current is independent of output voltages.
- Low input resistance (R_{in}).
- Low output and input compliance voltages.

I. Low Voltage Current Mirror Designing Technology

At low voltage, the main constraints faced are the device noise level and the threshold voltage (V_T). Reduction in V_T is dependent on the technology of the device . on other hand Higher V_T gives better noise immunity and the lower V_T reduces the noise margin to result in poor SNR. Hence, for present day CMOS technology, reduction in V_T is limited to the noise floor level, below which further reduction will introduce an amount of noise sufficient to result in very complex circuits. The restriction on further reduction in V_T paves the way to have simpler, smarter and efficient circuits [2]. Many new design techniques for low voltage analog circuits are being used and available, MOSFETs operating in the sub-threshold region, at instants bulk driven transistors (current mirror), self-cascode structures, floating gate approach and the level shifter techniques. Use of low voltage high performing building

Low Voltage Design Techniques	Available Bandwidth	Supply Voltage Requirements	Power Consumption	Technology Requirements
Sub-threshold	Low	$\approx 2V_T$	Low	Standard
Bulk-Driven	Low	$\approx 2V_T$	High	Special
Self-Cascode	Medium	$> 2V_T$	High	Standard
Floating-gate	Medium	$< 2V_T$	Medium	Special
Level shifter	High	$< 2V_T$	Medium	Standard
Use of low voltage cell	High	$< 2V_T$	Medium	Standard

Table 1: Characteristics for the technology used

blocks in low voltage analog circuits is another promising approach and yields a modular design concept in analog circuits as well.

II. Design Of A Low Power Low Voltage Current Mirror

One of the most fundamental building blocks of analog integrated circuit is the Low Voltage current mirror .Current mirror is enable a single current source to supply mirrors are output impedance and voltage headroom. The output impedance determines the variation of the mirrored current when the applied voltage varies. Higher output impedance implies less current variation with applied voltage and hence a more stable current source Voltage headroom specifies how much voltage drop across the current mirror is required ton operate the current mirror reliably. This is especially important for low voltage circuit design.

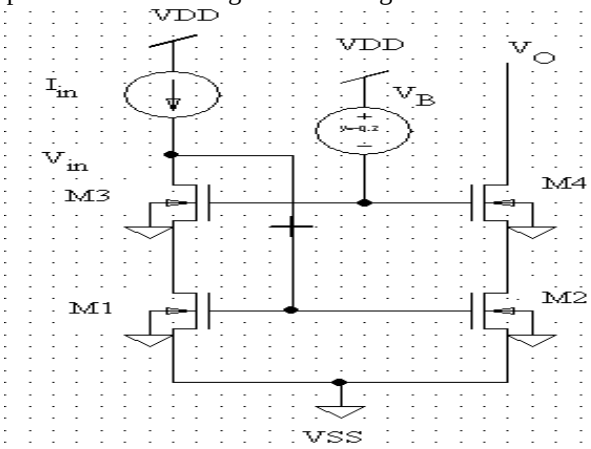

Figure 3: Low Voltage Current Mirror

The low voltage cascode current mirror shown in figure 3 .We assumes that the current mirror transistors M1 and M2 have identical, aspect ratio. $A_M = \frac{W_1}{L_1} = \frac{W_2}{L_2}$ Where W_1 and W_2 are the transistor channel width and L_1 and L_2 are the transistor length. Similarly the transistor M3 and M4 are assumed the same aspect ratio $A_C = \frac{W_3}{L_3} = \frac{W_4}{L_4}$ .The aspect ratio A_M may be different from the aspect ratio A_C . In the analysis of the dynamic range the same aspect ratio of A_M and A_C and we use standard Schman –Hodges transistor model for the transistor in the saturation region and we neglected the bulk effect and assume that all the NMOS transistors have the identical.

Low voltage current mirror input current I_{in} we find the gate-source voltages and drain -source voltages

$$V_{GS1} = V_{tn} + \sqrt{\frac{2I_{in}}{KA_M}} \qquad (5)$$

G to S voltage of transistor multiplier 3

$$V_{GS3} = V_{tn} + \sqrt{\frac{2I_{in}}{KA_C}} \qquad (6)$$

D to S voltage of transistor multiplier 1 is

$$V_{DS1} = V_{BC} - V_{tn} - \sqrt{\frac{2I_{in}}{KA_C}} \qquad (7)$$

Drain to source voltage of transistor multiplier 3 is

$$V_{DS3} = V_{GS1} - V_{DS1}$$

$$= 2V_{tn} - V_{BC} + \sqrt{\frac{2I_{in}}{K}}\frac{1}{\sqrt{A_M}} + \frac{1}{\sqrt{A_C}} \qquad (8)$$

Where, V_{tn} is the transistor threshold voltage, V_{BC} is the bias or gate voltage of transistor M3 and M4 and K is the transconductance parameter. Requiring $V_{GS} - V_{tn} \leq V_{DS}$ for both M1 and M3 result in:

$$\sqrt{\frac{2I_{in}}{K}}\left(\frac{1}{\sqrt{A_M}} + \frac{1}{\sqrt{A_C}}\right) + V_{tn} \leq V_B \qquad (9)$$

Biasing voltage:

$$V_B \leq 2V_{tn} + \sqrt{\frac{2I_{in}}{K A_M}} \qquad (10)$$

In figure 3 low voltage current mirror, biasing voltage V_B is fixed when I_{in} increases, voltage of the gate –source voltage V_{GS3} of transistor M3

and V_{in} will increase, and voltage level at the drain terminal of M1 decreases. There by M1 enter the triode region which determine upper limit of I_{in}.Below equation (11) ensure the saturation of M1 and determines the maximum value of I_{in} for given value of the cascode bias voltage V_B we

$$I_{in,max} = \frac{K}{2} A_M (V_B - V_{tn})^2 \left(\frac{\sqrt{A_C/A_M}}{1+\sqrt{A_C/A_M}}\right)^2 \quad (11)$$

Equations (9) ensure the saturation of M3 and determine the minimum value ofI_{in}. We find

$$I_{in,min} = \frac{K}{2} (V_B - 2V_{tn})^2 A_M \quad (12)$$

Maximum value of the bias voltage even at the minimum value of input current equation (10) determine, and equation (10) determined the value of A_C and A_M which determined the saturation of M1 and the maximum value of input current . To ensure Saturation operation of transistors M1 and M3 the input current range determined by

$$\frac{K}{2} A_M (V_B - 2V_{tn})^2 \leq I_{in} \leq \frac{K}{2} A_M (V_B - V_{tn})^2 \left(\frac{\sqrt{A_C/A_M}}{1+\sqrt{A_C/A_M}}\right)^2 \quad (13)$$

In a practical design procedure equation(10) can be used to determine the maximum value of the bias voltage which will ensure saturation of M3 even at the minimum value of input current, and equation (11) can then be used to determine values of A_C and A_M which will ensure saturation of M1, even at the maximum value of input current.

In the important special case of $I_{in,minimu} = 0$ we find from (12) $V_B \leq 2V_{tn}$. From equation (11) we then find the following design constraint on A_C and A_M

$$A_M \left(\frac{\sqrt{A_C/A_M}}{1+\sqrt{A_C/A_M}}\right)^2 \geq \frac{2I_{in,max}}{V_T^2 K} \quad (14)$$

Assuming as a typical case W1 = W3 and L1 = L3 i.e. identical aspect ratios for the mirror transistors and the cascode transistors, we find

$$A_M = A_C = \frac{W}{L} \geq \frac{2I_{in,max}}{V_T^2 K} \quad (15)$$

For such case the effective gate-source voltage of the mirror transistors M1 and M2 is

$$V_{GS1} - V_{tn} = \sqrt{\frac{2I_{in}}{K A_M}} = \frac{V_{tn}}{2}\sqrt{\frac{I_{in}}{I_{in,max}}} \quad (16)$$

So , case the minimum output voltage of the current mirror is and is independent of the input current.

$$V_{out,min} = V_B - V_{tn} = V_{tn} \quad (17)$$

In a high precision current mirror one would like to have as large an effective gate-source voltage as possible in order to minimize the effect of threshold voltage mismatch. It is evident that the effective gate-source voltage $V_{GS1} - V_{tn}$ can be increased above the value given by equation(17) if A_C is increased, i.e. a larger aspect ratio is used for the cascade transistor. In this case the cascode transistor requires a smaller effective gate-source voltage for a given value of input current, leaving more headroom for the drain-source voltage of the mirror transistor. Introducing $N = A_C/A_M$ we find

$$A_M = \left(\frac{1+N}{N}\right)^2 \frac{2I_{in,max}}{(V_B - V_{tn})^2 K} \quad (18)$$

And

$$V_{GS1} - V_{tn} = \frac{N}{1+N}(V_B - V_{tn})\sqrt{\frac{I_{in}}{I_{in,max}}} \quad (19)$$

Very low power signal output resistance of the mirror is given by

$$r_{out} = \frac{1}{g_{ds2}}\left(1 + \frac{g_{dm4}}{g_{ds4}}\right) \approx \frac{1}{g_{ds2}}\frac{g_{m4}}{g_{ds4}} \quad (20)$$

As g_{m4}/g_d is inversely proportional to the square root of , we find that the output resistance is inversely proportional to N. Thus, the higher effective gate-source voltage of the mirror transistors is achieved at the expense of a reduced output resistance.

III. DYNAMIC RANGE CALCULATION OF LOW VOLTAGE CURRENT MIRROR

Aspect ratio of transistors used in low voltage current mirror is given in table 2

MOSFETs	Type	Width	Length
M1,M2,M3,M4	NMOS	20µm	0.5µm
M5	PMOS	10µm	0.3µm

Table 2: Aspect Ratio in LVCM current mirror

Parameter	Unit
Supply voltage	1.0 volt
V_{bias} (Voltage bias)	-0.2 volt
Threshold voltage V_{tn} (NMOS)	0.44 Volt
Transconductance	156.8µA

Table 3: Parameters used in Low Voltage Current Mirror (LVCM)

IV. CONCLUSION

CMOS technology had already dominated the whole electronic industry. Demands on portable electronic devices, leads VLSI design to reducing power and increasing speed of electronic devices. With the advent of the portable electronic and mobile communication systems low-voltage and low-power mixed mode circuit design has gained importance. For the operation of such systems like hearing aids, implantable cardiac pacemakers, cell-phones and hand held multimedia terminals etc. battery is the main source of power. They require low power dissipation so as to have reasonable battery life and weight. Designing High Performance analog circuits is becoming increasingly challenging with the persistent trend toward reduced supply voltages. The main bottleneck in analog circuit design is the current mirror. The current mirror is one of most common building blocks both in analog and mixed mode VLSI circuits. The applications of battery powered analog and mixed mode electronic devices require designing current mirror circuits to operate at low voltage levels.

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AUTHOR PROFILE

Mr. Naveen kumar is a student of final year Master of Technology at applied college of Management and Engineering . His area of interest is memory application and low voltage device .