Parallel Power Flow AC/DC Converter with High Input Power Factor and Tight Output Voltage Regulation for Universal Voltage Application

Dhudem Santhosh, Jisha Bhubesh, Khaja Rafiulla

Abstract--In this paper, a new parallel-connected single phase power factor correction (PFC) topology using flyback converter in parallel with forward converter is proposed to improve the input power factor with simultaneously output voltage regulation taking consideration of current harmonic norms. Paralleling of converter modules is a well-known technique that is often used in medium-power applications to achieve the desired output power by using smaller size of high frequency transformers and inductors. The proposed approach offers cost effective, compact and efficient AC-DC converter by the use of parallel power processing. Forward converter primarily regulates output voltage with fast dynamic response and it acts as master which processes 60% of the power. Flyback converter with AC/DC PFC stage regulates input current shaping and PFC, and processes the remaining 40% of the power as a slave. This paper presents a design example and circuit analysis for 300 W power supply. A parallel-connected interleaved structure offers smaller passive components, less loss even in continuous conduction inductor current mode, and reduced volt-ampere rating of DC/DC stage converter. MATLAB/SIMULINK is used for implementation and simulation results show the performance improvement.

Index Terms-- Circuit analysis, PFC, Power Conversion.

I. INTRODUCTION

A number of power factor correction circuits have been developed recently [1]-[5]. Normally a boost converter is employed for PFC with DC/DC stage to improve performance or a flyback converter is used to reduce the cost. Although both boost converter and flyback converter are capable for PFC applications [6], [7], the main difficulty in two stage scheme employing a PFC boost and a DC/DC converter is the high cost and lower efficiency. However, single-stage method using the simplest flyback converter is not able to tightly regulate the output voltage.

Paralleling of converter power modules [8-9] is a well-known technique that is often used in high-power applications to achieve the desired output power with smaller size power transformers and inductors [1o]. Since magnetics are critical components in power converters because generally they are the size-limiting factors in achieving high-density and/or low profile power supplies, the design of magnetics becomes even more challenging for high-power applications that call for high power-density and low-profile packaging. Instead of designing large-size centralized magnetics that handle the entire power, low-power distributed high density low-profile magnetics can be utilized to handle the high processing power, while only partial load power flow through each individual magnetics [I0, 11].

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In addition to physically distributing the magnetics and their power losses and thermal stresses, paralleling also distributes power losses and thermal stresses of the semiconductors due to a smaller power processed through the individual paralleled power stages. As a result, paralleling is a popular approach to eliminating "hot spots" in power supplies. In addition, the switching frequencies of paralleled, lower power power stages may be higher than the switching frequencies of the corresponding single, high-power processing stages because lower-power, faster semiconductor switches can be used in implementing the paralleled power stages. Consequently, paralleling offers an opportunity to reduce the size of the magnetic components and to achieve a low-profile design for high power applications.

Without increasing the number of power stages and control circuit components, the transformer magnetics can be distributed by direct transformer paralleling. Not only that transformer paralleling distributes the processed power in each magnetics components, but also their power losses and thermal stresses are distributed at the same time. However, current sharing among the paralleled transformers needs to be maintained to ensure power balance.

In its basic form, the interleaving technique can be viewed as a variation of the paralleling technique, where the switching instants are phase-shifted within a switching period [12]. By introducing an equal phase shift between the paralleled power stages, the total inductor current ripple of the power stage seen by the output filter capacitor is lowered due to the ripple cancellation effect [12].

This chapter discusses the paralleling techniques to achieve high-density, low-profile designs for relative high `power` applications. It analyzes and compares the current sharing in various implementations of transformer paralleling. The goal of the proposed PFC scheme is to reduce the passive component size, to employ lower rated semiconductor, and to improve total efficiency. Simulation results show that the proposed topology is capable of offering good power factor correction and fast dynamic response.

II. PFC CELLS

A. Two Stage PFC Approach

A two-stage scheme shown in Fig. 1 is mainly employed for the switching power supplies since the boost stage can offer good input power factor with low total harmonic distortion (THD) and regulate the dc-link voltage and the DC/DC stage is able to obtain fast output regulation without low frequency ripple due to the regulated dc-link voltage [13].

These two power conversion stages are controlled separately. However, two-stage scheme suffers from higher cost, complicated control, low-power density, and lower efficiency.

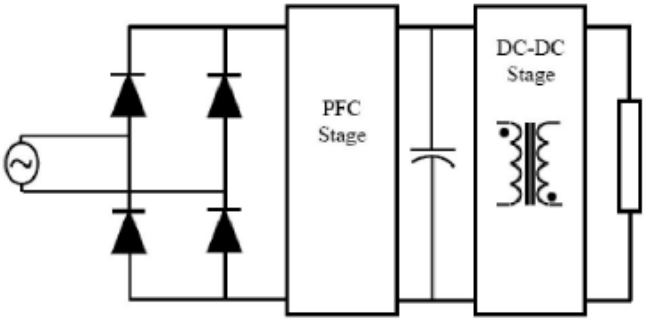

Fig. 1. Two-stage PFC.

B. Single Stage Approach

For low power applications, where cost is a dominant issue, a single-stage scheme using the flyback converter is more attractive than a two-stage scheme [14]. A single-stage scheme Fig.2, cannot provide good performance in terms of ride-through or hold-up time since it mainly regulates input current with rectified voltage input and also output voltage is normally too small to provide hold-up time. Therefore, most of flyback converters need a large electrolytic capacitor at the output terminal to reduce the second harmonic ripple. But its transient response is still poor. The limitation of the flyback PFC is the output power level and the high breakdown voltage is required for the switch. When the output power increases, both voltage and current stress increase. Due to the high ripple currents the flyback is less efficient than other designs. That is why the two-stage scheme is more attractive for higher power rating.

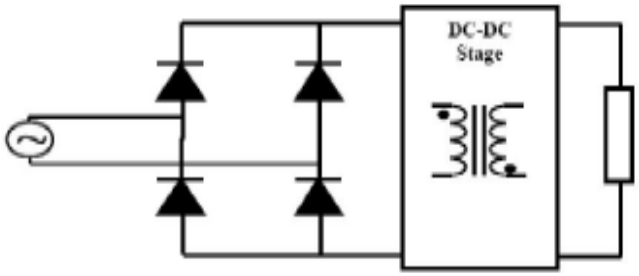

Fig. 2. Single- stage PFC.

C. Parallel PFC Approach

At higher power levels, since it may be beneficial to parallel two or more DC/DC converters rather than using a single higher power unit, a parallel-connected scheme is proposed as shown in Fig. 3. This approach can offer fast output voltage regulation and high efficiency. The forward converter with DC/DC stage can offer good output voltage regulation due to the pretty dc input voltage and the flyback converter with AC/DC PFC stage fulfills input current regulation to obtain highly efficient power factor. The advantages of the proposed approach are as follows.

1) This scheme offers good input power factor and output regulation.
2) Input inductor and dc-link capacitor can be smaller.
3) The power rating of flyback converter-I is lower than that of two-stage structure due to low dc-link voltage and lower current rating.
4) The diode reverse recovery losses can be minimized due to the tailed operating mode in diode current.

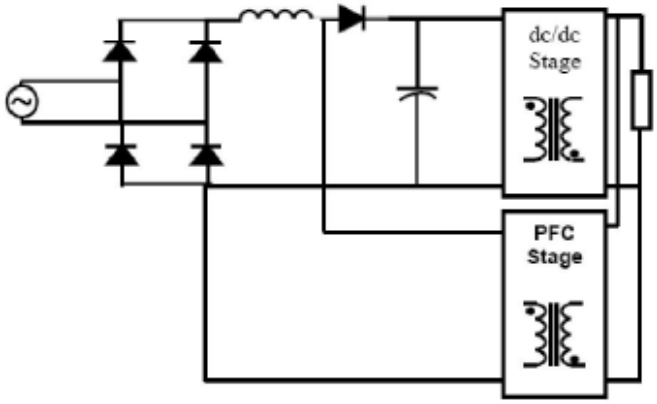

Fig. 3. Proposed parallel - connected single- stage PFC scheme.

III. PROPOSED PARALLEL PFC SCHEME

Fig. 4 shows the proposed parallel-connected PFC scheme which employs a diode rectifier, dc-link capacitor, forward converter and flyback converter. The function of a forward converter with an electrolytic capacitor is to support output voltage regulation.

A flyback converter fulfills the function of power factor correction by making input current sinusoidal and regulating dc-link voltage. The operation of the flyback converter is given in this paragraph considering that the forward converter operates ideally. The PFC Cell (forward converter) operates with continuous conduction mode in both an input inductor and a flyback transformer. The dc-link voltage in this scheme can be lower than other schemes as

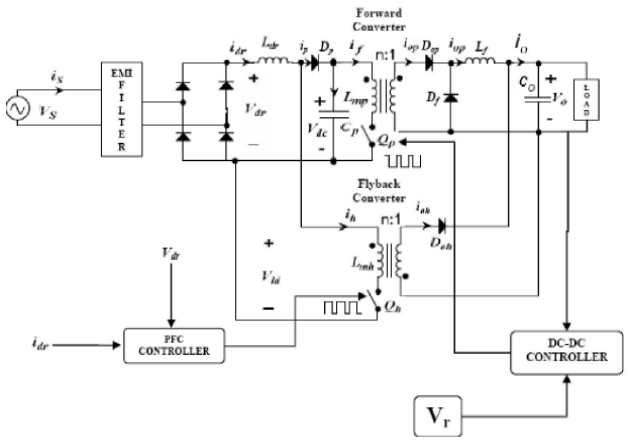

Fig. 4. Proposed parallel PFC converter.

$$Vdc = \sqrt{2}Vs \qquad (1)$$

The transfer function of the flyback converter is expressed by defining a conversion ratio as the ratio of the dc output voltage to the input voltage

$$M = \frac{Vo}{Vdr} = \frac{D}{D(1-n)} \qquad (2)$$

Where, D is the duty ratio of the switch Qh, n (=Np/N,), is defined as the ratio of Np to Ns, and Np and N, denote the number of turns of primary and secondary side, respectively.

The operational waveforms are shown in Fig. 6. To analyze the circuit parameters, basic equations for voltages and currents are given by

$$i_{dr} = i_p + i_h, \quad (3)$$

$$V_{Ldr} = L_{dr}\frac{di_r}{dt}, \quad (4)$$

$$V_{hi} = V_{dr} - V_{Ldr}, \quad (5)$$

$$V_{hl} = V_{hi} - V_{Qh}. \quad (6)$$

Where idr, ip, and ih are the rectified, DC/DC Cell, and PFC Cell input currents on dc side. VLdr, Vhf, Vhf, Vdr ,Vhl, VQh, and VO and are the input inductor, flyback converter input, rectified input, transformer primary winding, switch, and output voltages, respectively. Since the two input currents, ip and ih, are interleaved, input current, idr, ripple can be significantly reduced. The operational sequences are as follows.

to-t1: As shown in Fig. 5(a) The current of flyback transformer does not flow simultaneously in both windings. When the switch Qh is turned ON at to, VQh becomes zero and diode Doh is turned OFF with a reverse bias. The voltage across the diode Doh equals to Vo + Vh,/n. Energy, LmhI2, is charged in the magnetic field in the primary winding of the flyback transformer. Primary current, ih, ramps up from the remaining magnetizing current and reaches Idr with the slope, (Vhi/Lmh), ip decreases with a slow current tail, and slowly decreases until i'p reaches zero. At the same time the forward converter switch Q9p is OFF because, as the switch Qh iS ONthe potential at he junction of diode D and input inductor Ld. i.e. $V_{Ldr} > V_{hi}$, the diode DP is reverse biased. The diode DOP is also reverse biased due to the polarity of the forward transformer and a negative voltage of -nVo. The voltage across the output inductor is VL= - Vo and the inductor current iLf decreases and iLf along with ioh, circulates through diode Df and supplied to load.

tl-t2: The primary current of flyback converter increases by
Vdi/(Lmh + Ldr). The voltage across switch Q9 decreases from 2Vdr to Vdr. The input inductor current ramps up to till switch Qh iS OFF.

t2-t3: As shown if Fig. 5(b), when the switch Qh is turned OFF, Doh is turned ON with forward bias. The current in the primary winding ceases to flow. The stored energy is transferred to the secondary winding. At this time, the switch voltage, VQh, becomes Vhi+nVO, i'p becomes idr and decreases depending on input voltage, and the secondary current decreases with the slope (n^2Vo/Lmh). When the switch Qp is ON, the diode Dp is forward biassed because the potential at junction between the diode and inductor is VLdr<Vhi+±nVo. The primary current of forward transformer ramps up and the energy stored in the primary winding is instantaneously transferred to secondary, because of the same polarity of the forward transformer. The diode
Dop is forward biassed and diode Df is reversed biassed. The output inductor current iLf increases along with ioh which is delivered to load.

The current slope through the magnetizing inductor when the switch Qh is turned off is given as

$$\Delta i_{mh} = -\frac{nV_o}{L_{mh}}T_{off} \quad (7)$$

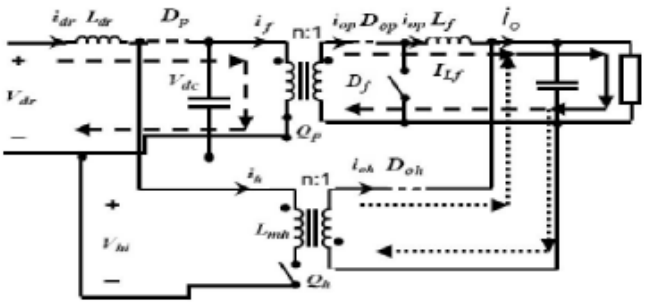

Fig. 5(a). Forward converter switch Qp is OFF and flyback converter switch Qh iS ON.

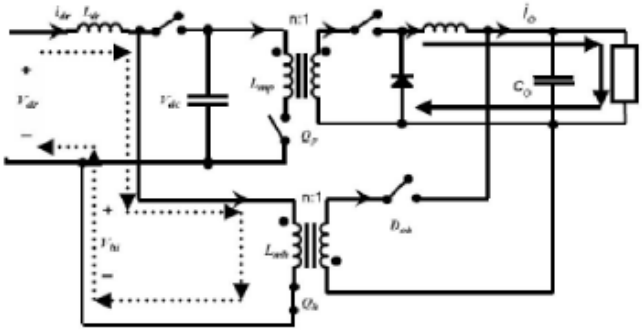

Fig. 5(b). Forward converter switch Qp is ON and flyback converter switch Qh iS OFF.

Where, Toff is the turn-off time. Similarly, the change of the flyback converter input current ip through a diode is

$$\Delta i_p = -\frac{Vdc - V_{dr}}{L_{dr}}T_{off} \quad (8)$$

Based on two slopes of imh and ip, the tailed diode current mode in which the diode current has current tail is defined as shown Fig. 7 when the slope of imh is greater than that of ip

$$v_{dr} > \frac{L_{mh}V_{dc} - nV_oL_{dr}}{L_{mh}} \quad (9)$$

In continuous conduction input inductor current mode, when the MOSFET is switched on, the diode DP is forced into reverse recovery at a high rate of change in the diode current ip. In this tailed mode operation, however, the diode current slowly decreases so that the reverse recovery effect can be minimized.
To analyze the flyback converter operation, an open loop duty ratio is obtained from (2) as

$$D_{open,h} = \frac{nV_o}{v_{dr} + nV_o} \quad (10)$$