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Research and Implementation of High-Speed Data Streams Symbol Synchronization Algorithm Using Training Sequence in IMDD-OOFDM System

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Abstract. We propose a symbol synchronization algorithm for high-speed data streams in IMDD-OOFDM system using a training sequence. Sampling point phase offset approximately sustains within ±π/32 and symbol synchronization deviation stabilizes within ±0.5 sampling point in a real-time system of 1.5Gsa/s.

Keyword. Symbol synchronization algorithm, high-speed data streams, IMDD-OOFDM, training sequence

1. Introduction

With the increasing bandwidth of optical communication networks, the increasingly supported sampling rate of the physical layer and more application of high-speed data streams systems will be needed. At present, the intensity-modulation and direct-detection optical orthogonal frequency division multiplexing (IMDD-OOFDM) systems based on FPGA can be run the bit rate of 20.37 Gb/s [1]. The increasing of sampling rate poses a challenge to the symbol synchronization of system.

Symbol synchronization is the first step of prime subsequent receiving processes in IMDD-OOFDM systems. In the system, OFDM symbols are continuously transmitted by using a fixed-length frame. Therefore, the purpose of symbol synchronization is to catch the starting position of the frame's header.

In fact, Sampling Clock Offset (SCO) inevitably affects the accuracy of symbol synchronization in high-speed data streams. SCO occurs due to the frequency offset between the transmitter and the receiver [2]. Therefore, SCO leads to the sampling

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point phase offset (SPPO) of the receiver, which accumulates into the integer sampling points deviation of the receiver over time.

In order to solve the problem of sampling point deviation caused by SCO, symbol synchronization of the low-speed data streams of IMDD-OOFDM system is performed on each frame and the length of each frame is set to be relatively short. In the aboved method, SPPO does not need to be considered, because SCO don't lead to integer sampling points deviation in the low-speed data streams system.

However, the frame length and sampling rate of high-speed data stream are several or even ten times higher than those of low-speed data stream, so that SCO lead to integer sampling points deviation in the high-speed data streams system. Moreover, SPPO becomes a non-negligible factor for symbol synchronization compared with low-speed data streams system. Therefore, symbol synchronization algorithm of low-speed data stream is not suitable for high-speed data stream. In summary, it is significant and meaningful to research symbol synchronization algorithm for high-speed data streams in the IMDD-OOFDM system.

In this paper, we propose a new symbol synchronization algorithm for high-speed data streams using a training sequence. The effect of SCO was eliminated by combining the proposed symbol synchronization algorithm and Frequency Offset Adjustment (FOA) in [3]. Moreover, based on FPGA, we implement the 1.5Gsa/s real-time IMDD-OOFDM system over 120km standard single mode fiber. The experimental result verifies that SPPO approximately keeps range from $-\pi/32$ to $+\pi/32$ and the deviation of symbol synchronization stabilizes within ±0.5 sampling point. These results show that each OFDM symbol is precisely located without any integer sampling point deviation.

2. System setup and the principle of the symbol synchronization algorithm

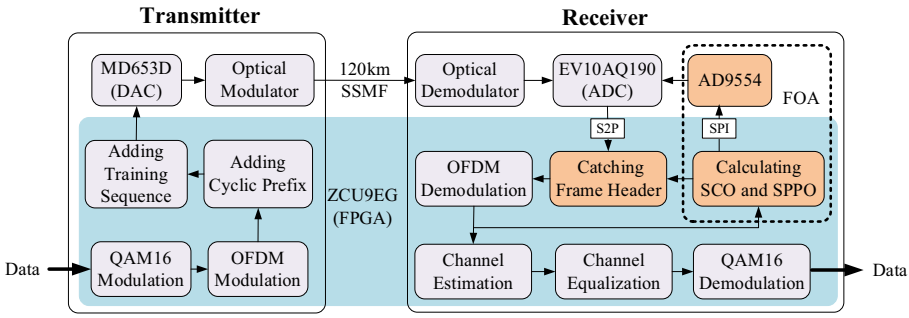

Figure 1. Block diagram of the IMDD-OOFDM system

Figure 1 shows the block diagram of the IMDD-OOFDM system over 120km standard single mode fiber to realize symbol synchronization algorithm for high-speed data streams. The part of the blue block diagram is realized in FPGA, which includes the DSP processing of the transmitter and the receiver. DAC and ADC are set to 1.5Gsa/s real-time sampling. FPGA receives serial sampling data from ADC and turns them into 40-point parallel sampling data. The length of the frame has 256 OFDM symbols. The frame is composed of 253 OFDM symbols and a frame header which is a training

sequence. Training sequence uses 3 OFDM symbols length which has 120-point data to implement symbol synchronization. OFDM modulation and demodulation are implemented with 32-point Inverse Fast Fourier Transform (IFFT) and 32-point Fast Fourier Transform (FFT). Cyclic Prefix (CP) is set to 8-point data. The length of the OFDM symbol has 40-point data after adding cyclic prefix.

Symbol Synchronization is implemented by three orange block diagrams in Figure 1. AD9554 is the clock chip that can compensate for the SCO of ADC in real-time. According to the principle of FOA in [3], the data on subcarriers No. 1, 5, and 9 of 256 OFDM symbols in each frame are used to calculate SCO and SPPO. The value of SCO is sent to AD9554 through the SPI interface. Finally, AD9554 uses this value to compensate for the SCO of ADC. It is worth noting that SPPO can reflect symbol synchronization performance. An OFDM symbol has a phase of 2π. Because the system uses 32-point IFFT and FFT, each point of the OFDM symbol represents a phase of $2\pi/32$. Therefore, if the absolute value of SPPO is greater than $\pi/16$, the symbol synchronization deviation is greater than 1 sampling point and is judged to have failed. In our proposed symbol synchronization algorithm, FOA is used to control the value of SPPO between $-\pi/32$ and $\pi/32$ nearby, which means that our symbol synchronization deviation is controlled within ± 0.5 sampling point.

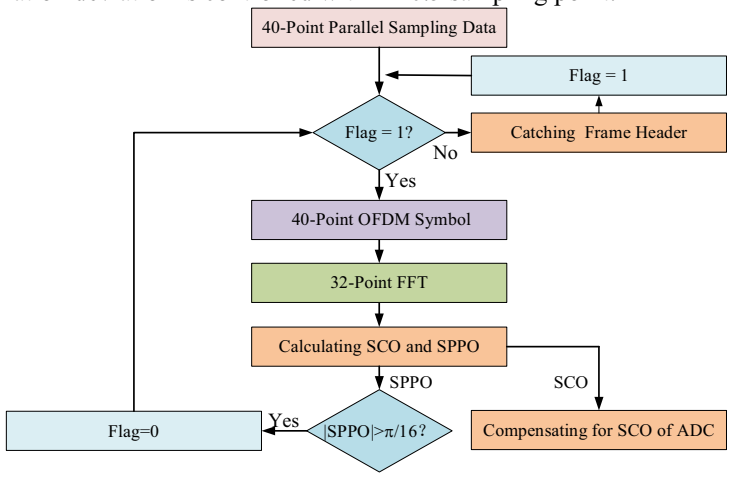

Figure 2. Flow diagram of the proposed symbol synchronization algorithm

Figure 2 shows a flow diagram of the proposed symbol synchronization algorithm in the IMDD-OOFDM system. If catching frame header succeeds, the flag is set to 1. Otherwise, the flag is set to 0. When the system starts to run, the flag is equal to 0. At this time, SPPO does not accumulate into the deviation of a sampling point. Therefore, the module of catching frame header receives 40-point parallel sampling data and utilizes the character of time-domain data of training sequence to catch frame header. When catching frame header is successful, the flag is set to 1. At this time, the system can know which sampling point in the 40-point parallel sampling data is starting position of the OFDM symbol and get complete 40-point OFDM symbols. System changes the time-domain data of OFDM symbols into the frequency-domain data of OFDM symbols through performing 32-point FFT. The module of calculating SCO and SPPO uses the frequency-domain data on subcarriers No. 1, 5, and 9 of OFDM symbols to calculate SCO and SPPO in real-time [3]. Finally, the value of SCO is sent to AD9554 through the SPI interface and AD9554 uses this value to compensate for the

SCO of ADC. At the same time, the value of SPPO can be used to determine whether the result of catching the frame header is valid. If the absolute value of SPPO is greater than $\pi/16$, which means the deviation of catching frame header is greater than 1 sampling point, the result of catching frame header is not valid. Therefore, the flag is set to 0 and the system starts catching the frame header again. If the absolute value of SPPO is less than $\pi/16$, the result of catching the frame header is always valid and the system can directly obtain complete 40-point OFDM symbols from 40-point parallel sampling data. Unlike the symbol synchronization of low-speed data streams which requires catching frame header for each frame, we proposed symbol synchronization algorithm does not require catching frame header for every frame. Therefore, the execution complexity of our catching frame header algorithm is much lower than that of low-speed data streams.

Using the correlation of time-domain data of training sequence catchs frame header. We assume that the time-domain data of the training sequence consists of A, B, and C in Eq. (1).

$$A=[a_{L-1},a_{L-2},\ldots,a_0],B=[b_{L-1},b_{L-2},\ldots,b_0],C=[c_{L-1},c_{L-2},\ldots,c_0],a_i=b_i=c_i,i\in[0,L-1] \tag{1}$$

We define R as the value of the correlation of A, B, and C in Eq. (2).

$$R=\sum_{i=0}^{L-1}|c_i-b_i|+|b_i-a_i| \tag{2}$$

Ideally, R is 0 in Eq. (2). Due to the existence of noise, the actual value of R is not equal to 0 but is very small. Because other OFDM symbols of the frame are not related to each other, the correlation values of these symbols are very large. Therefore, we can use R of the training sequence as judgment criteria for symbol synchronization. According to this characteristic, we calculate R between any $3\times L$-point sampling data in a frame and find the minimum value of R. Therefore, the sample point corresponding to this minimum value is the starting point of the training sequence. Namely, the header of each frame is found.

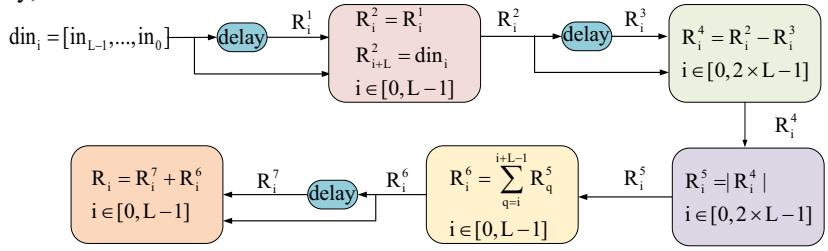

Figure 3. Eight-level pipeline architecture to calculate the R of each point in L-point parallel sampling data.

We design the eight-level pipeline architecture to calculate the R of each point in L-point parallel sampling data, as illustrated in Figure 3. The length of the OFDM symbol is L. The serial sampling data of ADC becomes L-point parallel sampling data after $1/L$ serial-to-parallel transformation. din_i is L-point parallel sampling

data. R_i is the R of each point of din_i. First-level, third-level, and seventh-level are delaying one clock cycle. Second-level is to transform two L-point parallel data into one $2\times L$-point parallel data. Four-level is subtraction operation. Fifth-level is the absolute value operation. Sixth-level is the sum of L-point data. Eighth-level is an addition operation. R_i^1, R_i^2, R_i^3, R_i^4, R_i^5, R_i^6, and R_i^7 are the results of each level.

According to the eight-level pipeline architecture, we can calculate the R of Eq. 2 for each point in L-point parallel sampling data. We suppose the length of the frame has M OFDM symbols. Each frame has $M\times L$ R according to this pipeline architecture. Therefore, the starting position of each frame can be determined by finding the minimum of $M\times L$ R. In this paper, the value of L is 40, and the value of M is 256. Therefore, each frame has 10240 R and R is the value of the correlation between each sampling point and the following 119 sampling points.

3. System equipment and results analysis

We have researched and implemented an equipment of the 1.5Gsa/s real-time IMDD-OOFDM system over 120km standard single mode fiber on the PCB integrating FPGA, ADC, DAC, and AD9554, as illustrated in Figure 4. We utilize the VIVADO software to get the value of sampling point phase offset and R of Eq. (2) and analyze them.

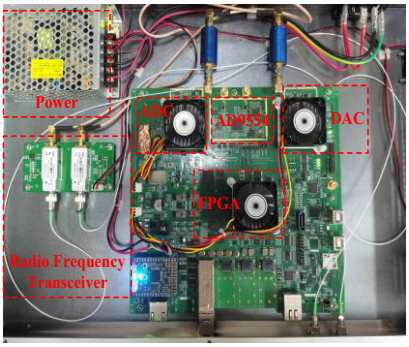

Figure 4. System equipment.

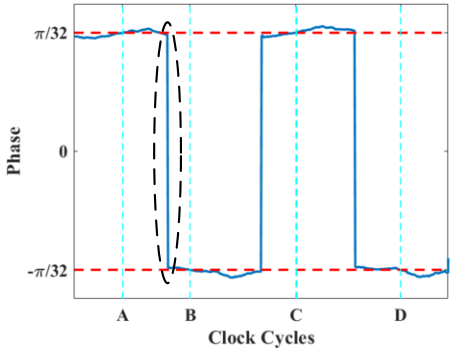

Figure 5. The curve of SPPO

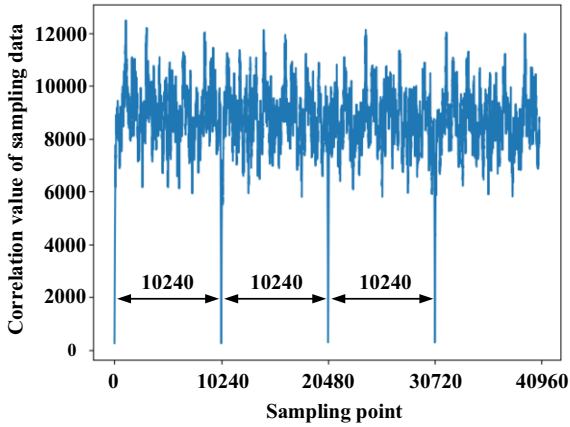

Figure 6. Frame header timing metric chart.

Figure 5 shows the curve of SPPO. When the absolute value of SPPO is equal to π/32 at A, B, C, and D, the value of SCO is sent to AD9554 through the SPI interface. After several clock cycles, the absolute value of SPPO begins to decrease. The value of SPPO is kept between positive and negative π/32 nearby. Because an OFDM symbol has a phase of 2π, 0.5 point of OFDM symbol represents a phase of π/32. Therefore, symbol synchronization deviation is controlled within ±0.5 sampling point. It is worth noting that the curve of SPPO is a similar sine curve with an ultra-long period. Due to VIVADO software's limited computing power, a complete period of SPPO's curve can't be measured. Therefore, we discretely measure the values of peak and trough of SPPO. As shown in Figure 5, the curve jump at the black dotted line ellipse is not a true phase jump but a measurement time gap between approximately positive and negative π/32. The other two curves jump for the same reason.

Figure 6 shows the frame header timing metric chart about symbol synchronization algorithm, whose abscissa is the number of sampling points and the ordinate is the value of R of Eq. (2) between each sampling point and the following 119 sampling points. As we can see from the chart, the sampling points corresponding to the four smallest correlation values are the starting points of the four frames header. The number of sampling points per frame is 10240(256×40=10240) and the intervals between the sampling points corresponding to the four smallest correlation values are also 10240 points. Therefore, the starting point of each frame header is located without any integer point deviation.

4. Conclusions

We have studied and implemented a new symbol synchronization algorithm for a high-speed data streams in a 1.5Gsa/s real-time FPGA-based IMDD-OOFDM system over 120km standard single mode fiber. The system experimentally demonstrated that the sampling point phase offset was approximately controlled within ±π/32 and symbol synchronization deviation was handled between -0.5 and +0.5 sampling points. It's worth noting that this symbol synchronization algorithm does not require symbol

synchronization for every frame and can be applied to symbol synchronization of wireless channel.

Acknowledgment

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