Dynamic power estimation based on switching activity propagation

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***Abstract*—A new power estimation approach based on the decomposition of a digital system into basic operators is presented. This approach aims to estimate the energy consumption at early design phases of digital blocks implemented on FPGAs. Each operator has its own model which estimates the switching activity and the power consumption. By interconnecting several operators, statistical information is then propagated to provide a global power estimation of a given system. A simple sum of the power dissipation contribution of each operator is enough to compute the total power consumption. This is performed by taking into account the switching activities relative to a given input pattern. Earlier, faster and more flexible power analysis for system designers are the advantages. This approach has been evaluated in a use-case application. The preliminary results indicate a promising speed-up of the design process and an error which is less than 8.0% compare to the classical power estimation tools.**

I. Introduction

Due to high-level integration, high operating frequencies and low cost, Field Programmable Gate Arrays (FPGAs) constitute one of the best solution for rapid prototyping. The major drawback of the FPGA, compared to their ASICs counterparts, is their relatively high power consumption since they are not optimized for a given application and are far more generic and flexible. To circumvent this issue, it is then necessary to optimize the power consumption in the FPGA design flow and estimate power in various design stages. The power estimation techniques in FPGA can be divided into two categories according to the abstraction level of the circuit: low level i.e. physical up to RTL (Register Transfer Level) and high level or system level. At low level, transistors, logic gates and registers are specified and fully described physically, whereas at high level, only a global structure view is considered. Generally, this last level lacks from technological details which are crucial to get an accurate information on the dissipated power. At low level, accurate power estimation may be achieved but with a significant simulation time that is often prohibitive.

In this paper, a new power estimation technique is presented, which consists of a high-level modeling and simulation of systems based on basic operators. Each operator has been carefully modeled using low-level information to benefit from the low level approach and get accurate results. Combining low-level information and high-level modeling leads to significantly speed-up the design process and provides accurate power estimation.

II. Related works

The total dissipated power has two origins: first the static power, second the dynamic power as shown in eq. 1.

$$P_{Total} = P_{Dyn} + P_{Stat} = \alpha C V_{dd}^2 f + V_{dd} I_{leakage} \quad (1)$$

where P_{Dyn} is the dynamic power and depends on the switching activity factor α, the node capacitance C, the supply voltage V_{dd}, and the frequency f. The static power P_{Stat} is estimated as $V_{dd}\ I_{leakage}$, where $I_{leakage}$ represents the leakage currents.

Probabilistic and statistical techniques are generally used for dynamic power estimation. Probabilistic methodology is based on the input probability of a signal pattern to estimate the internal transitions in a digital component. Signal probabilities are then propagated throughout the device to get the output probability. [1], [2]. The main drawback in probabilistic methods is that they do not take into account glitches and propagation delays although these factors have a significant impact on power estimation. Statistical techniques, as presented in [3], are based on randomly generated input patterns and consist in monitoring power dissipation through a specific power tool. With this approach, obtaining accurate results requires a huge number of input patterns to cover different scenarios. A significant simulation time is usually deplored and constitutes a critical limitation for these techniques. In the work of [4], a methodology was proposed, based on real measurements, which allows designers to model power consumption with architectural and algorithmic parameters. Design reuse is a key advantage of this method. In [5], a power estimation technique at RTL is proposed. It enables the power estimation of a macro (e.g. adder) or an IP directly from the study of the inputs/outputs statistical properties. Their models deliver an average error ranging from 9% to 15%.

III. methodology

In this paper, dynamic power is studied. Our assumption is that any hardware system can be represented by basic operators that exchange data with each other. In our model,

each operator may be fully characterized in terms of statistical input/output relationship and power consumption. More precisely, each component model consists of two sub-models $M1$ and $M2$ that are described in Fig. 1.

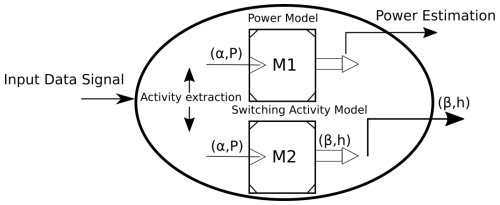

Fig. 1. Operator Model

$M1$ is used to estimate the dynamic power from the signal activity of the operator's inputs and from the percentage HIGH parameter. It provides an average of the energy consumed during a period of 1s. Inputs signal activity is expressed in terms of millions of transitions per second (Mtr/sec) whereas percentage HIGH represents the time ratio during which the signal is active HIGH in a clock period. $M2$ enables to estimate the signal activity of the outputs (as well as the percentage high). This sub-model is useful as designers want to propagate activity among all operators in order to obtain a global power estimation of the entire design.

The proposed methodology is composed of 2 steps. Step1: operators are characterized after being implemented on FPGA. A low-level power analyzer is used to estimate the average dynamic power that is consumed by each operator. $M1$ is then obtained after performing timing simulations with randomly generated input patterns i.e. switching activity rate and percentage high. Both (α, p) are the input patterns of the two models whereas power dissipation and (β, h) constitute the outputs for $M1$ and $M2$ respectively. Step2: a full system may be built by connecting different operators. This system is composed of power models and described in SystemC in order to ease the interoperability between components. For a system composed of N operators, assuming that the switching activity rate is α_i, and that p_i is the % high at the input of the op_i operator. Therefore (β_i,h_i) constitutes the output feature vector of this operator. α_1 and p_1 respectively correspond to the switching activity and percentage high at the input of the op_1 given by the input stimuli. $M_{1,i}$ and $M_{2,i}$ are the two models for op_i. By propagating these information to the next operators, the total estimated power can be expressed as in eq. 2.

$$P_{Global} = M_{1,1}(\alpha_1, p_1) + \sum_{i=2}^{N-1} M_{1,i}(\beta_{i-1}, h_{i-1}). \quad (2)$$

IV. Results

In order to demonstrate the feasibility of the approach, a particular case has been studied based on a multiplier accumulator (MAC) operator, and a parallel to serial converter (P2S). Based on these basic operators, a neural network circuit has been implemented on a Xilinx xc7z045ffg900 FPGA device. Each operator has been previously modeled as shown in Fig. 1. The full architecture of the neural network is depicted in Fig. 2. Note That $op1$ and $op2$ represent the MAC and P2S respectively. After high-level simulation of the neural network

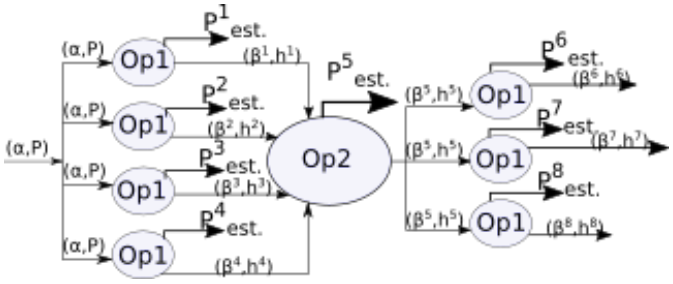

Fig. 2. Neural Network Model

model and parameters propagation, a first power value has been estimated ($P_{method} = 221.0\ mw$). This value can be compared to the value obtained when implementing the full neural network design on the FPGA ($P_{ref} = 239.0\ mW$). Note that, according to these results, the estimation error is only 7.5 %. Another estimation has been performed without parameters propagation (only 12.5 % default toggle rate has been considered). It returned $P_{default} = 166\ mW$ which corresponds to 30.5 % of error compared to the reference design.

V. Conclusion and future work

In this paper, we have proposed a new approach for the FPGA dynamic power estimation, at system level. It is achieved by the decomposition of a digital system into a set of basic operators. By propagating and summing up the estimated power computed for each operator, we obtain a global power estimation. The presented method allows designers to early perform power estimation in the design flow. We have shown that our method provides significant results, since the estimation error is less than 8%. We have then demonstrated that taking the signal activity and percentage HIGH parameters are sufficient enough to obtain a correct accuracy at high level. As future work, we will improve our models based on real power measurements, on various hardware platforms.

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