

A Multimode Hybrid Memristor-CMOS Prototyping Platform Supporting Digital and Analog Projects

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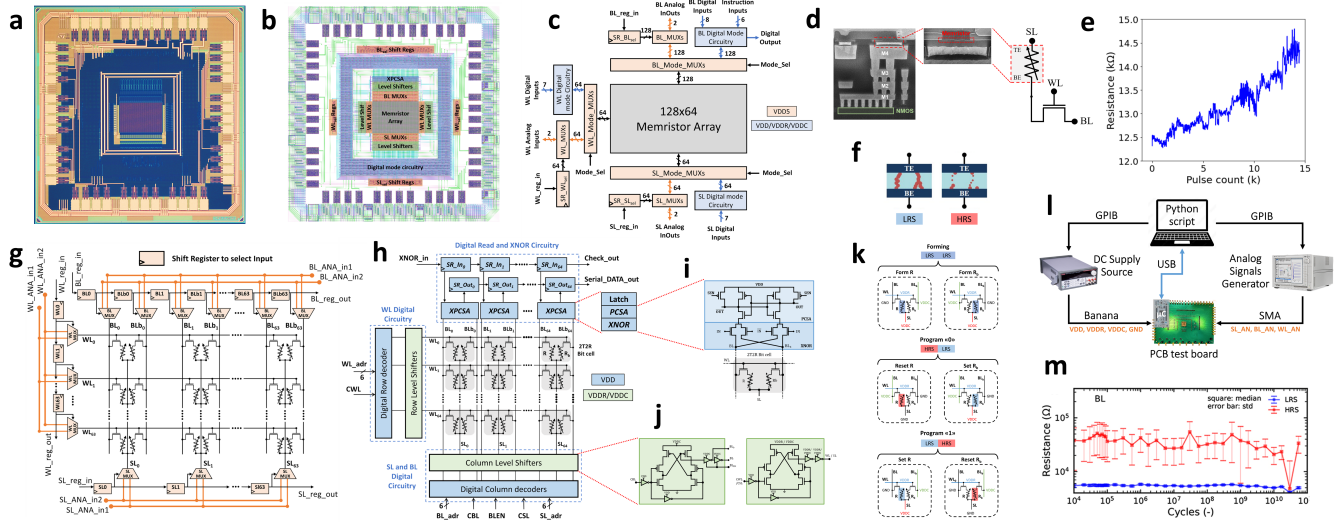


Figure 1: **a** Optical microscopy photograph, **b** layout view, and **c** schematic of the hybrid Memristor-CMOS die. **d** Electron microscopy image of a memristor in our hybrid memristor/CMOS process. **e** Measurement of memristor resistance as a function of number of RESET programming pulses, for implementing a synaptic learning rule. **f** Illustration of memristor programming states. **g** Schematic of the analog mode circuitry, with shift registers selecting inputs via Multiplexers. **h** Schematic of the digital mode circuitry, with a complementary 2T2R memristor basic cell. **i** Schematics of the sensing circuitry with XNOR logic-in-memory feature. **j** Schematic of the level shifters, used for shifting digital nominal voltage to forming and programming voltages of memristors. **k** Voltages applied for forming or programming a complementary cell in the digital mode. **l** Measurements setup of the prototyping platform. **m** Memristor endurance study, using the digital mode for programming and the analog mode for resistance measurements.

ABSTRACT

We present an integrated circuit fabricated in a process co-integrating CMOS and hafnium-oxide memristor technology, which provides a prototyping platform for projects involving memristors. Our circuit includes the periphery circuitry for using memristors within digital circuits, as well as an analog mode with direct access to memristors. The platform allows optimizing the conditions for reading and

writing memristors, as well as developing and testing innovative memristor-based neuromorphic concepts.

CCS CONCEPTS

• **Hardware** → **Memory and dense storage.**

KEYWORDS

memristor, RRAM, prototyping platform, neural networks.

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1 INTRODUCTION

Memristors, also known as resistive random access memories (RRAM) are a new type of memory technology fully embeddable in CMOS, providing a compact nonvolatile, and fast memory [6]. These devices provide fantastic opportunities to integrate logic and memory tightly and allow low-power computing, in particular for Artificial Intelligence models and neuromorphic computing [4]. Unfortunately, the behavior of memristors is highly complex and partly stochastic [3]: device models do not provide an accurate prediction of their behavior. It is therefore essential to prototype computing concepts involving memristors experimentally. However, appropriate platforms are extremely complex to fabricate due to the need to co-integrate commercial CMOS and memristor devices on the same die. In this work, we designed, fabricated, and tested a prototyping platform, associating an array of 8,192 hafnium-oxide-based memristors and a collection of CMOS periphery circuits. Our platform is multi-paradigm, which permits prototyping a wide range of both digital and analog projects.

2 DESCRIPTION OF THE DIE

A photograph and a layout view of our integrated circuit are presented in Figs. 1a-b. An electron microscopy image of a memristor in the backend of line of our hybrid memristor/CMOS process is shown in Fig. 1d. A commercial foundry fabricated the CMOS part (including the backend up to metal layer 4), using a 130-nanometer process. Afterward, we deposited the memristors on top of metal 4 using atomic layer deposition, and a fifth layer of metal.

Our integrated circuit embeds periphery circuitry enabling the use of memristors within two modes. Fig. 1c shows a simplified schematic of the circuit. It uses consistent color codes: blue-colored blocks are digital-mode circuits, designed using thin oxide low-power transistors and supplied by digital nominal voltage (except for level shifters), and orange-colored blocks are analog-mode circuits, designed using thick oxide transistors to be compatible with high voltages.

The digital mode circuits (Figs. 1h-k) consist of: row and column decoders to select devices based on input addresses, level shifters on each row and column, which shift digital nominal voltage to higher voltages required to form and program memristors, and precharge sense amplifiers, with a logic-in-memory feature, at each column [5]. These sense amplifiers allow reading the binary states of memory cells in a highly energy-efficient fashion while optionally performing logic operations at the same time. The complementary approach of [1] is used in our array for reducing the bit error rate.

When activating the analog mode (Figs. 1g), digital circuits are deactivated and the memristors array connections are switched to the analog circuitry. In this mode, shift registers configure input multiplexers permitting direct access to the analog state of memristors, using low-resistance transmission gates. Each word line, bit line, and source line is then connected to the ground or to one of two analog InOut Pads, which can be connected to external equipment, e.g., Keysight B1530, a pulse source and measurement unit widely used to characterize memory devices.

The memristor array and all analog and mixed-signal circuits were designed in a full custom fashion, based on an extensive work on memristor characterization, modeling, and simulation. All digital circuits were placed and routed automatically using an HDL

description and a Cadence Encounter flow provided by the foundry. Then, all circuits of the system were assembled manually and routed automatically using a Cadence Encounter flow developed in-house using a homemade abstract view of the memory array.

3 USES OF THE PLATFORM

To make the system re-configurable for different projects, we developed the experimental setup of Fig. 1l: a PCB routes a microcontroller unit and measurement equipment with our packaged die. Python scripts control the measurement.

Optimizing read and programming strategies using the digital mode can allow the successful implementation of digital applications. Memristors feature a complex interplay between programming energy, reading speed, read disturb effects, and device endurance, which our platform allows understanding. Fig. 1m shows an endurance study example. A memristor is programmed repeatedly using the digital mode circuits, and the memristor resistance is checked regularly using the analog mode and reported in Fig. 1m. It shows that the memristor resistance starts to degrade after 10^9 cycles, concurrently with the emergence of bit errors seen by the reads after each programming using sense amplifiers (not shown in Figures). We observed that memristor endurance can vary between 10^3 and 10^9 cycles depending on programming conditions.

The analog mode of the platform can be used to prototype computing concepts where memristors are used in an analog fashion, e.g., as artificial synapses in machine learning or neuromorphic circuits [4]. Fig. 1e shows measurements on a memristor in our platform when applying a succession of 15,000 1V 1.5- μ s programming pulses: the memristor resistance progressively increases, a feature that permits the memristor to implement a synaptic learning rule. This use is particularly appealing due to its compactness, but the imperfections of memristors (thermal and random telegraph noise, cycle-to-cycle, and device-to-device variability) pose challenges that make it necessary to test ideas experimentally. Our platform supports prototyping various neuromorphic experiments, targeting inference, deterministic or probabilistic learning [2].

4 CONCLUSION

We have designed, fabricated, and tested a flexible multi-paradigm platform to prototype and optimize digital and/or analog computing concepts, based on a hybrid CMOS/memristor integrated circuit. We are currently using it to validate multiple digital logic-in-memory and analog neuromorphic concepts, and plan to make the platform available to other research groups.

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