

Performance Analysis of Priority-Aware NoCs with Deflection Routing under Traffic Congestion

Sumit K. Mandal¹, Anish Krishnakumar¹, Raid Ayoub², Michael Kishinevsky², Umit Y. Ogras¹

¹Dept. of ECE, University of Wisconsin-Madison; ²Intel Corporation, Hillsboro, OR

ABSTRACT

Priority-aware networks-on-chip (NoCs) are used in industry to achieve predictable latency under different workload conditions. These NoCs incorporate deflection routing to minimize queuing resources within routers and achieve low latency during low traffic load. However, deflected packets can exacerbate congestion during high traffic load since they consume the NoC bandwidth. State-of-the-art analytical models for priority-aware NoCs ignore deflected traffic despite its significant latency impact during congestion. This paper proposes a novel analytical approach to estimate end-to-end latency of *priority-aware* NoCs with *deflection routing* under *bursty and heavy traffic* scenarios. Experimental evaluations show that the proposed technique outperforms alternative approaches and estimates the average latency for real applications with less than 8% error compared to cycle-accurate simulations.

CCS CONCEPTS

• **Networks** → **Network performance modeling**; • **Computer systems organization** → **System on a chip**;

1 INTRODUCTION

Pre-silicon design-space exploration and system-level simulations constitute a crucial component of the industrial design cycle [12, 27]. They are used to confirm that new generation designs meet power-performance targets before labor- and time-intensive RTL implementation starts [4]. Furthermore, virtual platforms combine power-performance simulators and functional models to enable firmware and software development while hardware design is in progress [21]. These pre-silicon evaluation environments incorporate cycle-accurate NoC simulators due to the criticality of shared communication and memory resources in overall performance [1, 16]. However, slow cycle-accurate simulators have become the major bottleneck of pre-silicon evaluation. Similarly, exhaustive design-space exploration is not feasible due to the long simulation times. Therefore, there is a strong need for fast, yet accurate, analytical models to replace cycle-accurate simulations to increase the speed and scope of pre-silicon evaluations [36].

Analytical NoC performance models are used primarily for fast design space exploration since they provide significant speed-up compared to detailed simulators [17, 18, 26, 30]. However, most

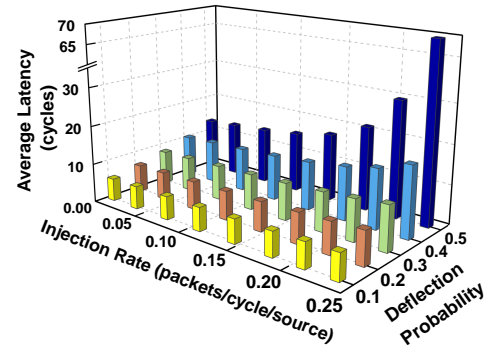


Figure 1: Cycle-accurate simulations on a 6×6 NoC show that the average latency increases significantly with larger deflection probability (p_d) at the sink.

existing analytical models fail to capture two important aspects of industrial NoCs [15]. *First*, they do not model routers that employ priority arbitration. *Second*, existing analytical models assume that the destination nodes always sink the incoming packets. In reality, network interfaces between the routers and cores have finite (and typically limited) ingress buffers. Hence, packets bounce (i.e., they are deflected) at the destination nodes when the ingress queue is full. Recently proposed performance models target priority-aware NoCs [23, 24]. However, these ignore deflection due to finite buffers and uses the packet injection rate as the primary input. This is a significant limitation since the deflection probability (p_d) increases both the hop count and traffic congestion. Indeed, Figure 1 shows that the average NoC latency increases significantly with the probability of deflection. For example, the average latency varies from 6–70 cycles for an injection rate of 0.25 packets/cycle/source when p_d varies from 0.1–0.5. Therefore, performance models for priority-aware NoCs have to account for deflection probability at the destinations.

This work proposes an accurate analytical model for *priority-aware NoCs with deflection routing under bursty traffic*. In addition to increasing the hop count, deflection routing also aggravates traffic congestion due to extra packets traveling in the network. Since the deflected packets also have a complex effect on the egress queues of the traffic sources, analytical modeling of priority-aware NoCs with deflection routing is challenging. To address this problem, we first need to approximate the probability distribution of inter-arrival time of deflected packets. Specifically, we compute the first two moments of inter-arrival time of deflected packets since we consider bursty traffic. To this end, the proposed approach starts with a canonical queuing system with deflection routing. We first model the distribution of deflected traffic and the average queuing delay for this system. However, this methodology is not scalable when the network has multiple queues with complex interactions between them. Therefore, we also propose a superposition-based

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technique to obtain the waiting time of the packets in arbitrarily sized industrial NoCs. This technique decomposes the queuing system into multiple subsystems. The structure of these subsystems is similar to the canonical queuing system. After deriving the analytical expressions for the parameters of the distribution model of deflected packets of individual subsystems, we superimpose the result to solve the original system with multiple queues. Thorough experimental evaluations with industrial NoCs and their cycle-accurate simulation models show that the proposed technique significantly outperforms prior approaches [18, 24]. In particular, the proposed technique achieves less than 8% modeling error when tested with real applications from different benchmark suites. *The major contributions of this work are as follows:*

- An accurate performance model for priority-aware NoCs with deflection routing under bursty traffic,
- An algorithm to obtain end-to-end latency using the proposed performance model,
- Detailed experimental evaluation with industrial priority-aware NoC under varying degrees of deflection.

The rest of this paper is organized as follows. Section 2 summarizes the related research. Section 3 presents the background and overview of the proposed work. Section 4 describes the proposed methodology to construct the analytical model for priority-aware NoCs, which considers deflection routing. Section 5 details experimental evaluations, and Section 6 concludes the paper.

2 RELATED WORK

Deflection routing was first introduced in the domain of optical NoC as hot-potato routing [7]. Later, it was adapted for the NoCs used in high-performance SoCs to minimize buffer requirements and increase energy efficiency [10, 11, 25]. This routing mechanism always assigns the packets to a free output port of a router, even if the assignment does not result in minimum latency. This way, the buffer size requirement in the routers is minimized. Authors in [22] perform a thorough study on the effectiveness of deflection routing for different NoC topology and routing algorithm. Deflection routing is also used in industrial priority-aware NoC [15]. Since arbitrary deflections can cause livelocks and unpredictable latency, industrial priority-aware NoCs deflect the packets only at the destination nodes when the ingress buffer is full. Furthermore, the deflected packets always remain within the same row or column, and they are guaranteed to be sunk after a fixed number of deflections.

NoC performance analysis techniques have been used for design space exploration and architectural studies such as buffer sizing [26, 28, 35]. However, most of these techniques do not consider NoCs with priority arbitration and deflection routing, which are the key features of industrial NoCs [15]. Performance analysis of priority-aware queuing networks has also been studied for off-chip networks [3, 6, 33]. These analytical models consider the queuing networks in continuous time. However, each transaction in NoC happens at each clock cycle. Therefore, the underlying queuing system needs to be considered in the discrete time domain. A performance analysis technique for a priority-aware queuing network in discrete time domain is presented in [33]. However, this technique

suffers from high complexity for a complex queuing network, hence not applicable to industrial priority-aware NoCs.

A recent technique targets priority-aware NoCs [18], but it considers only a single class of packets in each queue of the network. In contrast, industrial priority-aware NoCs have multiple classes of packets that can exist in the same queue. NoCs with multiple priority traffic classes has recently been analyzed in [24]. However, this analysis assumes that the input traffic follows a geometric distribution. This technique has limited applications since industrial NoCs can experience bursty traffic. Furthermore, it does not consider deflection routing. Since deflection routing increases traffic congestion, it is crucial to incorporate this aspect while constructing performance models. An analytical bound on maximum delay in networks with deflection routing is presented in [8]. However, evaluating maximum delay is not useful since it leads to significant overestimation. Another analytical model for NoCs with deflection routing is proposed in [13]. The authors first compute the blocking probability at each port of a router using an M/G/1 queuing model. Then, they compute the contention matrix at each router port. The average waiting time of packets at each port is computed using the contention matrix. However, this analysis ignores different priority classes and applies to only continuous-time queuing systems.

In contrast to prior work, we propose a performance analysis technique that considers **both priority-aware NoCs with deflection routing under bursty and high traffic load**. The proposed technique applies the superposition principle to obtain the statistical distribution of the deflected packets. Using this distribution, it computes the average waiting time for each queue. To the best of our knowledge, this is the first analytical model for priority-aware industrial NoCs with deflection routing under high traffic load.

3 BACKGROUND AND OVERVIEW

3.1 Assumptions and Notations

Architecture: This work considers priority-aware NoCs used in high-end servers and many core architectures [15]. Each column of the NoC architecture, shown in Figure 2, is also used in client systems such as Intel i7 processors [31]. Hence, the proposed analysis technique is broadly applicable to a wide range of industrial NoCs.

In priority-aware NoCs, the packets already in the network have higher priority than the packets waiting in the egress queues of the

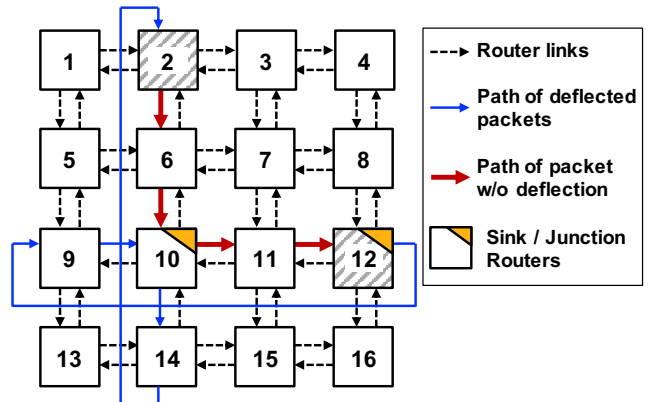


Figure 2: A representative 4x4 mesh with deflection routing.

sources. Assume that Node 2 in Figure 2 sends a packet to Node 12 following Y-X routing (highlighted by red arrows). Suppose that a packet in the egress queue of Node 6 collides with this packet. The packet from Node 2 to Node 12 will take precedence since the packets already in the NoC have higher priority. Hence, packets experience a queuing delay at the egress queues but have predictable latency until they reach the destination or turning point (Node 10 in Figure 2). Then, it competes with the packets already in the corresponding row. That is, the path from the source (Node 2) to the destination (Node 12) can be considered as two segments, which consist of a queuing delay followed by a predictable latency.

Deflection in priority-aware NoCs happens when the ingress queue at the turning point (Node 10) or final destination (Node 12) become full. This can happen if the receiving node, such as a cache controller, cannot process the packets fast enough. The probability of observing a full queue increases with smaller queues (needed to save area) and heavy traffic load from the cores. If the packet is deflected at the destination node, it circulates within the same row, as shown in Figure 2. Consequently, a combination of regular and deflected traffic can load the corresponding row and pressure the ingress queue at the turning point (Node 10). This, in turn, can lead to deflection on the column and propagates the congestion towards the source. Finally, if a packet is deflected more than a specific number of times, it reserves a slot in the ingress queue. This bounds the maximum number of deflections and avoids livelock.

Traffic: Industrial priority-aware NoCs can experience bursty traffic, which is characteristic of real applications [5, 30]. This work considers generalized geometric (GGeo) distribution for the input traffic, which takes burstiness into account [20]. GGeo traffic is characterized by an average injection rate (λ) and the coefficient of variation of inter-arrival time (C^A). We define a traffic class as the traffic of each source-destination pair. The average injection rate and coefficient of variation of inter-arrival time of class- i are denoted by λ_i and as C_i^A respectively, as shown in Table 1. Finally, the mean service time and coefficient of variation of inter-departure time of class- i are denoted as T_i and C_i^S .

3.2 Overview of the Proposed Approach

Our goal is to construct an accurate analytical model to compute the end-to-end latency for priority-aware NoCs with deflection routing. The proposed approach can be used to accelerate full system simulations and also to perform design space exploration. We assume that the parameters of the GGeo distribution of the input traffic to the NoC (λ, C^A) are known from the knowledge of the application. The proposed model uses the deflection probability (p_d) as the second major input, in contrast to existing techniques

Table 1: Summary of the notations used in this paper.

λ_i	Arrival rate of class- i
p_{d_j}	Deflection probability at sink- j
T_i, \hat{T}_i	Original and modified mean service time of class- i
ρ_i	Mean server utilization of class- i ($=\lambda_i T_i$)
C_i^A	Coefficient of variation of inter-arrival time of class- i
C_i^S, \hat{C}_i^S	Coefficient of variation of original and modified service time of class- i
C_i^D	Coefficient of variation of inter-departure time of class- i
C_i^M	Coefficient of variation of inter-departure time of merged traffic of class- i
W_i	Mean waiting time of class- i

that ignore deflection. Its range is found from architecture simulations as a function of the NoC architecture (topology, number of processors, and buffer sizes). Its analytical modeling is left for future work. The proposed analytical model utilizes the distribution of the input traffic to the NoC (λ, C^A) and the deflection probability (p_d) to compute the average end-to-end latency as a sum of four components: (1) Queuing delay at the source, (2) the latency from the source router to the junction router, (3) queuing delay at the junction router, and (4) the latency from the junction router to the destination. Note that all these components account for deflection, and it is challenging to compute them, especially under high traffic load.

4 METHODOLOGY

This section presents the proposed performance analysis technique for estimating the end-to-end latency for priority-aware NoCs with deflection routing. We first construct a model for a canonical system with a single traffic class, where the deflected traffic distribution is approximated using a GGeo distribution (Section 4.1). Subsequently, we introduce a scalable approach for a network with multiple traffic classes. In this approach, we first develop a solution for the canonical system. Then, employ the principle of superposition to extend the analytical model to larger and realistic NoCs with multiple traffic classes (Section 4.2). Finally, we propose an algorithm that uses our analytical models to compute the average end-to-end latency for a priority-aware NoC with deflection routing (Section 4.3).

4.1 An Illustration with a Single Traffic Class

Figure 3(a) shows an example of a single class input traffic and egress queue that inject traffic to a network with deflection routing. The input packets are buffered in the egress queue Q_i (analogous

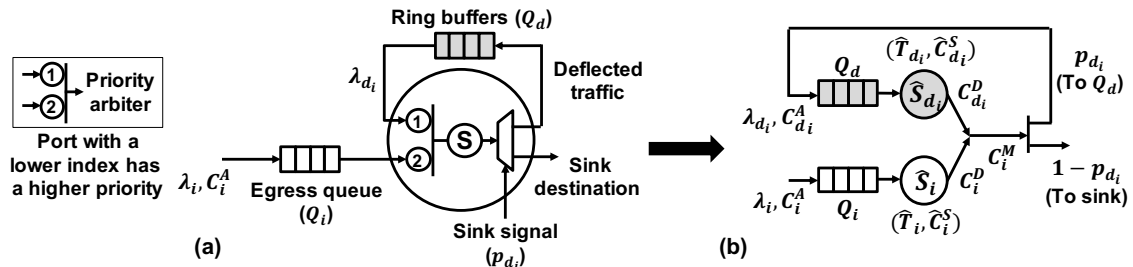


Figure 3: (a) Queuing system of a single class with deflection routing (b) Approximate queuing system to compute $C_{d_i}^A$.

to the packets stored in the egress queue of Node 2 in Figure 2). We denote the traffic of Q_i as class- i , which is modeled using GGeo distribution with two parameters (λ_i, C_i^A) . The packets in Q_i are dispatched to a priority arbiter and assigned a low priority, marked with ②. In contrast, the packets already in the network have a high priority, which are routed to the port marked with ①. The packet traverses a certain number of hops (similar to the latency from the source router to the junction router in Figure 2) and reaches the destination. Since the number of hops is constant for a particular traffic class, we omit these details in Figure 3(a) for simplicity. If the ingress queue at the destination is full (with probability p_{d_i}), the packet is deflected back into the network. Otherwise, it is consumed at the destination (with probability $1 - p_{d_i}$). Deflected packets travel through the NoC (within the column or row as illustrated in Figure 2) and pass through the source router, but this time with higher priority. The profile of the deflected packets in the network is modeled by a buffer (Q_d) in Figure 3(a), since they remain in order and have a fixed latency from the destination to the original source. This process continues until the destination can consume the deflected packets.

Our goal is to compute the average waiting time W_i in the source queue, i.e., components 1 and 3 of the end-to-end latency described in Section 3.2. To obtain W_i , we first need to derive the analytical expression for the rate of deflected packets of class- i (λ_{d_i}) and the coefficient of variation of inter-arrival time of the deflected packets ($C_{d_i}^A$) as follows.

Rate of deflected packets (λ_{d_i}): λ_{d_i} is obtained by calculating the average number of times a packet is deflected (N_{d_i}) until it is consumed at the destination as:

$$\begin{aligned} N_{d_i} &= p_{d_i}(1 - p_{d_i}) + 2p_{d_i}^2(1 - p_{d_i}) + \dots + np_{d_i}^n(1 - p_{d_i}) + \dots \\ &= \sum_{n=1}^{\infty} np_{d_i}^n(1 - p_{d_i}) = \frac{p_{d_i}}{1 - p_{d_i}} \end{aligned} \quad (1)$$

Therefore, λ_{d_i} can be expressed as:

$$\lambda_{d_i} = \lambda_i N_{d_i} = \lambda_i \frac{p_{d_i}}{1 - p_{d_i}} \quad (2)$$

Coefficient of variation of inter-arrival time of deflected packets ($C_{d_i}^A$): To compute $C_{d_i}^A$, the priority related interaction between the deflected traffic of Q_d and new injections in Q_i must be captured. This computation is more involved due to the priority arbitration between the packets in Q_d and Q_i that involve a circular dependency. We tackle this problem by transforming the system in Figure 3(a) into an approximate representation shown in Figure 3(b) to simplify the computations. The idea here is to transform the priority queuing with a shared resource into separate queue nodes (queue + server) with a modified server process. This transformation enables the decomposition of Q_d and Q_i and their shared server into individual queue nodes with servers \widehat{S}_d and \widehat{S}_i respectively. The departure traffic from these two nodes merge at the destination, consumed with a probability $1 - p_{d_i}$ and deflected otherwise.

The input traffic to the egress queue, as well as the deflected traffic, may exhibit bursty behavior. Indeed, the deflected traffic distribution can be bursty because of the server-process effect and the priority interactions between the input traffic and the deflected traffic, even when the input traffic is not bursty. Therefore, we

approximate the distribution of the deflected traffic via GGeo distribution. To compute the parameters of the GGeo traffic, we need to apply the principle of maximum entropy (ME) as shown in [20]. To obtain the modified service process of class- i , we first calculate the probability of no packets in Q_i and in its corresponding server (i.e., $p_{Q_i}(0)$) using ME as,

$$p_{Q_i}(0) = 1 - \rho_i - \rho_{d_i} \frac{\bar{n}_i}{\bar{n}_i + \rho_i + \rho_{d_i}} \quad (3)$$

where ρ_i and ρ_{d_i} denote the utilization of the respective servers, and \bar{n}_i is the occupancy of class- i in Q_i . Next, we apply Little's law to compute the first order moment of modified service time (\widehat{T}_i) as:

$$\widehat{T}_i = \frac{1 - p_{Q_i}(0)}{\lambda_i} \quad (4)$$

Subsequently, we obtain the effective coefficient of variation \widehat{C}_i^S as:

$$(\widehat{C}_i^S)^2 = \frac{(1 - \widehat{\rho}_i)(2\bar{n}_i + \widehat{\rho}_i) - \widehat{\rho}_i(C_i^A)^2}{\widehat{\rho}_i^2} \quad (5)$$

where $\widehat{\rho}_i = \lambda_i \widehat{T}_i$. We follow similar steps (Equation 3 – Equation 5) for the deflected traffic to obtain \widehat{T}_{d_i} and $\widehat{C}_{d_i}^S$. With the modified service process, the coefficients of variation of inter-departure time of the packets in Q_d ($C_{d_i}^D$) and Q_i (C_i^D) are computed using the process merging method [29]. Then, we find the coefficient of variation (C_i^M) of the merged traffic from queues Q_d and Q_i as:

$$(C_i^M)^2 = \frac{1}{\lambda_{d_i} + \lambda_i} (\lambda_{d_i}(C_{d_i}^D)^2 + \lambda_i(C_i^D)^2) \quad (6)$$

We note that C_i^M is a function of the coefficient of variation of the inter-arrival time of deflected traffic $C_{d_i}^A$. Since part of this merged traffic is consumed at the sink, we apply the traffic splitting method from [29] to approximate $C_{d_i}^A$ as:

$$(C_{d_i}^A)^2 = 1 + p_{d_i}((C_i^M)^2 - 1) \quad (7)$$

Finally, we extend the priority-aware formulations in continuous time domain [6] to discrete time domain to obtain the average waiting time of the packets in Q_{d_i} and Q_i :

$$W_{d_i} = \frac{\rho_{d_i}(T_{d_i} - 1) + \rho_i(T_i - 1) + T_{d_i}((C_{d_i}^A)^2 + \lambda_{d_i} - 1)}{2(1 - \rho_{d_i})} \quad (8)$$

$$W_i = \frac{\rho_{d_i}(T_{d_i} + 1) + 2\rho_{d_i}W_{d_i} + \rho_i(T_i - 1) + T_i((C_i^A)^2 + \lambda_i - 1)}{2(1 - \rho_i - \rho_{d_i})} \quad (9)$$

4.2 Queuing System with Multiple Traffic Classes

The analytical model for the system with a single class presented in Section 4.1 becomes intractable with a higher number of traffic classes. This section introduces a scalable approach based on the superposition principle that builds upon our canonical system used in Section 4.1.

Figure 4(a) shows an example with priority arbitration and N egress queues, one for each traffic class. We note that this queuing system is a simplified representation of a real system. The packets routed to port ① have higher priority than those routed to port ② for $i < j$. The deflected traffic in the network is buffered in Q_d , which has the highest priority in the queuing system. The primary goal is to model the queuing time of the packets of each traffic

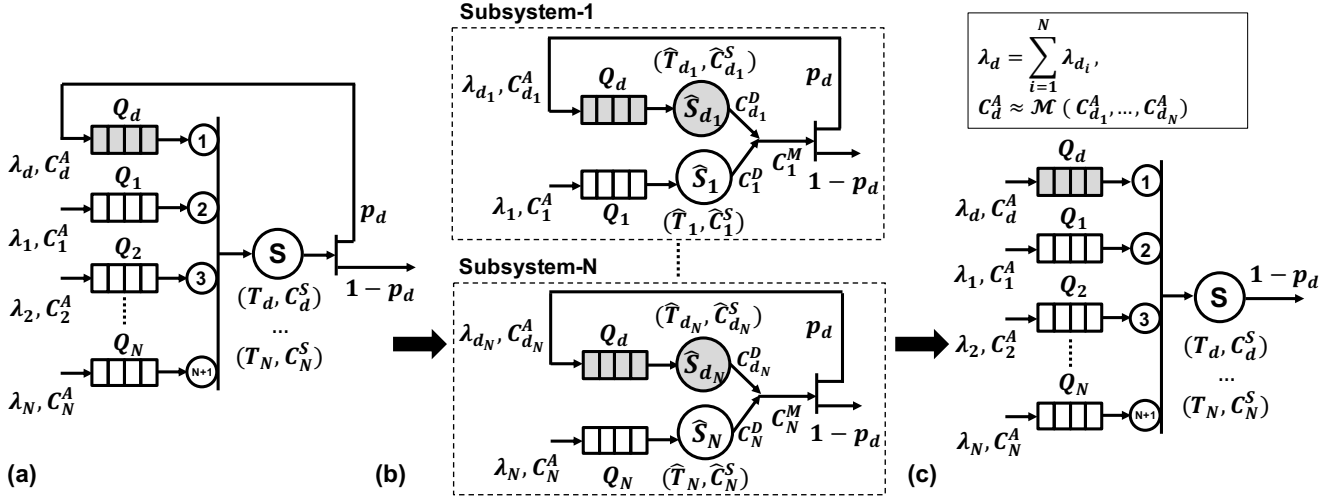


Figure 4: (a) Queuing system with N classes with deflection routing, (b) Decomposition into N subsystems to calculate GGeo parameters of deflected traffic per class, (c) Applying superposition to obtain the GGeo parameters of overall deflected traffic. \mathcal{M} denotes the merging process.

class. Modeling the coefficient of variations of the deflected traffic becomes harder since deflected packets interact with all traffic classes rather than a single class. These interactions complicate the analytical expressions significantly.

Priority arbitration enables us to sort the queues in the order at which the packets are served. The queue of the deflected packets has the highest priority, while the rest are ordered with respect to their indices. Due to this inherent order between the priority classes, their impact on the deflected traffic distribution can be approximated as being independent of each other. This property enables us to decompose the queuing system into multiple subsystems and model each subsystem separately, as illustrated in Figure 4(b). Then, we apply the principle of superposition to obtain the parameters of the GGeo distribution of the deflected traffic. Note that *each of these subsystems is identical to the canonical system analyzed in Section 4.1*. Hence, we first compute λ_{d_i} and $C_{d_i}^A$ of each subsystem- i following the procedure described in Section 4.1. Subsequently, we apply the superposition principle to λ_{d_i} and $C_{d_i}^A$ for $i = 1 \dots N$ to obtain the GGeo distribution parameters of the deflected traffic (λ_d, C_d^A) .

In general, we obtain the GGeo distribution parameters of the deflected traffic corresponding to class- i by setting all traffic classes to zero except class- i , ($\lambda_j = 0, j = 1 \dots N, j \neq i$). The values of λ_{d_i} and $C_{d_i}^A$ can be expressed as:

$$\lambda_{d_i} = \lambda_d \Big|_{\lambda_j=0, j \neq i; \lambda_i > 0} \quad \text{and} \quad C_{d_i}^A = C_d^A \Big|_{\lambda_j=0, j \neq i; \lambda_i > 0} \quad (10)$$

Subsequently, we apply the principle of superposition to obtain the distribution parameters of Q_d as shown in Figure 4(c). First, we compute λ_d by adding all λ_{d_i} as:

$$\lambda_d = \sum_{i=1}^N \lambda_{d_i} \quad (11)$$

The value of C_d^A is approximated by applying the superposition-based traffic merging process [29] for each $C_{d_i}^A$, as shown below:

$$(C_d^A)^2 = \sum_{i=1}^N \frac{\lambda_{d_i}}{\lambda_d} (C_{d_i}^A)^2 \quad (12)$$

Next, we use these distribution parameters (λ_d, C_d^A) of the deflected packets to calculate the waiting time of the traffic classes in the system. The formulation of the priority-aware queuing system is applied to obtain the waiting time of each traffic class- i (W_i) [3]:

$$W_i = \frac{\rho_d(T_d + 1) + 2\rho_i W_d}{2(1 - \rho_d - \sum_{n=1}^i \rho_n)} + \frac{\sum_{n=1}^{i-1} (\rho_n(T_n + 1) + 2\rho_n W_n)}{2(1 - \rho_d - \sum_{n=1}^i \rho_n)} + \frac{\rho_i(T_i - 1) + T_i((C_i^A)^2 + \lambda_i - 1)}{2(1 - \rho_d - \sum_{n=1}^i \rho_n)} \quad (13)$$

The first term in Equation 13 denotes the effect of deflected traffic on class- i ; the second term denotes the effect of higher priority classes (class- $j, j < i$) on class- i ; and the last term denotes the effect of class- i itself. For more complex scenarios that include traffic splits, we apply an iterative decomposition algorithm [23] to obtain the queuing time of different classes.

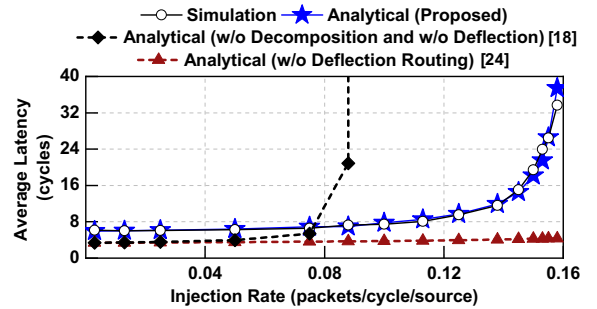


Figure 5: Comparison of average latency between simulation and analytical model for the canonical example shown in Figure 4 with $p_d = 0.3$ and $N = 5$.

Figure 5 shows the average latency comparison between the proposed analytical model and simulation for the system in Figure 4. In this setup, we assume the number of classes is 5 ($N = 5$), $p_d = 0.3$, and input traffic distribution is geometric. The results show that the analytical model performs well against the simulation, with only 4% error on average. In contrast, the analytical model from [18] highly overestimates the latency as it does not consider multiple traffic classes. The performance model of the priority-aware NoC in [24] accounts for multiple traffic classes, but it does not model deflection. Hence, it severely underestimates the average latency.

4.3 Summary & End-to-End Latency Estimation

Summary of the analytical modeling: We presented a scalable approach for the analytical model generation of end-to-end latency that handles multiple traffic classes of priority-aware NoCs with deflection routing. It applies the principle of superposition on subsystems where each subsystem is a canonical queuing system of a single traffic class to significantly simplify the approximation of the GGeo parameters of deflected traffic and in turn, the latency calculations.

End-to-End latency computation: Algorithm 1 describes the end-to-end latency computation with our proposed analytical model. The input parameters of the algorithm are the NoC topology, routing algorithm, service process of each server, input traffic distribution for each class, and deflection probability per sink. It outputs the average end-to-end latency (L_{avg}). First, the queuing system is decomposed into multiple subsystems as shown in Figure 4(b) and

Algorithm 1: End-to-end latency computation

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1 Input: NoC topology, routing algorithm, service process,
  input distribution for each class, ( $\lambda$ ,  $C_A$ ), deflection
  probability ( $p_d$ ) for each sink
2 Output: Average end-to-end latency ( $L_{avg}$ )
3  $S$  = set of all classes in the network
4  $N$  = number of queues in the network
5  $S_n$  = set of classes in queue  $n$ 
  /* Distribution of deflected traffic */
6 for  $i = 1: |S|$  do
7   Compute  $\lambda_{di}$  and  $C_{di}^A$  using Equation 10
8   Compute  $\lambda_d$  and  $C_d^A$  using Equation 11 and Equation 12
9 end
10 Compute  $W_d$  using  $\lambda_d$  and  $C_d^A$ 
  /* Average waiting time of each class */
11 for  $n = 1:N$  do
12   for  $s = 1: |S_n|$  do
13     Compute  $W_{ns}$  using Equation 13 (if  $|S_n| = 1$ )
14     Compute  $W_{ns}$  following the decomposition method
      in [23] (if  $|S_n| > 1$ )
15   end
16 end
17  $L_{avg} = \frac{\sum_{n=1}^N \sum_{s=1}^{|S_n|} (W_{ns} + L_{ns}) \lambda_{ns}}{\sum_{n=1}^N \sum_{s=1}^{|S_n|} \lambda_{ns}}$  (For mesh this term includes
  the latency both on the rows and the columns.)

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λ_{di} and C_{di}^A for each subsystem- i are computed. Subsequently, the proposed superposition methodology is applied to compute λ_d and C_d^A , shown in lines 6–9 of the algorithm. Then, λ_d and C_d^A are used to compute the average waiting time of the deflected packets (W_d). Then, the average waiting time for class- s in Q_n (W_{ns}) is computed as shown in lines 13–14. The service time combined with static latency from source to destination (L_{ns}) is added to W_{ns} to obtain the end-to-end latency. Finally, the average end-to-end latency (L_{avg}) is computed by taking a weighted average of the latency of each class, as shown in line 16 of the algorithm.

5 EXPERIMENTAL EVALUATIONS

This section validates the proposed analytical model against an industrial cycle-accurate NoC simulator under a wide range of traffic scenarios. The experiment scenarios include real applications and synthetic traffic that allow evaluations with varying injection rates and deflection probabilities. The evaluations include a 6×6 mesh NoC and a 6×1 ring as representative examples of high-end server CPUs [15] and high-end client CPUs [31], respectively. In both cases, the traffic sources emulate high-end CPU cores with a 100% hit rate on the shared last level cache (LLC) to load the NoCs. The target platforms are more powerful than experimental [32] and special-purpose [34] platforms with simple cores, although the mesh size is smaller. To further demonstrate the scalability of the proposed approach, we also present results with mesh sizes up to 16×16 . All cycle-accurate simulations run for 200K cycles, with a warm-up period of 20K cycles, to allow the NoC to reach the steady-state.

5.1 Estimation of Deflected Traffic

One of the key components of the proposed analytical model is estimating the average number of deflected packets. This section evaluates the accuracy of this estimation compared to simulation with a 6×6 mesh. To perform evaluations under heavy load, we set the deflection probability at each junction and sink to $p_d = 0.3$ and injection rates at each source to 0.33 packets/cycle/source, which are relatively large values seen in actual systems. We first run cycle-accurate simulations to obtain the average number of deflected packets at each row and column of the mesh. Then, the analytical model estimates the same quantities for the 6×6 mesh. Figure 6 shows the estimation accuracy for all rows and columns. The average estimation accuracy across all rows and columns is 96% and the worst-case accuracy is 92%. Overall, this evaluation

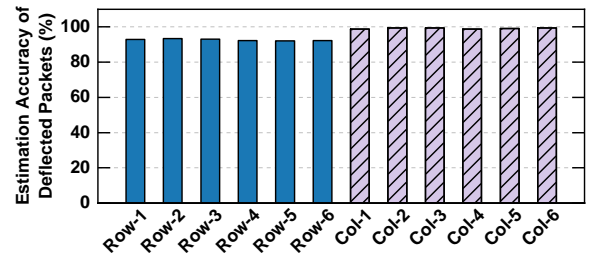


Figure 6: Estimation accuracy of average number of packets deflected for each row and column in a 6×6 mesh with $p_d = 0.3$.

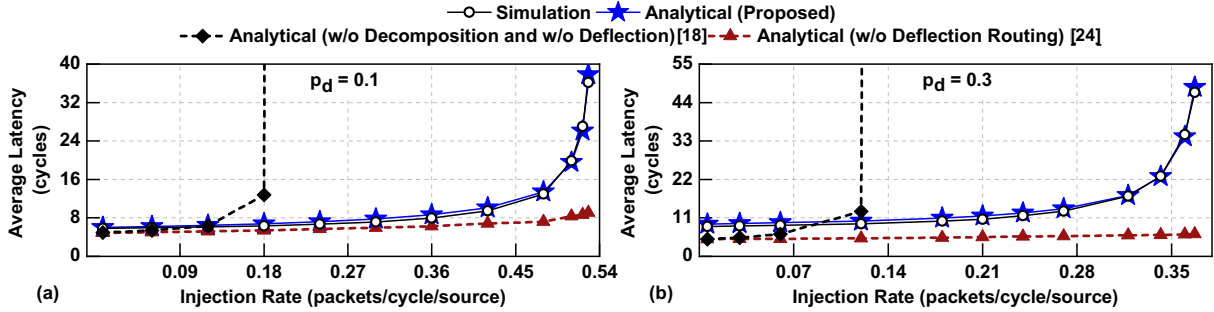


Figure 7: Comparison of average latency between simulation, the analytical model proposed in this work, and analytical models proposed in [18, 24] for a 6×6 mesh with deflection probability (a) 0.1 and (b) 0.3.

shows that the proposed model accurately estimates the average number of deflected packets.

5.2 Evaluations with Geometric Traffic Input

This section evaluates the accuracy of our latency estimation technique when the sources inject packets following a geometric traffic distribution. We note that our technique can also handle bursty traffic, which is significantly harder. However, we start with this assumption to make a fair comparison to two state-of-the-art techniques from the literature [18, 24]. The model presented in [18] does not incorporate multiple traffic classes and deflection routing. On the other hand, the model presented in [24] considers multiple traffic classes but does not consider bursty traffic and deflection routing.

The evaluations are performed first on the server-like 6×6 mesh for deflection probabilities $p_d = 0.1$ and $p_d = 0.3$ while sweeping the packet injection rates. Figure 7(a) and Figure 7(b) show that the proposed technique follows the simulation results closely for all injections. More specifically, the proposed analytical model has only 7% and 6% percentage error on average for deflection probabilities of 0.1 and 0.3, respectively. In sharp contrast, the analytical model proposed in [18] significantly overestimates the latency starting with moderate injection rates, since it does not consider multiple traffic classes. Its performance degrades even further with larger deflection probability, as depicted in Figure 7(b). We note that it also slightly underestimates the latency at low injection rates since it ignores deflection. Unlike this approach, the technique presented in [24] considers multiple traffic classes in the same queue, but it ignores deflected packets. Consequently, it severely underestimates the latency impact of deflection, as shown in Figure 7.

We repeated the same evaluation on a 6×1 priority-aware ring NoC which follows a high-end industrial quad-core CPU with an integrated GPU and memory-controller [15]. The average error between the proposed analytical model and simulations are 7%

and 4% for deflection probabilities of 0.1 and 0.3, respectively. In contrast, the model presented in [18] underestimates the latency at low injection rates and significantly overestimates it under high traffic load similar to the 6×6 results in Figure 7. Similarly, the analytical model presented in [24] severely underestimates the average latency. It leads to an average 43% error with respect to simulation. The plots of these results are not included for space considerations since they closely follow the results in Figure 7.

5.3 Latency Estimation with Bursty Traffic Input

Since real applications exhibit burstiness, it is crucial to perform accurate analytical modeling under bursty traffic. Therefore, this section presents the comparison of our proposed analytical model with respect to simulation under bursty traffic. For an extensive and thorough validation, we sweep the packet injection rate (λ), probability of burstiness (p_{br}), and deflection probability (p_d). The injection rates cover a wide range to capture various traffic congestion scenarios in the network. Likewise, we report evaluation results for two different burstiness ($p_{br} = \{0.2, 0.6\}$), and three different deflection probabilities ($p_d = \{0.1, 0.2, 0.3\}$). The coefficient of variation for the input traffic (C_A), the final input to the model, is then computed as a function of p_{br} and λ [19]. We simulate the 6×6 mesh and 6×1 ring NoCs using their cycle-accurate models for all input parameter values mentioned above. Then, we estimate the average packet latencies using the proposed technique, as well as the most relevant prior work [18, 24].

The estimation error of all three performance analysis techniques is reported in Table 2 for all input parameters. The mean and median estimation errors of our proposed technique are 9.3% and 9.5%, respectively. Furthermore, we do not observe more than 14% error even with relatively higher traffic load, probability of deflection, and burstiness than seen in real applications (presented in the following section). In strong contrast, the analytical models proposed

Table 2: Validation of the proposed analytical model for 6×6 mesh and 6×1 ring with bursty traffic arrival, and comparisons against prior work [18, 24]. ‘E’ signifies error >100%.

Topo.	6×6 Mesh						6×1 Ring																													
	0.1		0.2		0.3		0.1		0.2		0.3																									
	p_{br}	λ	p_{br}	λ	p_{br}	λ	p_{br}	λ	p_{br}	λ	p_{br}	λ																								
Error (%)	7.3	9.6	8.1	14	13	14	8.9	8.0	7.7	13	12	12	9.6	9.2	6.5	11	12	13	1.0	4.1	5.8	4.6	5.2	5.5	0.7	2.3	4.2	6.3	7.3	8.6	0.7	0.9	3.3	6.3	8.5	8.6
Ref[18]	2.6	E	E	26	E	E	22	E	E	39	E	E	35	18	E	57	E	E	7.0	E	E	34	E	E	23	E	E	45	E	E	42	E	E	54	E	E
Ref[24]	12	15	23	3.1	18	23	28	41	65	19	33	49	42	45	55	39	35	31	15.3	18	22	18	24	33	30	38	67	31	44	54	41	50	73	42	50	58

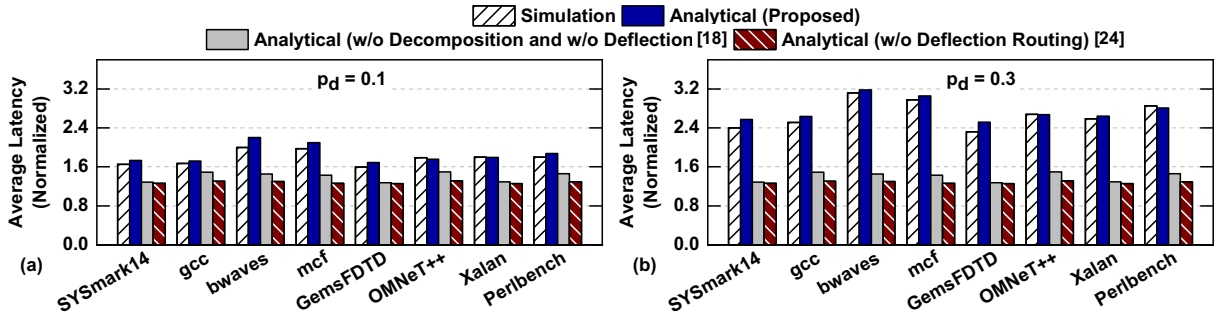


Figure 8: Average latency comparison between simulation, the analytical model proposed in this work, and analytical models proposed in [18, 24] for a 6×6 mesh with (a) $p_d = 0.1$ and (b) $p_d = 0.3$.

in [18] severely overestimate the latency similar to the results presented in Section 5.2. The estimation error is more than 100% for most cases since the impact of multiple traffic classes and deflected packet become more significant under these challenging scenarios. Similarly, the model proposed in [24] underestimates the latency because it does not model bursty traffic.

The right-hand side of Table 2 summarizes the estimation errors obtained on the 6×1 ring NoC that follows high-end client systems. In most cases, the error with the proposed analytical model is within 10% of simulation, and the error is as low as 1%. With $p_d = 0.1$, $p_{br} = 0.6$ and $\lambda = 0.4$, the error is 14%, which is acceptable, considering that the network is severely congested. In contrast, the analytical models proposed in [18] overestimate the latency, whereas the models in [24] underestimate the latency which conforms the results with geometric traffic, as in the 6×6 mesh results.

5.4 Experiments with Real Applications

In addition to the synthetic traffic, the proposed analytical model is evaluated with applications from SPEC CPU@2006 [14], SPEC CPU@2017 benchmark suites [9], and the SYSmark@2014 application [2]. Specifically, the evaluation includes SYSmark14, gcc, bwaves, mcf, GemsFDTD, OMNeT++, Xalan, and perlbench applications. The chosen applications represent a variety of injection rates for each source in the NoC and different levels of burstiness. Each application is profiled offline to find the input traffic parameters. Of note, the probability of burstiness for these applications ranges from $p_b = 0.25$ to $p_b = 0.55$, which is aligned with the evaluations in Section 5.3.

The benchmark applications are executed on both 6×6 mesh and 6×1 ring architectures. The comparison of average latency between simulation and proposed analytical model for the 6×6 mesh is shown in Figure 8. The proposed model follows the simulation results very closely for deflection probability $p_d = 0.1$ and $p_d = 0.3$, as shown in Figure 8(a) and Figure 8(b), respectively. These plots show the average packet latencies normalized to the smallest latency from the 6×1 ring simulations due to the confidentiality of the results. On average, the proposed analytical model achieves less than 5% modeling error. In contrast, the analytical models which do not consider deflection routing [18, 24] underestimate the latency, since the injection rates of these applications are in the range of 0.02–0.1 flits/cycle/source (low injection region).

We observe similar results for the 6×1 ring NoC. The average estimation error of our proposed technique is less than 8% for all applications. In contrast, the prior techniques underestimate the

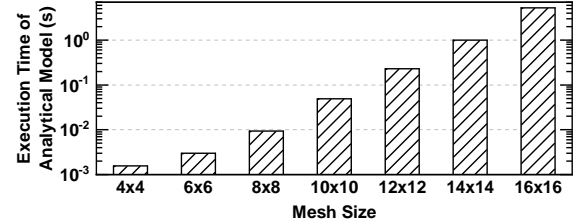


Figure 9: Execution time of the proposed analytical model (in seconds) for different mesh sizes.

latency by more than $2 \times$ since they ignore deflected packets, and the average traffic loads are small. In conclusion, the proposed technique outperforms state-of-the-art for real applications and a wide range of synthetic traffic inputs.

5.5 Scalability Analysis

Finally, we evaluate the scalability of the proposed technique for larger NoCs. We note that accuracy results for larger NoCs are not available since they do not have detailed cycle-accurate simulation models. We implemented the analytical model in C. Figure 9 shows that the analysis completes in the order of seconds for up to 16×16 mesh. In comparison, cycle-accurate simulations take hours with this size, even considering linear scaling. When we scale the mesh size aggressively to 16×16 , the analysis completes in about 5 seconds, which is orders of magnitude faster than cycle-accurate simulations of NoCs of this size.

6 CONCLUSIONS

Industrial NoCs incorporate priority-arbitration and deflection routing to minimize buffer requirement and achieve predictable latency. Analytical performance modeling of these NoCs is needed to perform design space exploration, fast system simulations, and tuning architectural parameters. However, state-of-the-art performance analysis models for NoCs do not incorporate priority arbitration and deflection routing together. This paper presented a performance analysis technique for industrial priority aware NoCs with deflection routing under heavy traffic. Experimental evaluations with industrial NoCs show that the proposed technique significantly outperforms existing analytical models under both real application and a wide range of synthetic traffic workloads.

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