A Direct-Sequence Spread-Spectrum Communication System for Integrated Sensor Microsystems

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***Abstract*—Some of the most important challenges in health-care technologies have been identified to be development of noninvasive systems and miniaturization. In developing the core technologies, progress is required in pushing the limits of miniaturization, minimizing the costs and power consumption of microsystems components, developing mobile/wireless communication infrastructures and computing technologies that are reliable. The implementation of such miniaturized systems has become feasible by the advent of system-on-chip technology, which enables us to integrate most of the components of a system on to a single chip. One of the most important tasks in such a system is to convey information reliably on a multiple-access-based environment. When considering the design of telecommunication system for such a network, the receiver is the key performance critical block. The paper describes the application environment, the choice of the communication protocol, the implementation of the transmitter and receiver circuitry, and research work carried out on studying the impact of input data characteristics and internal data path complexity on area and power performance of the receiver. We provide results using a test data recorded from a pH sensor. The results demonstrate satisfying functionality, area, and power constraints even when a degree of programmability is incorporated in the system.**

***Index Terms*—Communication, sensor systems, spread spectrum, system-on-chip (SoC).**

I. Introduction

SOME OF the most important challenges in health-care technologies have been identified to be development of noninvasive or minimally invasive systems and miniaturization [1]. In developing the core technologies, progress is required in pushing the limits of miniaturization, minimizing the costs and power consumption of microsystems components, developing mobile/wireless communication infrastructures, and computing technologies that are reliable, pervasive, and can be adapted to accommodate new applications and services [2]. There has been a general interest in the development of miniaturized and low-power integrated sensor microsystems in many fields such as medical diagnosis [3], environmental monitoring [4], biomedical telemetry [5], and other industrial applications.

Manuscript received April 15, 2003; revised April 6, 2004. This work was supported by the Scottish Higher Education Founding Council (RDG 130).

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Digital Object Identifier 10.1109/TITB.2004.837825

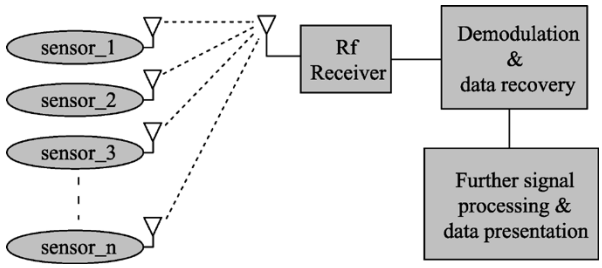

Fig. 1. A conceptual representation of typical multiple sensor systems—one base-station communication scenario.

Wireless implantable sensors are also increasingly being used in the medical field [3]. The advent of system-on-chip (SoC) technology [6], which enables us to integrate most of the components of a system on to a single chip accelerated these interests and made it feasible to shrink the size of such systems, while increasing their functionality. For example, the microsensor system can be swallowed by a human/animal or dropped into an environment to be measured or monitored. Then it will communicate with remote centers of expertise for diagnosis and follow-up action. One such system is an ingestible electronic capsule [7], which integrates several sensors, amplifiers, analog–digital converter (ADC), and includes microsystem scheduling, coding, and transmitting circuitry [8], [9]. The system is able to monitor some common physiological parameters of gastrointestinal tract such as temperature, pH, conductivity, and oxygen concentration [10], [11].

One of the main problems of such a system is how to retrieve information from the sensor system in real-time nonintrusively. The most feasible solution is to integrate a wireless communication circuit into the system which constitutes an important part of an SoC implementation. Some of the desirable properties of the communication system are capable of communicating with multiple sensor systems for the purpose of centrally monitoring or controlling more than one medium at the same time and interference rejection for reliable communication in critical applications such as medical diagnosis. A conceptual representation of a desirable system is shown in Fig. 1. In this system, each sensor will be able to transmit data at the same time and frequency using a unique code assigned to it. The receiver will receive the combined signal. The receiver will also know the codes and will have a correlator for each sensor. Ideally, each code at the receiver will correlate with the respective sensor data ignoring the others. Preliminary results of such a system-design attempt have been reported in [12] and [13]. In fact, the goal is to provide an energy-efficient and scalable solution for a range of sensor applications. There are several

TABLE I
NOMENCLATURE

ADC	Analog-digital converter
CDMA	Code-division multiple access
CMOS	Complementary metal-oxide-semiconductor
DS-SS	Direct sequence spread spectrum
FDMA	Frequency-division multiple access
HDL	Hardware Description Language
L	Length of PN code
LFSR	Linear feedback shift register
MAC	Multiplier-accumulator circuit
PN	Pseudo-random noise
$r_{xy}(k)$	Cross-correlation between signals $x(n)$ and $y(n)$
SoC	System-on-chip
SS	Spread spectrum
TDMA	Time-division multiple access
VLSI	Very large scale integration

differences between distributed microsensor networks and conventional wireless multimedia networks. These include lower transmission distances (<10 m), lower bit rates (typically < kb/s), the need for collaboration (sensor data fusion), limited battery capacity (volume constraints), time varying resources (e.g., energy), and quality requirements.[1] These requirements translate to several interesting technical challenges. The low bit rates imply that the electronic circuits must be designed for low duty cycles. Commercial radio transceivers are unacceptable for these applications due to their high-energy overhead of turning ON and OFF [14]. In addition, innovative solutions to transceiver design are required to achieve efficient transmission of short packets over short distances. Programmability is a key requirement and techniques for energy efficient software needs to be developed. In this paper, we present the theoretical bases of our approach and describe design and implementation of a communication system to fulfill some of these requirements. The nomenclature used in this paper is listed in Table I.

II. MULTIPLE-ACCESS SYSTEMS

In a multiple-access system, a large number of users share a common channel to transmit information to a receiver. Within a communication system, we have a fixed amount of resources, a fixed amount of spectrum, a fixed amount of equipment, and a fixed number of channels. We also have multiple subscriber units which are trying to access the system at the same time. The system has to manage resources appropriately in order to cover and support all the users that want to access the system. There are three common technologies used to create a wireless interface: frequency-division multiple-access (FDMA), time-division multiple-access (TDMA), and code-division multiple-access (CDMA) [15]. In FDMA, the available channel bandwidth is subdivided into a number of frequency nonoverlapping channels. These subchannels are assigned to each user upon request by the users. FDMA allocates a single channel to one user at a time. Although technically simple to implement, FDMA is wasteful of bandwidth. TDMA relies upon the fact that the signal has been digitized, that is, divided into a number of packets. It allocates a single frequency channel for a short time and then moves to another channel. The digital samples from a single transmitter occupy different time slots in several bands at the same time. The main drawback is that with narrower bandwidth there is grater distortion. In an environment where the transmission from the various users is bursty and low duty cycle, FDMA and TDMA tend to be inefficient because a certain percentage of the available frequency slots or time slots assigned to user do not carry information [16]. This inefficiency in a multiple-access system limits the number of simultaneous users of the channel. An alternative to FDMA and TDMA is to allow more than one user to share a channel by use of direct-sequence spread-spectrum (DS-SS) signals [17], [18].

[1]The MIT AMPS Project. [Online]. Available: http://www-mtl.mit.edu/research/icsystems/uamps/.

TABLE II
DS-SS CODING OF DATA SEQUENCE '101'

Data	1	0	1
Coding	$\overline{PN}$	PN	$\overline{PN}$
DS-SS	1010110	0101001	1010110
Bipolar	-1,1,-1,1,-1,-1,1	1,-1,1,-1,1,1,-1	-1,1,-1,1,-1,-1,1

A. DS-SS

In the DS-SS system, each user is assigned a unique code sequence [19] that allows the user to spread the information signal across the assigned frequency band. Signals from the various users are separated at the receiver by cross correlation of the received signal with each of the possible user code sequences. Possible narrow-band interference is also suppressed in this process. By designing these code sequences to have relatively small cross correlation, the crosstalk inherent in the demodulation of the signals received from multiple transmitters is minimized. This multiple-access method is CDMA [20]–[22], which is a form of a DS-SS system. It is the spectral spreading of the transmitted signal that gives CDMA its multiple access capability. In order to classify a system as spread-spectrum (SS) modulated system, the transmission bandwidth must be much larger than the information bandwidth and the resulting radio-frequency (RF) bandwidth must be determined by a function other than the information being sent. The SS modulation transforms an information-bearing signal into a transmission signal with a much larger bandwidth. This transformation is achieved by encoding the information signal with a code signal that is independent of the data and has much larger spectral width than the data signal. This spreads the original signal power over a much broader bandwidth, resulting in a lower power density. The DS-SS transmitter is a fairly simple circuit in its basic form. The data is spread by multiplying with a pseudorandom noise (PN) code. A PN sequence (code) is a binary sequence that exhibits randomness properties but has a finite length and is, therefore, deterministic. PN codes are used to implement synchronization and uniquely code individual user signals across the transmission interface. PN generators are based on linear feedback shift registers (LFSRs) [23], [24]. The multiplication process is a simple modulo-2 addition. This multiplication also acts as a phase modulator. Consider a data sequence consisting of "101" is to be transmitted by using a PN code given as "0 101 001." Resulting DS-SS coding is shown in Table II. In practice, the data is transmitted by using bipolar format for convenience. Binary "1" is represented by "-1," and binary "0" by "$+1$." The mean of the transmitted signal will

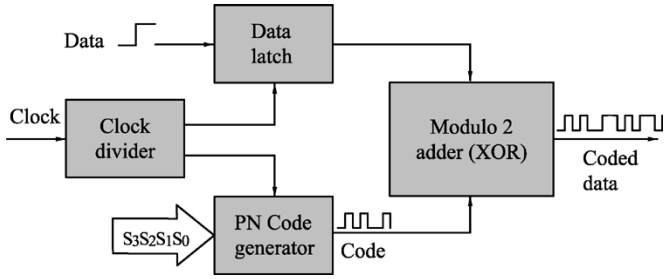

Fig. 2. The block diagram of the DS-SS transmitter.

be approximately "0." This convention will eliminate the *dc* component of the signal and has also a significant implication in the receiver as will be discussed later.

The DS-SS receiver, which is based on a correlator, exploits correlation properties of the PN codes [23]. The correlators attempt to match the incoming received signal with each of the candidate prototype waveforms known *a priori* to the receiver. In fact, it is a measure of similarities of two signals. Since we deal with the discrete signals in practice, the discrete form of the correlation of two discrete signals is given as

$$r_{xy}(k) = \sum_{n=0}^{N-1} x(n)y(k+n)dt. \tag{1}$$

Equation (1) is the fundamental equation implemented in software and hardware. The hardware implication of (1) is that the implementation of a correlator is based on a multiplier-accumulator circuit (MAC). At the receiver, the same PN code used in transmitter is correlated with an incoming signal. Assuming an ideal transmission, if the PN code and the incoming signal are identical, it is apparent from (1) that the correlator output will yield a positive peak output at zero phase shifts. If the input signal is 180° out of phase. the correlator output will yield a negative peak output. Then a threshold function recovers the original data. At other phases, the output of the correlator will ideally be zero. However, this is the case when the PN code length is infinite, which is unrealizable. In practice, a finite length of PN code is used. Therefore, there is a certain degree of correlation between incoming signal and the PN code at phases other than zero.

III. Design Considerations

A. Transmitter Design

A block diagram of the transmitter is given in Fig. 2. The heart of the DS-SS transmitter is the PN generator. Two different transmitters were designed and implemented. The first, a DS-SS transmitter based on a fixed length PN code generator, was designed. The PN code generator was capable of generating up to nine different codes depending on code-select inputs. A seven-stage LFSR giving maximum 127 code length was used. The transmitter output data rate was 127 times higher than the input data rate. In the second design, the degree of programmability was extended to enabling the choice of appropriate PN code with different lengths. The PN generator consists of eight stages LFSR and a multiplexer. General rule for the required LFSR stages can be given as $log_2(L+1)$, where L is the PN code length. The PN code length was programmable to provide an appropriate amount of data spreading for a particular application. One of the 12 different codes (three for each length in this application) is available depending on code-select inputs $(s_3s_2s_1s_0)$, as given in Table III. Code select input 0000 disables the PN generator and bypasses coding. The transmitter output data rate in the second design is L times higher than the input data rate. The structure of the programmable LFSR-based PN generator is illustrated in Fig. 3. The upper two bits of code-select input (s_3s_2) determine the PN code length and active LFSR stages, and multiplexes the appropriate PN code to the output pin. The required feedback combination is selected by setting the remaining bits of code-select input (s_1s_0) to the appropriate logic levels, as given in Table III. The transmitter also comprises a memory block for storage of data, a clock divider providing appropriate clock for the memory block and the PN generator, and a block of logic gates to perform the data coding and spreading. In LFSR implementation all-zero state (all-one state if XNOR is used at the feedback path) is not allowed. In the second design, this was prevented by an additional control circuit. This rearrangement also enables us to generate even-length PN codes by inserting an additional zero to a code sequence. Serial bit stream data to be transmitted is coded by either the PN code if the bit is logic 0° or a 180° phase-shifted version of the PN code if the bit is Logic 1. This coding is performed automatically by the EXOR operation.

The DS-SS transmitter was integrated to sensor microsystem together with an RF transmitter. The transmission frequency was 40.01 MHz generating a signal of 10-kHz bandwidth. In

TABLE III
Code Selection for Programmable Transmitter and Receiver

$s_3s_2s_1s_0$	Feed-back	PN Code length
0 0 0 0	No Coding	-
0 0 0 1	[5,2]	32
0 0 1 0	[5,4,3,2]	32
0 0 1 1	[5,4,2,1]	32
0 1 0 0	Reserved	-
0 1 0 1	[6,1]	64
0 1 1 0	[6,5,2,1]	64
0 1 1 1	[6,5,3,2]	64
1 0 0 0	Reserved	-
1 0 0 1	[7,1]	128
1 0 1 0	[7,3]	128
1 0 1 1	[7,3,2,1]	128
1 1 0 0	Reserved	-
1 1 0 1	[8,4,3,2]	256
1 1 1 0	[8,6,5,3]	256
1 1 1 1	[8,6,5,2]	256

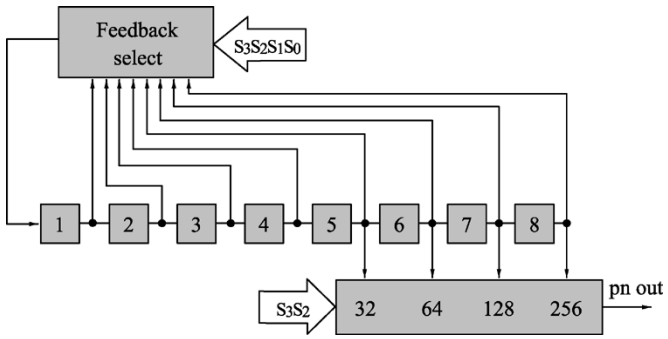

Fig. 3. Structure of the programmable LFSR based PN generator.

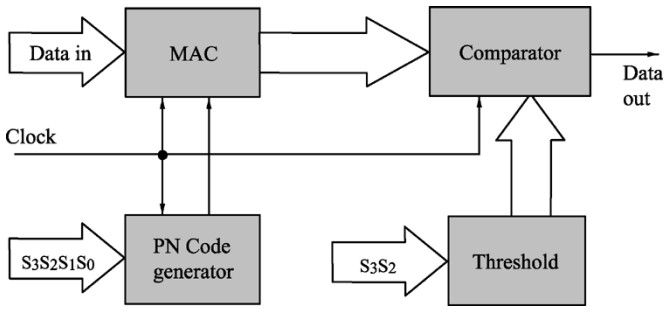

Fig. 4. Block diagram of the DS-SS receiver.

fact, it is impossible to design an antenna at this frequency, which would fit in an ingestible capsule. In order to operate the system in far-field mode, either a much higher transmission frequency or much bigger antenna should have been used. Wireless transmission was done by using an inductor relying on the near-field electromagnetic radiation providing approximately 1-m communication distance with a data rate of 1 kb/s, which appears to be adequate for such an application [9]–[11]. Employing relatively low frequency also prevents the signal to be absorbed by the tissue, as the absorption rate increases by increasing transmission frequency [25]. However, achieving longer ranges at these scales (in terms of the miniaturization) remains a challenge and is mainly related to design of the antenna, which is small enough to fit in ultraminiature systems and is efficient.

B. Receiver Design

Two different receiver designs corresponding to the fixed and programmable PN length transmitters were designed and implemented. In the first design, the PN code length was (127), accumulator size was 16 bits, and input data size was assumed to be 8 bits. In the second design, the PN code length was programmable (length of 32, 64, 128, and 256). The design was implemented by considering different input data sizes (4, 8, and 12 bits) and different accumulator sizes (from 6 to 16). The block diagram of a DS-SS receiver is illustrated in Fig. 4. Assuming perfect synchronization and no channel distortion, the DS-SS receiver is no more complicated than the transmitter except for few extras, namely accumulator and comparator. However, in reality, the incoming signal is no longer a simple digital signal due to distortions caused by many noise sources such as channel distortion, multiple-access distortion, and additive white Gaussian noise. Moreover, the DS-SS-coded signal is modulated with a carrier and transmitted as an analog signal. At the receiver side, the incoming signal must be demodulated and digitized. Therefore, a proper computational circuitry such as multiplier and accumulator (MAC) is employed for implementing the DS-SS receivers. This results in a much more complex digital design. As mentioned before, the DS-SS receiver is based on a correlator, which attempts to match the incoming received signal with each of the candidate prototype waveforms known *a priori* to the receiver. The implementation of a correlator is based on an MAC comprising a dedicated n bit digital multiplier and accumulator.

Although the DS-SS receiver is a complex digital circuit compared to the transmitter [12], a certain degree of simplification can be achieved by exploiting some properties of PN codes. The same programmable PN code generator as in the transmitter is used at the receiver side. In fact, the PN code has only two values: zero or one. This corresponds to $+1$ and -1 in bipolar format. The implication of this is that the multiplication of the DS-SS-coded input data and PN code is no more than that of a sign modification. The multiplier is redundant. As a result, the receiver circuit reduces to a simple adder or subtractor depending on the PN code value. Addition and subtraction use the same circuit when two's complement arithmetic is used. This further simplifies the receiver design.

The comparator is basically a logic circuit comparing the n bit correlator output to a known threshold value. If the correlator output is a positive peak, a Logic 0 is assigned to the comparator output. On the other hand, if the correlator output is a negative peak, a Logic 1 is assigned to the comparator output. Otherwise, nothing is assigned to the output. In fact, this circuit is a window comparator and it allows us to reconstruct the original data. In the programmable design, for each PN code length, an appropriate threshold value is automatically selected. Since it has a direct effect on the DS-SS receiver output, determination of the threshold value is an important issue in the SS systems [26]. Because of the area and power restrictions, a fixed threshold approach was adapted in our implementation.

IV. Implementation Simulations and Results

The transmitters and the receivers were synthesized using Synopsys Design Compiler and Alcatel 0.35 μ technology. In order to test the functionality and do the power analysis of the designed cores, several netlist simulations were performed using Cadence's Verilog-XL simulator for each case. All netlist simulations were also confirmed by MATLAB simulations.

In order to demonstrate the functionality of the designs, a test-bench program written in Verilog was used to simulate the transmitter and receiver systems. First a combination of two different test data (length of 7 bits) coded by two different PN codes (pn1 and pn2, length of 127) and noise, which is illustrated in Fig. 5(a), were transmitted. One of the coded test data was "0 101 010." Autocorrelation of the PN code "pn1" is shown in Fig. 5(b). Fig. 5(c) illustrates the output of the receiver correlator when the first PN code (pn1) is used in the receiver. Well-defined positive or negative peeks imply that a component of the incoming signal and the local PN code are highly correlated. This is because of the autocorrelation property of the PN code. In this case, it is apparent that original data can be recovered quite easily by simple thresholding. Fig. 5(d) illustrates the output of the receiver correlator when a PN code other than "pn1" and "pn2" is used. Here, the output has no definite peak suggesting that there is no correlation between received signal and the PN code. This is because of the cross-correlation property of the PN code.

In order to perform the power analysis for the fixed PN length transmitter and receiver implementations, a real test data recorded from a pH sensor, which was a component of an integrated sensor microsystem [7], was used. The data set included 8-bit 1000 samples. The pH scale is a notation that extends from 0 to 14 with 7 as its middle point. It is a scale that measures hydrogen ion concentration [27]. The DS-SS

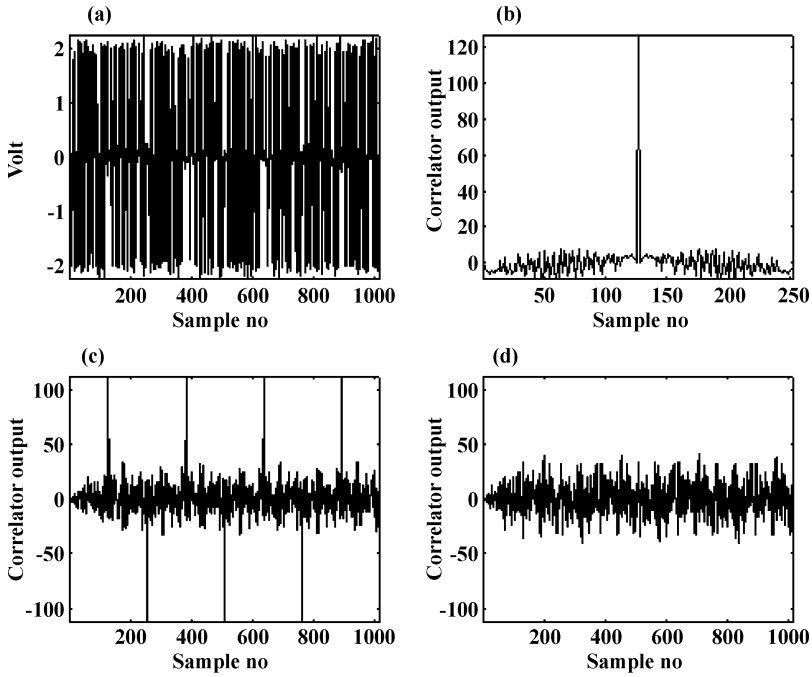

Fig. 5. (a) A SS signal comprising two DS-SS encoded signals and random noise, (b) auto-correlation of a PN code, which was used to encode one of the signals in (a), (c) cross-correlation of the signal given in (a) and the PN code given in (b), and (d) cross-correlation of the signal in (a) and a PN code which was not used in encoding the signals in (a).

transmitter and receiver circuits were designed in Verilog HDL and synthesized using Synopsis Design Compiler. Then the final layout of the circuits were generated using Cadence Silicon Ensemble layout design tool. The switching activity information obtained from the postlayout simulations was fed into Synopsys Design Power, which is a tool for estimating power consumption of the designed cores. Since the data rate in the targeted application is very low (less than 1 kbs/s), a clock frequency of 100 kHz for driving the DS-SS system was assumed. The power supply voltage was assumed to be 3 V. Prior to simulating implemented DS-SS transmitter, the pH sensor data, which was recorded during the test of the first generation of the ingestible capsule by placing it in a test solution with different pH values [10], were digitized by an ADC modeled in Matlab and converted into a bit stream. Because a 10-bit ADC with effective 8-bit resolution having $\pm$1.5-V power supply was used in the actual mixed-signal implementation [9], the ADC resolution was assumed to be 8 bits corresponding to 256 level of quantization, and input dynamic range was assumed to be $\pm$1.5 V. The output of the Matlab program was a serial bit stream ready to be encoded by the DS-SS circuit and transmitted. Encoding and transmission processes were implemented in the Verilog environment by assuming the output of Matlab program as the input. The transmitter output, which was the DS-SS encoded data, was saved in a file. The next step was to model the analog reception part of the receiver in the Matlab environment. This time, the encoded DS-SS data was converted into an analog-transmitted signal, digitized by an 8-bit ADC and saved into a file. This file was used as the input to the DS-SS receiver circuit. The original test data from the pH sensor is illustrated in Fig. 6(a). The reconstructed data at the receiver with 8-bit input resolution is shown in Fig. 6(b). Fig. 6(c) illustrates the difference between the original signal recorded at the output of pH sensor and the reconstructed signal at the DS-SS receiver. This difference is mainly caused by the quantization. The same analysis was also performed for the second design considering an 8-bit data input and 16-bit accumulator sizes. Again a clock frequency of 100 kHz and a power supply voltage of 3 V were used. The power consumption analysis and area estimation results for the designs are presented in Table IV. Although, the area of the transmitter with programmable PN generator is at least twice of the transmitter with fixed length PN generator, a comparable power saving was achieved in the programmable transmitter. However, the power consumption of the programmable transmitter is a function of the PN code length as seen from Table IV (1.8 μW for the PN length of 32, 3.9 μW for 256).

Finally, in order to investigate the effect of input data and internal register sizes on the area and power consumptions of the programmable receiver cores, the designed cores were synthesized and simulated by considering three different data input sizes (4, 8, and 12 bits) and different internal register sizes (from 6 to 16). For this study, a total of 33 synthesis and 132 simulations were performed. Considering the number of synthesis and simulations to perform within a reasonable time, a test data given as "10 101 010" was used. The data was coded by the designed transmitter using each PN length (32, 64, 128, and 256) and transmitted. Then the transmitted (coded) signals were digitized in the Matlab environment as described before. The digitized signals were then used by the receiver considering three input data widths and all the possible internal register widths up to 16 bits as mentioned above. The switching activity informa-

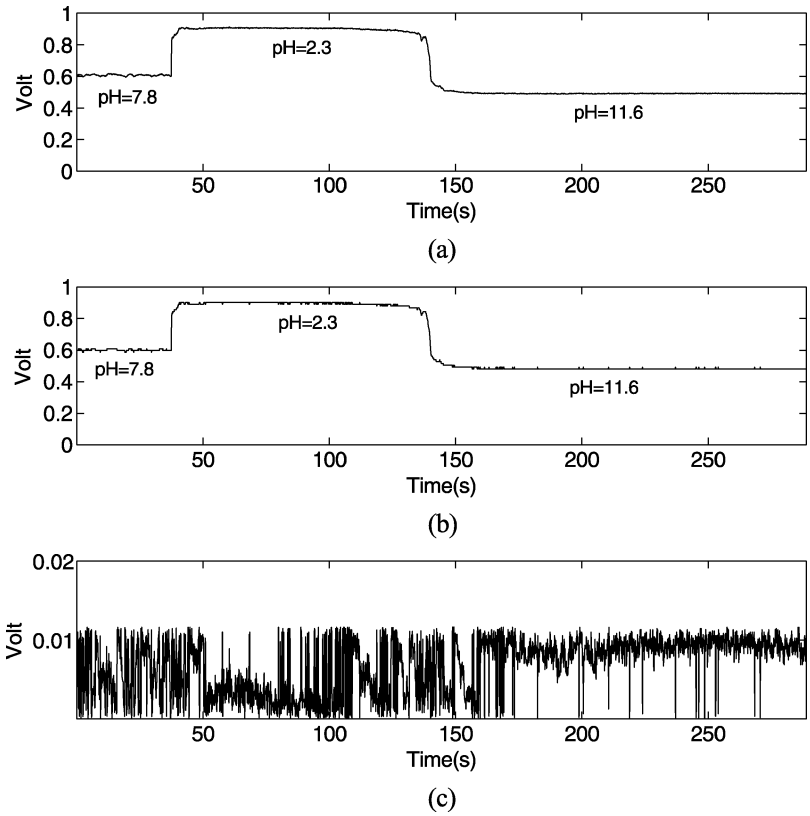

Fig. 6. (a) Normalized original signal from the pH sensor, (b) normalized reconstructed signal at the receiver, and (c) the difference between the original signal and the reconstructed signal.

TABLE IV
POWER AND AREA ESTIMATIONS FOR FIXED AND PROGRAMMABLE DESIGNS

Design	PN Length	Area (ENG)	Power(μW)
Transmitter	127	93	1.6
Transmitter (Prog.)	32	226	1.8
	64	226	2.1
	128	226	2.7
	256	226	3.9
Receiver	127	6520	23.4
Receiver (Prog.)	32	15856	61.2
	64	15856	61.7
	128	15856	66.4
	256	15856	79.8

ENG: Equivalent NAND gate. For the receiver, input data size is 8 bits, accumulator size is 16 bits.

information obtained from the netlist simulations was fed into the Synopsis Design Power and total power consumptions were estimated.

Unlike the receiver, the transmitter implementation is straightforward and not complicated. So the power consumption of the transmitter is quite low compared to the receiver [13]. Assuming the clock frequency is fixed (10 MHz), the transmitter power and area is a function of the PN code length. However, the receiver power and area may greatly be influenced by the choice of input data width and the internal register width of accumulator as well as the PN code length. Therefore, we assumed that the data was digitized by 4-, 8-, and 12-bit ADC in each case. In the first case (4 bits), power consumptions and areas of the receiver were evaluated for internal register widths from 6 to 16 bits, each for four different PN code lengths (32, 64, 128, and 256). In the second case (8 bits), power consumptions and areas of the receiver were evaluated for internal register widths from 9 to 16 bits, each for four different PN code lengths. In the last case (12 bits), power consumptions and areas of the receiver were evaluated for internal register widths from 12 to 16 bits, again each for four different PN code lengths.

V. DISCUSSION

Area and comparative power estimations of the receiver for all the combinations of input data width and internal register widths are illustrated in Fig. 7. Although the receiver core area linearly increases by increasing internal register length, it is mainly a function of input data width [Fig. 7(a)]. The memory block takes most of the space in the correlator. This has an important implication on the applications with area constraints such as described in this paper. Therefore, in area-constrained SoC applications, utilization of unnecessarily higher resolution ADCs for the correlator receiver should be avoided. Fig. 7(b) shows power figures when the input data width is 4 bits. In this case, the minimum internal register length, which will not cause saturation in accumulator, is 6 bits with a PN code length of 32, 7 bits with a PN code length of 64, 8 bits with a PN code length of 128, and 9 bits with a PN code length of 256. Although power consumption increases linearly with increasing register lengths, it is insignificant. Fig. 7(c) and (d) shows the estimation of the powers when the input data width is 8 and 12 bits, respectively. In those cases, internal register sizes less than 9(12) bits for 8(12)-bit input data will cause saturation in the

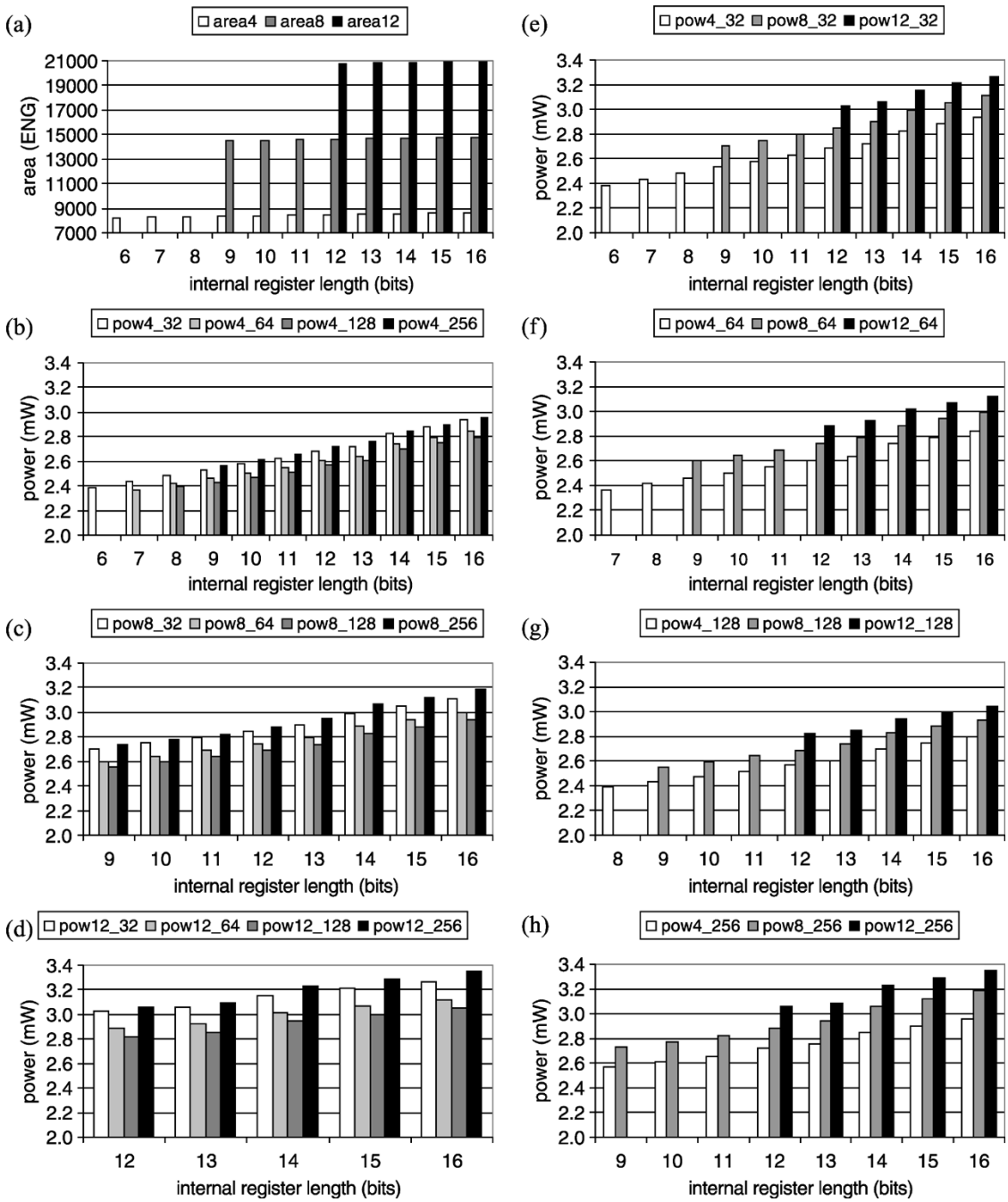

Fig. 7. Area and power estimations of the receiver as a function of input data and internal register width. (*ENG*: equivalent NAND gate, *area*4(8)(12): receiver core area with the input data width of 4(8)(12) bits, *pow*4(8)(12)_32(64)(128)(256): power estimation with the PN code length of 32(64)(128)(256) and the input data width of 4(8)(12) bits).

accumulator. Again power consumptions increase linearly with increasing register lengths. For a safe data reception, the internal register size in the programmable receiver described here should be at least 9 bits when the input data width is 4 and 8 bits, and 12 bits when the input data width is 12 bits. Normally, if a separate circuit had been designed for each code length, the power consumption for smaller codes would have been less than the longer ones, as it requires a lower number of LFSR stages. However, since in this implementation the code length is programmable, all four codes use the same circuit. The number of LFSR stages is the same for all code lengths giving the same static power dissipation. However, major power consumption in a very large scale integration circuit is caused by the switching activities in the complementary metal–oxide–semiconductor (CMOS) device [28], which is also data-dependent. Fig. 7(b), (c), and (d) shows that the code length of 128 is the most optimized in terms of the power consumption. Fig. 7(e), (f), (g), and (h) illustrates comparisons of different input data widths for PN code length of 32, 64, 128, and 256, respectively. From the experimental results presented here, it can be concluded that for very special-

ized implementations requiring the lowest possible power consumption, ideally the design with minimum register size, which do not cause any degradation to the data transmission, should be considered. However if a certain degree of programmability and input data flexibility is required, then the size of the internal register length should be at least 12. This will also assure in practice that the accumulator will not saturate as a result of unexpected input signal fluctuations.

VI. Conclusion

We have designed and implemented a DS-SS-based communication system incorporating a certain degree of programmability to be used in an integrated sensor microsystem, which measures approximately 30 $\times$ 12 mm [8]. Only the DS-SS transmitter was integrated into the sensor microsystem described here and fabricated using Austria Microsytems's 0.6 μ CMOS technology. The fabricated chip has been tested for functionality by recording the output on a digital scope. It was found by comparing recorded results with simulated ones that the transmitter functions as intended. However, estimated power consumption of the fabricated system (approximately 100 μW) [29] was higher than the power consumption estimated during the design process due to the power consumed by peripheral circuits running with the transmitter and the old technology used in fabrication. We have also performed extensive power and area evaluations in order to determine the optimized receiver design. Based on the results presented here, in our application, a considerable amount of area and power (up to 59% and 11%, respectively) can be saved by optimizing the input data width and internal register size. It is expected that the utilization of the observations presented in this paper in the next generation of the integrated sensor microsystem will enable us to integrate the DS-SS receiver and to increase functionality while reducing power consumption and area. The designs reported here require very low power enabling its utilization in advanced communication systems where area and power budgets are severely limited. The described communication system provides a reliable data transmission in a noisy environment by rejecting narrow-band interference. It also provides a simple multiple-access capability. Since the receiver is based on a correlator, the synchronization requirement is also significantly reduced.

Acknowledgment

The authors would like to thank E. Johannessen and T. B. Tang for providing the pH test data.

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