Variability-Aware Noise-Induced Dynamic Instability of Ultra-Low-Voltage SRAM Bitcells

Léopold Van Brandt, Jean-Charles Delvenne and Denis Flandre

ICTEAM Institute, UCLouvain, Louvain-la-Neuve, Belgium

leopold.vanbrandt@uclouvain.be

Abstract—**Stability of ultra-low-voltage SRAM bitcells in retention mode is threatened by two types of uncertainty: process variability and intrinsic noise. While variability dominates the failure probability, noise-induced bit flips in weakened bitcells lead to dynamic instability. We study both effects jointly in a unified SPICE simulation framework. Starting from a synthetic representation of process variations introduced in a previous work, we identify the cases of poor noise immunity that require thorough noise analyses. Relying on a rigorous and systematic methodology, we simulate them in the time domain so as to emulate a true data retention operation. Short times to failure, unacceptable for a practical ultra-low-power memory system application, are recorded. The transient bit-flip mechanism is analysed and a dynamic failure criterion involving the unstable point is established. We conclude that, beyond static variability, the dynamic noise inflates defectiveness among SRAM bitcells. We also discuss the limits of existing analytical formulas from the literature, which rely on a linear near-equilibrium approximation of the SRAM dynamics to, inaccurately, predict the mean time to failure.**

I. Introduction

The need for *ultra-low-power* (ULP) circuits and systems is notably motivated by the massive deployment of connected autonomous IoT nodes [1], translating into *ultra-low voltage* (ULV) design [2]. Processors operating at a *supply voltage* (V_{DD}) lowered below $200\,\text{mV}$ are demonstrated [3]. *Static Random Access Memory* (*SRAM*) arrays are essential blocks of ULP systems [2], typically ranging from a few kB [2], [3] to $32\,\text{kB} = 262\,144$ bits [4]. The functionality of these bitcells must be statistically guaranteed and thereby predicted.

Whereas the smallest MOS transistors offer higher-density SRAM and faster read/write operations, they are also more sensitive to uncertainties like *process variability* and *intrinsic noise*. The robustness of SRAM bitcells against all read-/write/hold failures is a major concern for ULV design [2], [5]. To overcome the limitations of the Six-Transistor (6T) SRAM bitcell (Figure 1), dedicated ULV architectures like the 8T [6], [7] and the 10T [8]–[11] are provided with a read buffer. In this configuration, the hold mode becomes the critical one. For all these bitcells, data *retention* is ensured by a cross-coupled inverter pair (*latch*, dotted box in Figure 1) [10, Fig. 1],
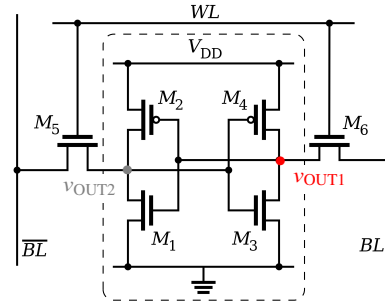
Figure 1. 6T SRAM bitcell. Data retention is ensured by the cross-coupled inverter pair (M_1 and M_2, M_3 and M_4), like in 8T and 10T architectures.

which implements a feedback loop counteracting moderate disturbances.

Observing *transient failures*, i.e. bit flips induced by the intrinsic noise of the transistors, requires computational intensive transient simulations [12]–[14]. Previous work [13], [14] mainly focused on symmetrical latches (neglecting access transistors M_5 and M_6 in Figure 1) operating at extremely low V_{DD}. It highlighted the fact that SRAM bitcells whose noise margin is positive (hence deemed functional at time zero) but small may be *dynamically unstable* [13], [14]. Crucially, short *times to failure* (*TTF*) are observed for the bitcells already severely affected by variability [12], [15]. The rarity of these events makes the brute-force approach coupling Monte-Carlo simulations with transient noise analyses prohibitively expensive. Reference [12] developed an home-made accelerated simulator, yet not straightforwardly compatible with industrial tools. Like in the theoretical work of physicists [16], simplified transistor model and constant capacitances are coarsely assumed. Work [15] attempted to apply Kish [17]'s analytical formula to estimate the mean *TTF* (*MTTF*) but lacks a basis of comparison. In [12], [15]'s studies, variability is only introduced in noise analyses as a global deterministic imbalance between nMOS and pMOS transistors (asymmetrical process corner).

In the present work, we propose to unify the extensive knowledge of SRAM static stability and related concepts [18] with the robust noise simulation methodology of [14], as summarized in Section II, in order to insightfully observe and analyse the combined effects of process variability and intrinsic noise on the functionality of ULV SRAM bitcell in retention mode. In Section III, we explain the bit-flip mech-

(a)

(b)

(X_0, Y_0)

$v_{\mathrm{OUT1}} = v_{\mathrm{IN2}}$ [mV]

$v_{\mathrm{IN1}} = v_{\mathrm{OUT2}}$ [mV]
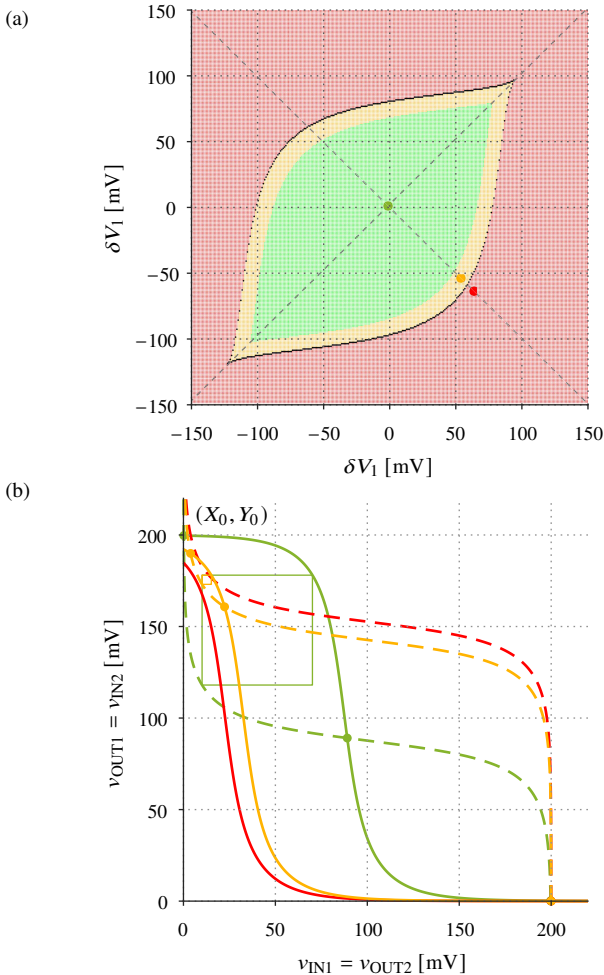
δV_1 [mV]

δV_1 [mV]

Figure 2. (a) 2D representation of functional and defective SRAM bitcells in presence of process variability, deterministically simulated with a double DC sweep of variations $(\delta V_1, \delta V_2)$ applied at the inputs of the inverters (M_1 and M_2, M_3 and M_4 in Figure 1). The orange crown contains the bitcells of positive but low SNM ($\leq 10\,\mathrm{mV}$).
Voltage step of the double DC sweep : $\Delta\delta V = 1\,\mathrm{mV}$.

(b) Butterfly plots of three special cases marked by dots in (a), along the line $\delta V_1 = -\delta V_2$ corresponding to the worse-case scenario where both inverters are adversely affected. For functional bitcells, the SNM is the width of the largest inscribed square.

Illustrated case: 28 nm FD-SOI Single-P-Well (SPW) SRAM cell (inverters made of RVT nMOS and LVT pMOS; RVT nMOS access transistors M_5 and M_6) of minimal transistor dimensions $L_n = L_p = 30\,\mathrm{nm}$ and $W_n = W_p = 80\,\mathrm{nm}$, $V_{\mathrm{PW}} \equiv V_B = 0$, operating at $V_{\mathrm{DD}} = 200\,\mathrm{mV}$ and room temperature ($T = 300\,\mathrm{K}$).

anism and the notion of SRAM dynamic stability within the mathematical framework of nonlinear dynamical systems [19], [20]. Attempts of analytical predictions of the $MTTF$ based on the literature are discussed in Section IV. Section V draws the conclusion and opens perspectives.

II. VARIABILITY-AWARE NOISE SIMULATION SETUP

The voltage limit in ULV circuits is mainly dictated by process variations [2, Fig. 17]. Enhanced Monte Carlo methods [21]–[26] speed up the simulations whose aim is to empirically estimate the SRAM failure probability. The intrinsic noise of the transistors (including the access transistors M_5

and M_6 shown in Figure 1) and of peripheral circuits comes as an additional uncertainty, taking on the design margins. The same goes for the supply-voltage (droop) noise. The V_{DD} referred to as below may therefore be thought as the minimal supply voltage, reduced compared to its nominal value.

In [18], a novel non-Monte-Carlo semi-analytical methodology was introduced the detect the hold failures caused by static variability within ULV SRAM bitcells. It was shown that the dominant effect can be suitably and accurately modelled by two series-voltage sources δV_1 and δV_2, each applied at the input of one inverter of the latch [18, Figure 4]. The noise margin of a CMOS inverter operating in subthreshold is indeed dominantly degraded by the imbalance between nMOS and pMOS transistors [2], [27]. These δV may notably be related to the individual V_{th} shifts and the same goes for their statistics [18]. The double DC sweep of the variations $(\delta V_1, \delta V_2)$ yields the two-dimensional (2D) representation of Figure 2(a). To each $(\delta V_1, \delta V_2)$ point is thoughtfully associated an SRAM bitcell, whose functionality has been assessed with the traditional "butterfly plot" [28] (Figure 2(b)). A tested bitcell is functional (green and orange), at time zero, if the number of cross points is exactly equal to three; defective (red) otherwise. The (positive) *static noise margin* (SNM) of the functional bitcells can be extracted with the SPICE-compliant method from List and Seevinck [28]. The procedure is graphically illustrated for three special cases of variations in Figure 2(b): nominal bitcell ($SNM = 61\,\mathrm{mV}$, comfortably stable), $\delta V_1 = -\delta V_2 = 55\,\mathrm{mV}$ ($SNM = 5\,\mathrm{mV}$, barely functional), $\delta V_1 = -\delta V_2 = 65\,\mathrm{mV}$ (defective).

Whereas any SRAM bitcell exhibiting a non-negative noise margin ($SNM \geq 0$) would be classified as functional based on purely static considerations, we expect those with lowest SNM to have poor noise immunity and to be dynamically *unstable*. Rigorously, the SNM only quantifies the robustness of a bitcell against DC sources of variations, in a particular scenario where both inverters are adversely affected [18] (dashed line $\delta V_1 = -\delta V_2$). The dynamic noise margin, i.e. the robustness of the bitcell against transient noise, is substantially larger than the SNM [13], [14], [29]. The SNM nevertheless remains an indicative metric of the noise immunity and we can identify cells to be treated in priority for noise analysis. In Figure 2(a), we have highlighted in orange the region corresponding to bitcells whose SNM lies between 0 (verge of instability)

We have focused the transient noise analyses on a few limit cases belonging to the worst-case line $\delta V_1 = -\delta V_2$; the case $55\,\mathrm{mV}$ presented earlier in orange in Figure 2(b) is one of them. From statistical considerations involving a two-dimensional Gaussian variability distribution [18], we can show that such selected points lie within a 10 ppm-equiprobability circle [18], i.e. frequently encountered among Monte-Carlo samples or fabricated bitcells. The choice $\delta V_1 = -\delta V_2$ does not affect the generality of the presented methodology and subsequent analyses.

The role of the two cross-coupled inverters of Figure 1 is totally interchangeable. Having adopted the convention $\delta V_1 = -\delta V_2 > 0$, the endangered memory state is $(v_{\mathrm{OUT2}}, v_{\mathrm{OUT1}}) =$
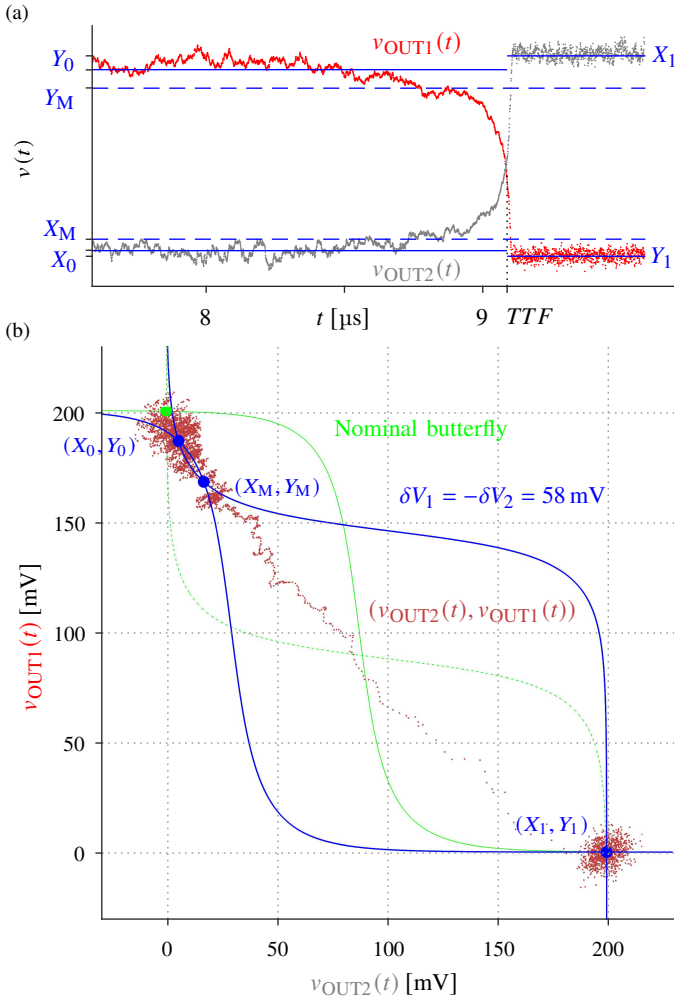
Figure 3. (a) Transient simulation of a noise-induced hold failure of a 6T SRAM bitcell (Figure 1).

(b) State trajectory of the bit flip of (a) in the state space.

Illustrated case: same SRAM design as Figure 2, with process variations $\delta V_1 = -\delta V_2 = 58\,\text{mV}$.

Bandwidth of the generated noise: $f_{\max} = 1\,\text{GHz}$ ($dt = 500\,\text{ps}$).

(X_0, Y_0) (see Figure 2). The exact high and low logic levels X_0 and Y_0 depend on the process variations affecting the particular bitcell (see again Figure 2). For simplicity, we assumed $(v_{\text{OUT2}}(0), v_{\text{OUT1}}(0)) = (0, V_{\text{DD}})$ as the initial condition for all the transient experiments of the retention operation. Careful setting of the transient simulations parameters like the generated noise bandwidth, time step, and duration optimizes the CPU-time tradeoff while ensuring accuracy [13], [14]. Let us mention that we still end up with a huge CPU time of a few hours per single bit-flip experiments and of several days to go through six selected $\delta V_1 = -\delta V_2$ variability cases. This, despite the use of a high-performance work station and parallel multi-core computing.

III. ANALYSIS OF THE BIT-FLIP MECHANISM

One typical transient simulation of a bit-flip caused by intrinsic transistor noise is shown in Figure 3(a). The bit-flip mechanism in SRAM bitcells is better understood within the mathematical formalism of nonlinear dynamical systems [19], [20]. We call *state vectors* the pairs of voltages $(v_{\text{OUT2}}(t), v_{\text{OUT1}}(t))$. The set of all the possible values of those vectors forms the *state space* [19]. The *state trajectory*, obtained by plotting the state vectors at various times in the state space, is depicted in Figure 3(b). The butterfly of the affected SRAM bitcell is also represented in the state space in order to locate the two stable states or points (X_0, Y_0) and (X_1, Y_1), which slightly deviate from the nominal and ideal $(0, V_{\text{DD}})$ and $(V_{\text{DD}}, 0)$ due to process variations δV_1 and δV_2, and to emphasize the out-of-equilibrium behaviour of the system during the transient bit flip. Each stable state may be regarded as an *equilibrium point* to which a *stability region* or *region of attraction* is associated [20]. The *stability boundary*, or *separatrix* [20], which separates the two stability regions, necessarily includes the *unstable* point (X_M, Y_M).

At the beginning of the represented time segment, the two node voltages $v_{\text{OUT2}}(t)$ and $v_{\text{OUT1}}(t)$ (defined in Figure 1) fluctuate quietly around the logic levels X_0 and Y_0, the data initially retained by the SRAM bitcell. Starting from about $8.5\,\mu\text{s}$, $v_{\text{OUT2}}(t)$ gradually increases and $v_{\text{OUT1}}(t)$ decreases due to hazardous and simultaneous large voltage noise fluctuations. This process goes against the deterministic regenerative property of the inverters, which in absence of continuous disturbance would restore the logic levels X_0 and Y_0. Once $v_{\text{OUT2}}(t)$ and $v_{\text{OUT1}}(t)$ have crossed specific thresholds, respectively X_M and Y_M (Figure 3(a)), i.e. $(v_{\text{OUT2}}(t), v_{\text{OUT1}}(t))$ has gone beyond the unstable point (X_M, Y_M) and thereby has crossed the separatrix (Figure 3(b)), the two cross-coupled inverters enter in positive feedback loop. $(v_{\text{OUT2}}(t), v_{\text{OUT1}}(t))$ falls in the region of attraction of the other equilibrium, (X_1, Y_1), the bit flip becomes highly likely and rapid as dictated by the natural dynamics of the SRAM bitcell. We consider the state flip effective and define the TTF when $v_{\text{OUT2}}(t)$ and $v_{\text{OUT1}}(t)$ cross. This TTF is a random variable for a given bitcell, since it takes a different value for each of the 100 experiments carried out.

Although determining the exact shape of the full separatrix is not required in this work, it is important to understand that (X_M, Y_M) is the threshold point. If we assume, after observation of Figure 3 (other trajectories simulated for other cases behaved similarly), that a bit flip occurs according to the preferential direction given by the line connecting the two nearby points (X_0, Y_0) and (X_M, Y_M), *the necessary failure criterion is that $v_{\text{OUT2}}(t)$ and $v_{\text{OUT1}}(t)$ cross the thresholds X_M and Y_M, respectively*. The largest the individual distances $\Delta X \equiv X_M - X_0$ and $\Delta Y \equiv Y_1 - Y_M$, the statistically rarest the bit-flip event (at fixed noise magnitude) and the most robust the SRAM bitcell. The deleterious effect of process variability is to reduce the noise margins (like the SNM) and, similarly, ΔX and ΔY. Those observations, notably the role played by ΔX and ΔY (obtained from the DC butterfly), combined with the cheap extractions of the noise bandwidth f_p and voltage noise standard deviations $\sigma_{v_{\text{OUT2}}}$ and $\sigma_{v_{\text{OUT1}}}$ from AC (spectral) simulation [13], [14], gives hope of analytically predicting the $MTTF$.
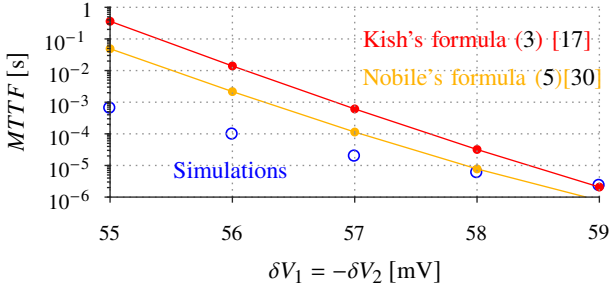
Figure 4. $MTTF$ empirically estimated from transient noise simulations (averaged over 100 experiments like Figure 3(a), for each point) compared to the predictions of the analytical formulas.

IV. RESULTS, PREDICTIONS AND DISCUSSION

From the transient noise simulations described in Section III, we have estimated the $MTTF$ for each selected variability case $\delta V_1 = -\delta V_2 = 55, 56, 57, 58$ or 59 mV. As expected, the SNM of the SRAM bitcells reduces accordingly, from 5 mV to 1 mV. The extracted $MTTF$, obtained by averaging 100 realizations of TTF for each point, are given in blue in Figure 4. As previously observed in [13], [14], the metric spans across orders of magnitude: it drops from about 1 ms at $\delta V_1 = -\delta V_2 = 55$ mV to a only few µs at 59 mV. The low reported $MTTF$ values confirm that, while they were considered functional at time zero ($SNM > 0$), all these bitcells weakened by static variations are prone to dynamic instability and should be classified as defective, whatever the memory system application.

A. Kish's Formula and Similar

Kish proposed a simplified Rice formula for the mean frequency of crossing a given threshold voltage by a Gaussian noise process [17, (8)]. Here, the stochastic process is the unidimensional voltage variable $\tilde{v}(t)$ along the preferential bit-flip direction. The threshold for $\tilde{v}$ is the Euclidean distance between (X_0, Y_0) and (X_M, Y_M):

$$\Delta\tilde{v} = \sqrt{(X_M - X_0)^2 + (Y_0 - Y_M)^2} = \sqrt{\Delta X^2 + \Delta Y^2}. \quad (1)$$

Assuming decorrelation between $v_{OUT2}(t)$ and $v_{OUT1}(t)$ (reasonable since the noises come from different transistors, each within one inverter), one can derive the variance of $\tilde{v}(t)$ from basic geometry and linear algebra:

$$\sigma_{\tilde{v}}^2 = \frac{\Delta X^2}{\Delta\tilde{v}^2} \cdot \sigma_{v_{OUT2}}^2 + \frac{\Delta Y^2}{\Delta\tilde{v}^2} \cdot \sigma_{v_{OUT1}}^2. \quad (2)$$

Kish's formula in integral form [17, (8)] diverges when applied to the power spectral density of the output voltage noise of an inverter (see, for instance, [14, Figure 5]). It is most often used (notably [15, (4)]) in a simplified form [17, (9)] supposing band-limited white (thermal) noise, written with the notations of this paper as:

$$\frac{1}{MTTF} = \frac{2}{\sqrt{3}} \exp\left(-\frac{1}{2}\left(\frac{\Delta\tilde{v}}{\sigma_{\tilde{v}}}\right)^2\right) f_p. \quad (3)$$

Whereas one can hardly find any proof of (3), reference [30] has rigorously formalized the mathematical problem of the *first passage time* of an Ornstein-Uhlenbeck process, defined by the linear scalar differential equation

$$\mathrm{d}\tilde{v}/\mathrm{d}t = -2\pi f_p \cdot \tilde{v}(t) + \eta(t) \quad (4)$$

where the drift term $-2\pi f_p \cdot \tilde{v}(t)$ refers to the regenerative action of the cross-coupled inverters that attract the state toward the stable point (X_0, Y_0), and $\eta(t)$ is the white noise process. Equation (4), which is formally similar to a noisy RC dynamics with time constant $1/2\pi f_p$, linearises around (X_0, Y_0) in the direction towards (X_M, Y_M) the true *nonlinear* dynamics of the SRAM bitcell. The $MTTF$ is then predicted as [30, (6a) multiplied by 2]:

$$MTTF = \frac{1}{\pi f_p}\left(\sqrt{\pi}\int_0^{\Delta\tilde{v}/\sqrt{2}\sigma_{\tilde{v}}} \mathrm{d}u\, \exp\left(u^2\right)\right. \quad (5)$$
$$\left. + \int_0^{\Delta\tilde{v}/\sqrt{2}\sigma_{\tilde{v}}} \mathrm{d}u\, \exp\left(u^2\right)\mathrm{erf}(u)\right).$$

Predictions of (3) and (5) were added in Figure 4, in red and orange respectively.

B. Discussion

As can be noticed in Figure 4, the formulas (3) and (5) predict the same $MTTF(\delta V_1)$ trend and seem to differ by a multiplicative constant between 4 and 7. If Nobile's (5) seems more accurate than Kish's (3), perhaps thanks to the mathematical rigor of [30]'s derivation, the fact remains that the two analytical formulas struggle to correctly predict the $MTTF$ estimated from the reference SPICE transient noise simulations. The analytical predictions are only fairly accurate for the smallest $MTTF$, and the discrepancy increases to more than one order of magnitude for $\delta V_1 = -\delta V_2 = 55$ mV. By extrapolation, we expect the formulas to be completely faulty for even larger $MTTF$ that would be measured in SRAM bitcells with moderate variability conditions.

The origin of the observed inaccuracy can be explained by the assumptions inherent to the model (4) behind (3) and (5). In (4), the deterministic drift coefficient $-2\pi f_p$ is coarsely assumed constant, i.e. independent on the actual instantaneous voltage values. In particular, the model (4) assumes a non-zero drift term $-2\pi f_p \Delta\tilde{v}$ at (X_M, Y_M) while it is exactly zero within the full nonlinear model. When $(v_{OUT2}(t), v_{OUT1}(t))$ becomes close to (X_M, Y_M), Ornstein–Uhlenbeck (4) model therefore severely *overestimates* the recall effect to (X_0, Y_0). This would explain the significant overestimation of the $MTTF$ reported in Figure 4.

V. CONCLUSIONS

ULV SRAM arrays are essential blocks of ULP systems. The data retention is threatened by two random phenomena affecting the MOS transistors and thus the SRAM bitcell functionality: static process variability and dynamic intrinsic noise. Whereas most simulation and modelling efforts have been rightly focused on variability, we have shown that,

because the noise immunity of the bitcells severely degrades with large process variations, dynamic instability comes as a non-negligible additional concern. An efficient variability-aware noise simulation framework, compatible with industrial SPICE tools and compact models, is therefore needed. We have exploited a 2D variability representation, mapping of the situation at time zero, to select cases to be treated in priority for noise analysis. So far, the computation cost remains widely unaffordable to pretend to an exhaustive characterization. Existing analytical formulas should be reworked: we have pointed out their inaccuracy that we attribute to the near-equilibrium approximation, inappropriate to model the nonlinear SRAM dynamics. In addition to accelerated transient noise simulators, we believe that an hybrid semi-analytical methodology combining a limited number of cheap SPICE simulations with closed-form formulas is the promising avenue for future variability- and noise-aware reliability predictions.

Acknowledgement

References

[1] D. Bol, G. de Streel, and D. Flandre, "Can We Connect Trillions of IoT Sensors in a Sustainable Way? A Technology/Circuit Perspective," in *2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*. IEEE, 2015, pp. 1–3.

[2] M. Alioto, "Ultra-Low Power VLSI Circuit Design Demystified and Explained: A Tutorial," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 1, pp. 3–29, 2012.

[3] A. P. Chandrakasan, D. C. Daly, D. F. Finchelstein, J. Kwong, Y. K. Ramadass, M. E. Sinangil, V. Sze, and N. Verma, "Technologies for Ultradynamic Voltage Scaling," *Proceedings of the IEEE*, vol. 98, no. 2, pp. 191–214, 2010.

[4] D. Bol, M. Schramme, L. Moreau, P. Xu, R. Dekimpe, R. Saeidi, T. Haine, C. Frenkel, and D. Flandre, "SleepRunner: A 28-nm FDSOI ULP Cortex-M0 MCU With ULL SRAM and UFBR PVT Compensation for 2.6-3.6-μW/DMIPS 40-80-MHz Active Mode and 131-nW/kB Fully Retentive Deep-Sleep Mode," *IEEE Journal of Solid-State Circuits*, 2021.

[5] D. Bol, R. Ambroise, D. Flandre, and J.-D. Legat, "Interests and Limitations of Technology Scaling for Subthreshold Logic," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 10, pp. 1508–1519, 2009.

[6] L. Chang, D. M. Fried, J. Hergenrother, J. W. Sleight, R. H. Dennard, R. K. Montoye, L. Sekaric, S. J. McNab, A. W. Topol, C. D. Adams *et al.*, "Stable SRAM Cell Design for the 32 nm Node and Beyond," in *Digest of Technical Papers. 2005 Symp. on VLSI Technology, 2005.* IEEE, 2005, pp. 128–129.

[7] N. Zheng and P. Mazumder, "Modeling and Mitigation of Static Noise Margin Variation in Subthreshold SRAM Cells," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 10, pp. 2726–2736, 2017.

[8] T.-H. Kim, J. Liu, J. Keane, and C. H. Kim, "A High-Density Subthreshold SRAM with Data-Independent Bitline Leakage and Virtual Ground Replica Scheme," in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers.* IEEE, 2007, pp. 330–606.

[9] B. H. Calhoun and A. P. Chandrakasan, "A 256-kb 65-nm Sub-threshold SRAM Design for Ultra-Low-Voltage Operation," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 3, pp. 680–688, 2007.

[10] J. P. Kulkarni, K. Kim, and K. Roy, "A 160 mV Robust Schmitt Trigger Based Subthreshold SRAM," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, 2007.

[11] I. J. Chang, J.-J. Kim, S. P. Park, and K. Roy, "A 32 kb 10T Sub-Threshold SRAM Array With Bit-Interleaving and Differential Read Scheme in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 2, pp. 650–658, 2009.

[12] E. Rezaei, M. Donato, W. R. Patterson, A. Zaslavsky, and R. I. Bahar, "Fundamental Thermal Limits on Data Retention in Low-Voltage CMOS Latches and SRAM," *IEEE Transactions on Device and Materials Reliability*, vol. 20, no. 3, pp. 488–497, 2020.

[13] L. Van Brandt, F. Silveira, J.-C. Delvenne, and D. Flandre, "On Noise-Induced Transient Bit Flips in Subthreshold SRAM," in *9th EUROSOI-ULIS, Tarragona, Spain*, 2023.

[14] ——, "On Noise-Induced Transient Bit Flips in Subthreshold SRAM," *Solid-State Electronics*, vol. 208, p. 108715, 2023.

[15] F. Veirano, F. Silveira, and L. Naviner, "Minimum Operating Voltage Due to Intrinsic Noise in Subthreshold Digital Logic in Nanoscale CMOS," *Journal of Low Power Electronics*, vol. 12, no. 1, pp. 74–81, 2016.

[16] N. Freitas, K. Proesmans, and M. Esposito, "Reliability and entropy production in nonequilibrium electronic memories," *Physical Review E*, vol. 105, no. 3, p. 034107, 2022.

[17] L. B. Kish, "End of moore's law: thermal (noise) death of integration in micro and nano electronics," *Physics Letters A*, vol. 305, no. 3-4, pp. 144–149, 2002.

[18] L. Van Brandt, R. Saeidi, D. Bol, and D. Flandre, "Accurate and Insightful Closed-Form Prediction of Subthreshold SRAM Hold Failure Rate," *IEEE Transactions on Circuits and Systems I: Regular Papers*, pp. 1–14, 2022.

[19] B. Zhang, A. Arapostathis, S. Nassif, and M. Orshansky, "Analytical Modeling of SRAM Dynamic Stability," in *Proceedings of the 2006 IEEE/ACM international conference on Computer-aided design*, 2006, pp. 315–322.

[20] W. Dong, P. Li, and G. M. Huang, "SRAM Dynamic Stability: Theory, Variability and Analysis," in *2008 IEEE/ACM International Conference on Computer-Aided Design*. IEEE, 2008, pp. 378–385.

[21] T. Haine, J. Segers, D. Flandre, and D. Bol, "Gradient Importance Sampling: an Efficient Statistical Extraction Methodology of High-Sigma SRAM Dynamic Characteristics," in *2018 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE, 2018, pp. 195–200.

[22] M. Wang, C. Yan, X. Li, D. Zhou, and X. Zeng, "High-Dimensional and Multiple-Failure-Region Importance Sampling for SRAM Yield Analysis," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 3, pp. 806–819, 2017.

[23] D. D. Weller, M. Hefenbrock, M. S. Golanbari, M. Beigl, J. Aghassi-Hagmann, and M. B. Tahoori, "Bayesian Optimized Mixture Importance Sampling for High-Sigma Failure Rate Estimation," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 39, no. 10, pp. 2772–2783, 2019.

[24] X. Shi, H. Yan, J. Wang, J. Zhang, L. Shi, and L. He, "An Efficient Adaptive Importance Sampling Method for SRAM and Analog Yield Analysis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 39, no. 12, pp. 4999–5010, 2020.

[25] M. Wang, W. Lv, F. Yang, C. Yan, W. Cai, D. Zhou, and X. Zeng, "Efficient Yield Optimization for Analog and SRAM Circuits via Gaussian Process Regression and Adaptive Yield Estimation," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 37, no. 10, pp. 1929–1942, 2018.

[26] D. D. Weller, M. Hefenbrock, M. Beigl, and M. B. Tahoori, "Fast and Efficient High-Sigma Yield Analysis and Optimization using Kernel Density Estimation on a Bayesian Optimized Failure Rate Model," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2021.

[27] M. Alioto, "Understanding DC Behavior of Subthreshold CMOS Logic Through Closed-Form Analysis," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 7, pp. 1597–1607, 2010.

[28] E. Seevinck, F. J. List, and J. Lohstroh, "Static-Noise Margin Analysis of MOS SRAM Cells," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 5, pp. 748–754, 1987.

[29] J. Lohstroh, "Static and Dynamic Noise Margins of Logic Circuits," *IEEE Journal of Solid-State Circuits*, vol. 14, no. 3, pp. 591–598, 1979.

[30] A. Nobile, L. Ricciardi, and L. Sacerdote, "Exponential trends of ornstein–uhlenbeck first-passage-time densities," *Journal of Applied Probability*, vol. 22, no. 2, pp. 360–369, 1985.