Improved RF Devices for Future Adaptive Wireless Systems Using Two-Sided Contacting and AlN Cooling

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***Abstract*—This paper reviews special RF/microwave silicon device implementations in a process that allows two-sided contacting of the devices: the back-wafer contacted Silicon-On-Glass (SOG) Substrate-Transfer Technology (STT) developed at DIMES. In this technology, metal transmission lines can be placed on the low-loss glass substrate, while the resistive/capacitive parasitics of the silicon devices can be minimized by a direct two-sided contacting. Focus is placed here on the improved device performance that can be achieved. In particular, high-quality SOG varactors have been developed and an overview is given of a number of innovative highly-linear circuit configurations that have successfully made use of the special device properties. A high flexibility in device design is achieved by two-sided contacting because it eliminates the need for buried layers. This aspect has enabled the implementation of varactors with special $N_d x^{-2}$ doping profiles and a straightforward integration of complementary bipolar devices. For the latter, the integration of AlN heatspreaders has been essential for achieving effective circuit cooling. Moreover, the use of Schottky collector contacts is highlighted also with respect to the potential benefits for the speed of SiGe heterojunction bipolar transistors (HBTs).**

***Index Terms*—Adaptive circuits, aluminum nitride deposition, bipolar junction transistors (BJTs), complementary bipolar silicon technology, heatspreaders, heterojunction bipolar transistors (HBTs), microwave devices, radio frequency (RF) circuits, Schottky collector contacting, selfheating, silicon-on-glass technology, substrate transfer, thermal instability, thermal resistance, thin-film heatspreaders, two-sided contacting, varactors, wireless systems.**

I. Introduction

IT HAS long been recognized that the conventional conductive silicon substrate is highly unsuitable for RF applications. The solutions that have found their way to production are mainly combinations of high-resistivity Si and silicon-on-insulator (SOI) substrates [1], [2]. In particular, RF SOI CMOS is challenging the frequency territory of BiCMOS processes. The advantage of these types of processes is that they are a "small" modification of mainstream Si technology. A more aggressive approach is to entirely remove the silicon under the critical circuit regions. This can be achieved by local micromachining of the Si substrate [3] or by Substrate-Transfer Technology (STT) [4]–[6]. Besides the elimination of the lossy Si, another advantage of the actual removal of the Si up to the device regions can be the possibility of direct device contacting from the back of the wafer (the back-wafer). Such two-sided contacting has been achieved in the back-wafer contacted Silicon-On-Glass (SOG) technology being run at DIMES. This technology is an almost natural extension of RF SOI technology, which, instead of restricting the device architecture as in pure SOI processes, frees the device designer of the complications associated with making plugs and buried contacts.

In this paper, we review the devices already developed in back-wafer contacted SOG technology and comment on the potentials of technologies that allow two-sided contacting. In this STT, an almost fully-processed SOI circuit-wafer is transferred to glass by a gluing process and the bulk silicon is removed with the buried oxide (BOX) as etch-stop. In the original Philips version of this STT process, the active device was a novel lateral SOI NPN that used the BOX isolation layer to achieve a very low collector-base capacitance C_{BC} [4]. The transfer to glass also reduced the NPN substrate parasitics, but the main goal was to eliminate the Si under large passive elements. This process was developed in the beginning of the 1990s and was transferred to Philips Hamburg where it was industrialized [5]. At DIMES, the SOG process itself was developed further by adding full wafer-stepper patterning of the back of the wafer with process modules for near-ideal diode and low-ohmic contact fabrication. The first Si device focus was also on NPN fabrication for the reduction of C_{BC}: a bulk-Si vertical 25 GHz NPN was transferred to glass and the collector contacts were made directly under the emitter, thus minimizing C_{BC} and collector series resistance R_C [7]. Further developments included Schottky collector contacting, which, besides potential benefits for high-frequency operation, also simplifies the device structure even further. Both vertical NPNs and PNPs with Schottky collector contacts were fabricated in a complementary process, which is illustrative of how any simplification of the device architecture also facilitates the task of combining different device types in one process [8].

Manuscript received January 09, 2009; revised April 08, 2009. Current version published August 26, 2009. This work has been supported in part by NXP/Philips Semiconductors Cluster and PACD projects. The circuit work is now also being continued in the context of the SmartMix MEMPHIS and SenterNovem projects, and process module development is being performed in cooperation with the STW TFN program and the FP6 D-DOTFET project.

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Digital Object Identifier 10.1109/JSSC.2009.2023016

Although these bipolar device designs were successfully fabricated, circuit realizations were hampered by an extremely high thermal resistance of the transistors themselves. This was a direct consequence of the almost perfect electrical dielectric-isolation of the devices that, for the conventional dielectrics in Si technology, also implies (unfortunately) a very good thermal isolation. The thermal resistance of the devices can be extremely large: in some cases about 100 times larger than the comparable bulk-Si devices. The electrothermal investigation of these devices has been scientifically very rewarding and has led to new insights in the electrothermal behavior of bipolar transistors [9], [10]. However, for reliable integrated-circuit realizations, it is obviously imperative to have an effective thermal management of the devices. This has led to the development of deposited AlN layers as thin-film heatspreaders. We have with success integrated them on a device level and shown that they can bring the thermal resistance of the individual devices and the electrothermal behavior of small circuits into a domain that is suitable for reliable circuit fabrication [11].

Parallel with the bipolar SOG research, the development of a varactor IC technology was also undertaken. Unlike the bipolar circuits, the targeted circuit applications in the field of RF adaptivity did not have electrothermal issues, and, as a consequence, this process has reached a high level of maturity. In general, for RF/microwave varactors the research focus over the last years has been directed towards revolutionary microelectromechanical systems (MEMS) implementations [12]–[16] or new material integration, such as Barium Strontium Titanate (BST) [17], [18], but both options still suffer from performance problems. In general, RF MEMS solutions raise reliability and packaging questions that are seriously hampering their introduction in production. In contrast, with our more evolutionary SOG varactor technology, it has been possible to immediately demonstrate superior circuit performance. Consequently, a number of record-breaking varactor-diode circuits have already been published and patented [19]–[27].

Besides very high quality factors (Q), the SOG varactor circuits have excelled with respect to linearity. In particular, special $N_d x^{-2}$ doping profiles, where N_d is the maximum doping concentration and x the depth, have been developed and implemented in novel low-distortion circuit configurations. For the preservation of these profiles during processing, the subsequent thermal budget must be low. This is not an issue in the SOG process since no buried contacts are needed. In a bulk realization, not only the thermal budget but also the series resistance to the buried contacts represents a problem: low RC parasitics can only be achieved by using finger-like structures that have the drawback of seriously complicating the control of the doping profile that determines the varactor's C-V characteristic. With back-wafer contacting, the metal contact can be placed directly next to the capacitor and, in this manner, the ideal intrinsic 1-D device performance is approached. To emphasize this great advantage of the two-sided contacting, a comparison in terms of RC parasitics to a few other, more typical, isolation strategies is given in the simplistic schematics of Fig. 1 and the associated Table I. The extremely low parasitics in the SOG version

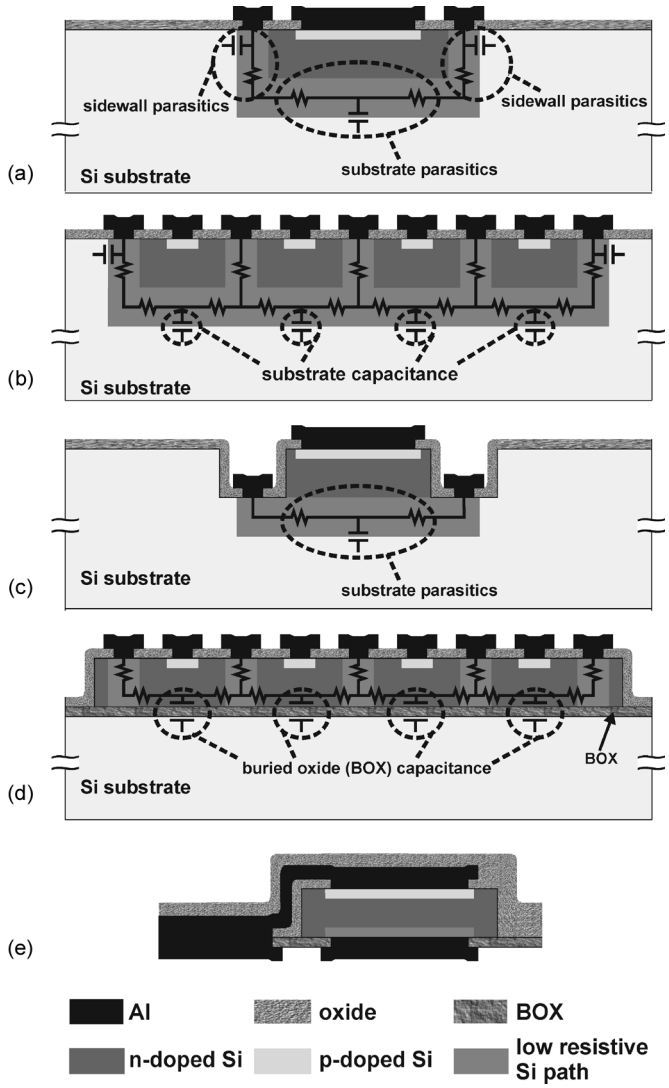

Fig. 1. Comparison of different isolation schemes for a diode processed as (a) a single-finger, (b) multi-finger or (c) trench-isolated device on bulk Si with buried layer, (d) a multi-finger device in SOI, and (e) a two-side contacted device as fabricated in SOG technology.

has meant that circuit concepts can be realized that are much simpler and more potent than otherwise feasible. For example, several very low-distortion varactor configurations for RF adaptivity have been realized and these are reviewed in relationship to the design strategies.

In the last section, we focused on the potentials of the SOG process. This includes comments on the advantages and disadvantages of using a more conservative micromachining approach to two-sided contacting.

II. High-Performance Varactors

A. Ultra-Low Distortion Varactor Configurations

Next-generation wireless systems, such as multi-mode transceivers and "cognitive radios", require circuit techniques that facilitate RF adaptivity. An ideal tuning element for these applications will exhibit extremely low loss, low dc power consumption, high linearity, ruggedness to high voltage and high

current, wide tuning range, high reliability, very low cost, low area usage, and continuous tunability with a high tuning speed. To meet these stringent requirements, different varactor diode-based circuit topologies—along with a dedicated high-performance SOG varactor process technology—have been developed and implemented. These proposed varactor configurations can act as variable capacitors between their RF terminals with ideally zero, or extremely low distortion. A brief description of these low-distortion varactor configurations is given below.

- The distortion-free varactor stack [20], [21] is based on an anti-series connection of two identical uniformly doped diodes as shown in Fig. 2(a). A capacitance power law coefficient of $n = 0.5$ [28] is applied along with an infinitely high impedance as center-tap connection. Under these conditions, all distortion components at the RF terminals are perfectly canceled, yielding a distortion-free operation.
- The high tuning range varactor stack [21] is a combined anti-series/anti-parallel topology of four hyperabrupt varactor diodes [28] as shown in Fig. 2(b). A capacitance power law coefficient $n > 0.5$ is applied along with two infinitely high center-tap impedances. At the RF terminals, the resulting even and third-order distortion products are canceled through a proper selection of the varactor area ratio X [see Fig. 2(b)].
- The narrow tone-spacing varactor stack [21]–[23] is based on an anti-series connection of two $N_d x^{-2}$ doped diodes as shown in Fig. 2(c). Note that this special doping profile results in exponential $C(V_R)$ behavior under reverse bias V_R. To cancel the third-order intermodulation distortion (IM_3), there must be a *low impedance* path (relative to the AC impedance of the varactor capacitance itself) between the center node (V_R) and the two RF terminals at low frequencies. At the same time, the high-frequency components (fundamental and higher harmonics) at the center tap node should experience a high impedance, i.e., $Z_c(s)$ should be much larger than the AC impedance of the varactor diode itself at these frequencies. When these conditions are met, the IM_3 will be cancelled and the remaining distortion is dominated by the much smaller fifth-order nonlinearity.
- The wide tone-spacing varactor stack [23] is a combined anti-series/anti-parallel topology of four $N_d x^{-2}$ doped diodes as shown in Fig. 2(d), which use an infinitely high impedance as center-tap connection. It can be regarded as a special case of the high tuning range varactor stack when the capacitance power law coefficient, n, approaches infinity, with the corresponding varactor area ratio of $2 \pm \sqrt{3}$. It shares the same doping profile as the narrow tone-spacing varactor stack and therefore both configurations (wide- and narrow-tone-spacing varactor stacks) can be implemented on the same wafer while offering complementary linearity properties in terms of tone spacing.

The different varactor configurations treated above, all provide a (center-tap) voltage-controlled tunable capacitance, which behaves linearly between the RF terminals provided that the appropriate combination of varactor doping profile, area ratio and center-tap termination is implemented. The differences between various varactor configurations are listed in Table II, which summarizes the topology, $C(V_R)$ relation, doping profile, harmonic conditions, area ratio for IM_3 cancellation and the resulting linearity at IM_3 frequencies for different tone-spacing regimes.

Note that the varactor configurations that feature infinitely high center-tap impedance(s) provide the best linearity for signals that have a relatively large frequency spacing (several hundred kilohertz). This property makes these configurations most suited for (adaptive) receiver applications where cross modulation of the "weak" desired signals by strong out-of-band interferers should be avoided. In (adaptive) transmitting systems, however, the in-band linearity will be the biggest concern. For these applications the narrow tone-spacing varactor stack [22] is recommended, since it provides the highest linearity for in-band signals (up to ten's of MHz's). Moreover, the fact that this latter configuration makes use of a base-band "short" (typically an inductor) connection to the varactor stack center-tap facilitates rapid modulation of its tunable capacitance, something that is beneficial for future RF applications like dynamic load-line power amplifiers or modulators.

It must be mentioned that the varactor configurations that make use of an "infinitely" high center-tap impedance can be linked to each other by considering the required area ratio for IM_3 cancellation. For example, for the high tuning-range varactor stack [21] with the corresponding doping profile $N_d x^{(1/n)-2}$, the appropriate area ratio for IM_3 cancellation is

$$X = \frac{4n + 1 + \sqrt{12n^2 - 3}}{2(n+1)}. \tag{1}$$

When setting the capacitance power law coefficient n to 0.5, the resulting X will be unity and therefore the two anti-series branches will be identical, which means that, in practice, the high tuning range varactor stack can be reduced to the distortion-free varactor stack configuration [21] [Fig. 2(b) simplifies to Fig. 2(a)]. On the other hand, when $n = \infty$, the corresponding doping profile and area ratio for IM_3 cancellation will be $N_d x^{-2}$ and $X = 2 + \sqrt{3}$, which is identical to the configuration of wide tone-spacing varactor stacks [23] as specified in Table II [Fig. 2(d) same as Fig. 2(b)]. From this perspective, both the distortion-free varactor stack and wide tone-spacing varactor stack can be regarded as special cases of the high tuning range varactor stack, which implies that these two topologies preserve all the merits of the high tuning range varactor stack. Closer inspection, however, shows that the distortion-free varactor stack has the unique property that it is basically free of all distortion in the high tone-spacing regime. In comparison, the high tuning range varactor stack and the wide-tone spacing varactor stack are limited by IM_5 products with respect to linearity. When considering the tuning range, the uniform doping of distortion-free varactor stacks has a relatively fixed relationship between the tuning range and control voltage, which is not the case for the other configurations due to the free-to-choose grading coefficient (a_2 or n of $C(V_R)$, see Table II). This flexibility in grading facilitates easy adjustment of the tuning range and control voltage range for a given application.

As far as integration is concerned, the wide tone-spacing varactor stack can be easily integrated with the narrow tone-spacing varactor stack since they can share the same doping profile.

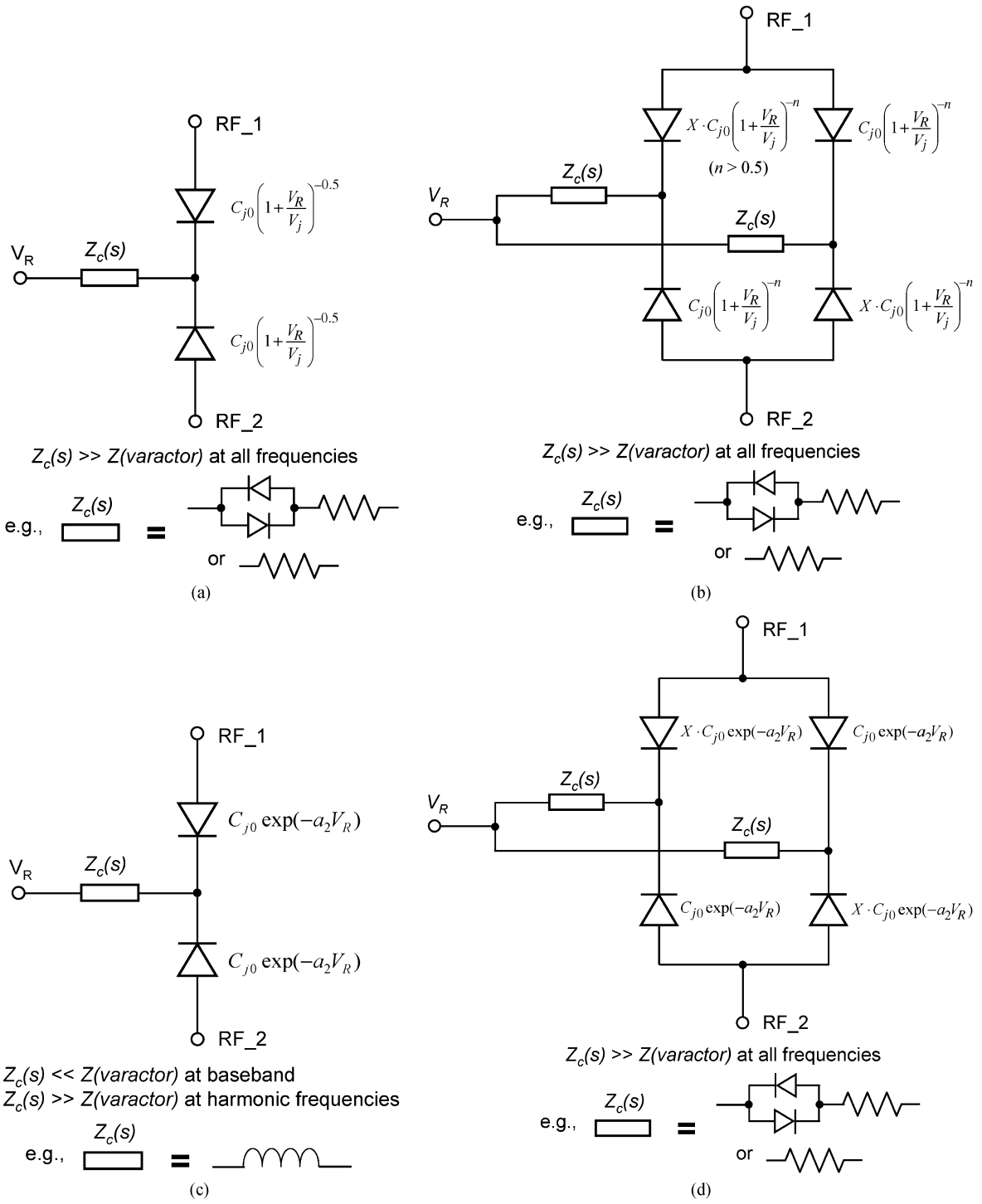

Fig. 2. (a) Configuration of the distortion-free varactor stack. (b) Configuration of high tuning range varactor stack. (c) Configuration of the narrow tone-spacing varactor stack. (d) Configuration of the wide tone-spacing varactor stack. Note that $Z(varactor)$ represents the AC impedance of the capacitance offered by a single varactor in the stack.

Therefore the different linearity requirements of transmit and receive chains can be addressed in one single technology [23].

B. High-Performance Varactor Diode Implementation

1) Doping Profile and Quality Factor Optimization: In order to achieve the capacitance power law coefficient of 0.5 for the distortion-free varactor stack, a uniform doping profile is required as shown Fig. 3(a). This doping concentration needs to be chosen carefully since this sets the quality factor and device breakdown. When the desired tuning range ($T_{tune} = C_{max}/C_{min}$ where C_{max} and C_{min} are the maximum and minimum capacitance values, respectively) is known, together with the material parameters, like maximum electric field ($E_{breakdown}$), dielectric constant (ε_s), mobility (μ_n) and

TABLE I
COMPARISON OF THE PARASITIC RESISTANCE R AND CAPACITANCE C FOR DIFFERENT ISOLATION SCHEMES AS ILLUSTRATED IN FIG. 1. THE $C = C_{sw} + C_{sub}$, WHERE C_{sw} AND C_{sub} ARE SIDEWALL AND SUBSTRATE COMPONENTS, RESPECTIVELY

Device type	R	C_{sw}	C_{sub}	Comments
(a) bulk	$R_{bulk} = R^{sw}_{bulk} + R^{sub}_{bulk}$	C^{sw}_{bulk}	C^{sub}_{bulk}	÷ doping-profile degraded by high-temperature processing
(b) multi-finger bulk	$R_{multi} < R_{bulk}$	$C^{sw}_{multi} \approx C^{sw}_{bulk}$	$C^{sub}_{multi} > C^{sub}_{bulk}$	+ n fingers: R ∝ 1/n, ÷ large diode perimeter ⇒ poor doping-profile control
(c) trench-isolated	$R_{trench} \approx R^{sub}_{bulk} < R_{bulk}$	0	$C^{sub}_{trench} \approx C^{sub}_{bulk}$	+ no high-temperature plug processing
(d) multi-finger SOI	$R_{SOI} > R_{multi}$	0	C_{OX}	÷ no low-resistive path to region beneath the diode, ÷ poor doping-profile control
(e) 2-side contacted	0	0	0	+ lossy substrate eliminated + 1-D diode, + good doping-profile control

TABLE II
OVERVIEW OF NARROW TONE-SPACING VARACTOR STACK, WIDE TONE-SPACING VARACTOR STACK, DISTORTION-FREE VARACTOR STACK AND HIGH TUNING RANGE VARACTOR STACK

	Topology	$C(V_R)$ Relation	Doping Profile	Center-Tap Impedance [$Z_c(S)$ in Fig.2]	Area Ratio (X) for IM_3 Cancellation	*Linearity* at $2f_1$-f_2 *and* $2f_2$-f_1
distortion-free varactor stack	anti-series [Fig. 2 (a)]	$C_{j0}\left(1+\frac{V_R}{V_j}\right)^{-0.5}$	$N_{uniform}$ constant	infinity for all frequencies	1:1	for large Δf free of distortion
high tuning range varactor stack	anti-series/ anti-parallel [Fig. 2 (b)]	$C_{j0}\left(1+\frac{V_R}{V_j}\right)^{-n}$ $(n>0.5)$	$N_d x^{\frac{1}{n}-2}$ $(n>0.5)$ hyper-abrupt	infinity for all frequencies	$\frac{4n+1+\sqrt{12n^2-3}}{2(n+1)}$	for large Δf IM_3 cancelled $IP_5 = 2.72(V_R+V_j)$ $(n=1, X=2)$
narrow tone-spacing varactor stack	anti-series [Fig. 2 (c)]	$C_{j0}\exp(-a_2 V_R)$	$N_d x^{-2}$	zero at low frequency; infinity at other frequencies	1:1	for small Δf IM_3 cancelled $IP_5 = \frac{3.52}{a_2}$
wide tone-spacing varactor stack	anti-series/ anti-parallel [Fig. 2 (d)]	$C_{j0}\exp(-a_2 V_R)$	$N_d x^{-2}$	infinity for all frequencies	$2\pm\sqrt{3}$	for large Δf IM_3 cancelled $IP_5 = \frac{2.75}{a_2}$

Symbols: C_{j0} is the capacitance at zero bias; Δf is the frequency difference or tone spacing of two-tone input RF signals and IP_5 is the fifth-order interception point at $2f_1 - f_2$ and $2f_2 - f_1$ (Note that IM_3 is cancelled while a much smaller IM_5 remains).

built-in potential (V_j), the best choice for the doping concentration $(N_{uniform})$ can be selected using

$$N_{uniform} = \frac{\varepsilon_s E^2_{breakdown}}{2eV_j\,(T^2_{tune}-1)} \tag{2}$$

where e is the electron charge.

With this selection, the related highest theoretically achievable quality factor for the varactor at zero bias operation is defined as

$$Q_{uniform}|_{V_R=0} = \frac{\mu_n E^2_{breakdown}}{2\omega V_j\,(T^2_{tune}-1)\,(T_{tune}-1)} \tag{3}$$

where ω is the angular RF frequency.

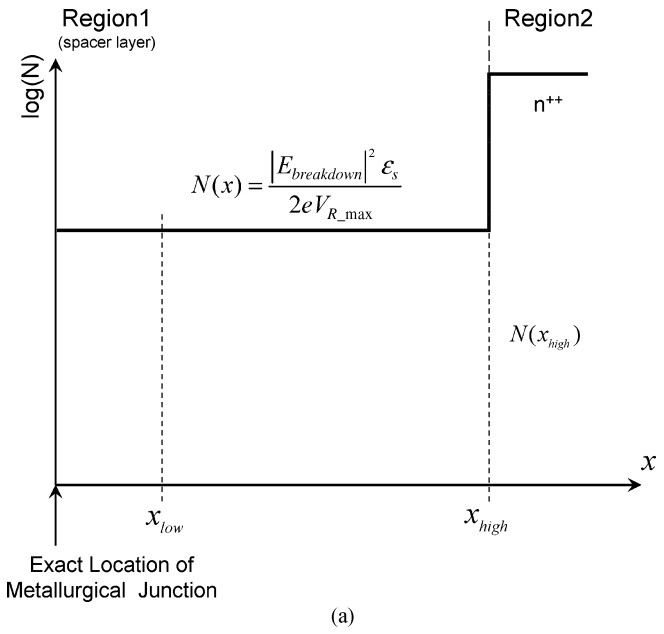

Fig. 3. (a) Optimized doping profile of the uniform doped diode for the distortion-free varactor stack. (b) Optimized doping profile for the narrow tone-spacing varactor stack and wide tone-spacing varactor stack to achieve the exponential $C(V_R)$ relation.

For the narrow tone-spacing varactor stack and wide tone-spacing varactor stack, the required $N_d x^{-2}$ doping profile, which provides the exponential $C(V_R)$ relationship, is shown in Fig. 3(b). Since we cannot implement infinitely high or extremely low doping concentrations, the $N_d x^{-2}$ relationship is restricted between x_{low} and x_{high}, which automatically defines the useful capacitance tuning range. To maintain the "exponential" $C(V_R)$ relation and avoid reduced breakdown voltage and quality factor, a lowly doped spacer layer [Region 1 in Fig. 3(b)] is required. In contrast to the uniformly doped case, here for a free-to-choose combination of tuning range

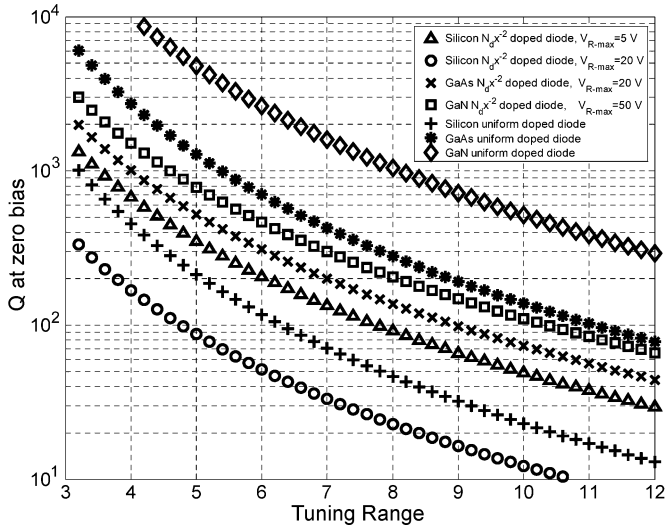

Fig. 4. The maximum achievable quality factors at zero bias for the uniform doped diode and $N_d x^{-2}$ doped diode with different technology implementations. (For silicon, $\mu_n = 1000\ \mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$, $E_{breakdown} = 6 \times 10^5$ V/cm; for GaAs, $\mu_n = 6000\ \mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$, $E_{breakdown} = 6 \times 10^5$ V/cm; for GaN, $\mu_n = 900\ \mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$, $E_{breakdown} = 3 \times 10^6$ V/cm).

and maximum reverse applied voltage (V_{R_max}), the quality factor can be optimized by dimensioning the doping profile. The resulting doping profile and maximum achievable quality factors at zero bias for these structures can be written as [24]

$$N(x) = \frac{\varepsilon_s V_{R\_\max}}{e \ln(T_{tune})} x^{-2} \tag{4}$$

$$Q|_{V_R=0} = \frac{3\mu_n \ln(T_{tune})}{\omega V_{R\_\max}(T_{tune}^3 - 1)} \left(\frac{T_{tune} E_{breakdown}}{T_{tune} - 1} \right)^2. \tag{5}$$

The resulting maximum achievable quality factors at zero bias are plotted as a function of T_{tune} in Fig. 4 for different technology implementations. Due to the fact that the optimized quality factor is proportional to μ_n and to the square of $E_{breakdown}$, the quality factor of these devices can be improved through the use of high-mobility or wide-bandgap materials; e.g., in GaAs an enhancement factor of 6–8 is feasible since $\mu_n = 6000\,\mathrm{cm}^2(\mathrm{V}\cdot\mathrm{s})$ and $E_{breakdown} = 6\times10^5$ V/cm [28], and in GaN even a factor of 25 is possible with $\mu_n = 900\,\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$ and $E_{breakdown} = 3 \times 10^6$ V/cm [29]. Also multi-stacking of the low-distortion varactor configurations can be considered to achieve a higher RF-voltage handling while still maintaining a high quality factor [20].

2) SOG Varactor Implementations: In the SOG varactor process the varactor diode itself is a very straightforward "one-dimensional" structure, for which the advantages of the two-sided contacting are over-evident. Using this feature, the intrinsic varactor can be directly contacted by thick metal interconnects on both sides as shown in Fig. 5. This eliminates the need for finger structures as typically used in conventional varactor implementations to lower the influence of the buried layer series resistance. The remaining losses of the metal interconnects can be significantly reduced through the use of plated copper, facilitating very high quality factors. Substrate losses are eliminated by the perfect isolating properties of the

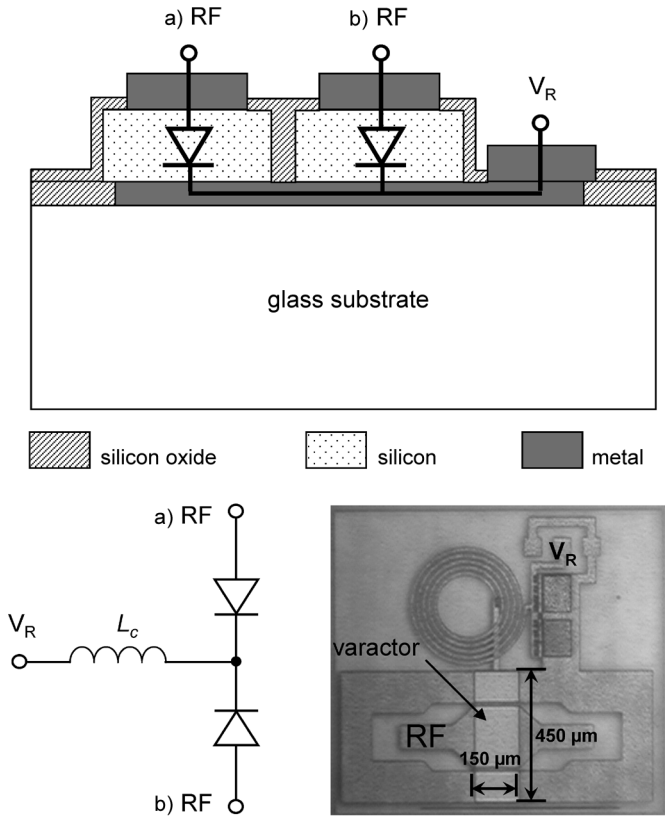

Fig. 5. Cross section, equivalent schematic, and layout of a 33 pF varactor stack implemented in SOG technology with metal interconnects on both sides.

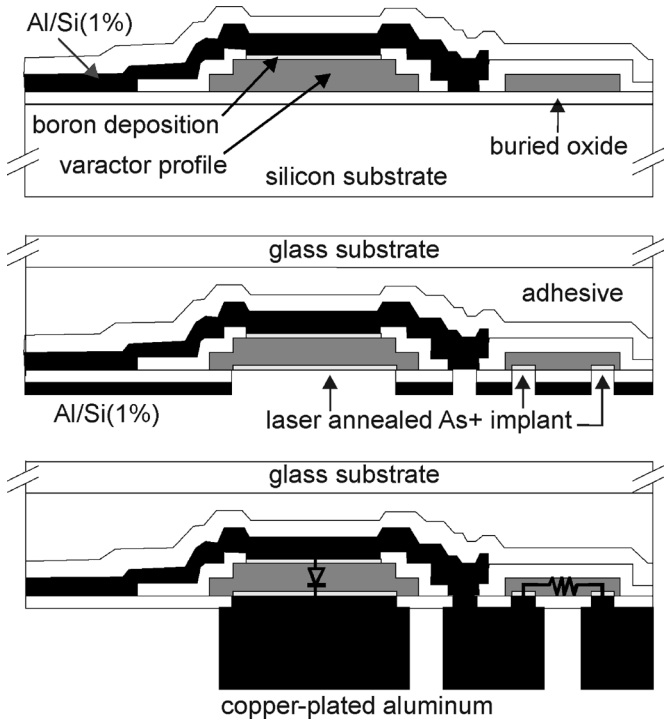

Fig. 6. Schematic of process flow for the integration of SOG varactor diodes and high-ohmic resistors.

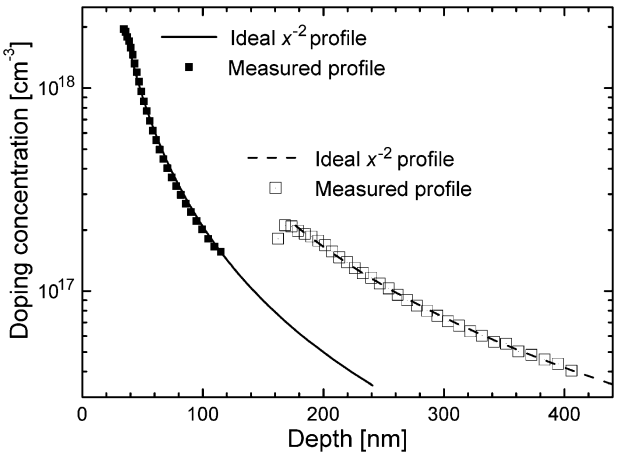

Fig. 7. Two examples of the experimental $N_d x^{-2}$ doping profiles (high- and low-voltage) as extracted from $C - V_R$ measurements and compared to the theoretically desired profile.

glass carrier, while due to low dielectric constant of glass also the influence of parasitic shunt capacitances are reduced.

The basics of the actual SOG process flow are illustrated in Fig. 6. Our starting material is 100 mm SOI SOITEC wafers on which any extra Si layers needed for the specific device fabrication are grown epitaxially. The varactor profiles are tailored to the application by arsenic doping-profile engineering during the epitaxy. The total n-epi thickness depends on the breakdown voltage that is required. Examples of the realized "high-voltage" and "low-voltage" $N_d x^{-2}$ doping profiles are shown in Fig. 7.

After epitaxy, the diode and resistor Si-islands are defined by plasma etching of shallow-trench steps to the BOX. The varactor diode p^+ terminal contact windows are processed and contacted by Al/Si(1%) metal tracks after which the metallization stack in which other passives are formed is processed. The wafer is covered with 1 μm PECVD oxide to enable the gluing of the wafer to a glass wafer. To preserve the integrity of the adhesive, all subsequent thermal processing temperatures must not exceed 300 °C. After gluing, the Si substrate is removed by etching selectively to the BOX. An Al layer is sputtered on the back-wafer to serve as a reflective mask for laser annealing and the back-wafer contact windows are then etched through the Al and BOX. The contacts are implanted with 5 keV As^+ and excimer laser annealed for dopant activation. In this manner it is possible to create low-ohmic contacts and near-ideal diodes essentially at "room-temperature" [30], [31]. This is because the laser pulse only melts the top few nm of the Si surface while the heat pulse that thereby is sent into the bulk is so short, in the μs range at most, that the underlying layers are unaffected. This step provides the low-ohmic contact to the back of the diodes as well as contacts to the resistors. Next, the contact windows to the front-wafer metal are etched and Al/Si(1%) is sputtered and patterned on the back-wafer. Electroplating of 4-μm-thick copper on the Al is then performed to achieve low metal resistance.

3) Experimental Results: Using the ability to adjust the $C - V_R$ relationship by the doping profile, to achieve the desired capacitance control range and related control voltage, the needs of various practical applications can be addressed. Consequently,

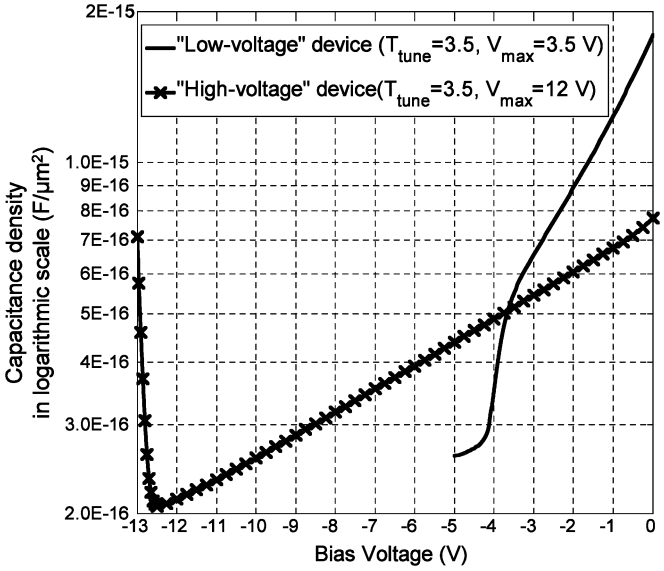

Fig. 8. Measured $C - V_R$ relations for "low-voltage" phase shifter and "high-voltage" matching network implementations. These results demonstrate that $C - V_R$ dependency realized in the SOG technology can be adjusted to the requirements of the application.

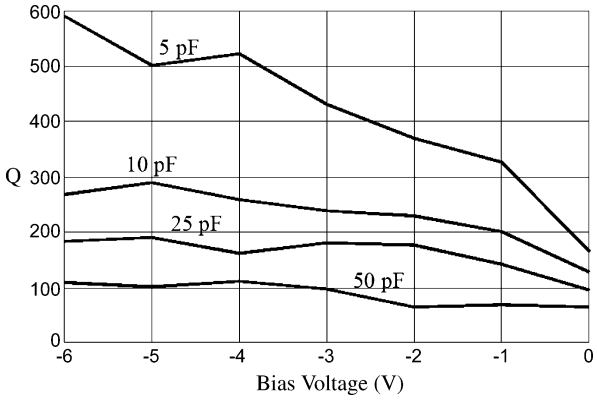

Fig. 9. The measured non-deembedded Q is plotted versus center-tap control voltage at 2 GHz for a copper-plated SOG distortion-free varactor-stack with zero-biased capacitances of 5, 10, 25, and 50 pF. This measurement result shows that very large Q can be obtained also for large varactors [20].

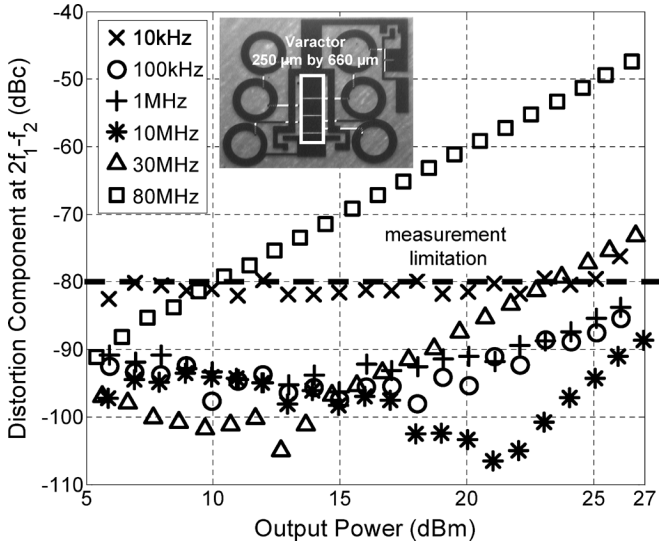

Fig. 10. Multi-stacked narrow-tone spacing varactor configuration with measured two-tone IM_3 ($f_{\rm center} = 2$ GHz) linearity as function of output power [21]. Note that, below the linearity level of -80 dBc, it is difficult to separate the nonlinearities resulting from the varactors from that of the measurement setup, and therefore a conservative boundary of trust is marked as "measurement limitation".

TABLE III
LINEARITY COMPARISON OF CURRENTLY AVAILABLE TUNABLE ELEMENTS

Technology	Input Third-order Intercept Point (dBm)
MEMS Switch	66-80 [33]
MEMS Varactor*	44 [34]
PIN diode*	27-45 [33]
FETs*	27-45 [33]
Ferroelectric based varactor*	50 [35]
This work*	> 67 [21]

* continuously tunable elements

"low-voltage" [23] and "high voltage devices" [23] have been implemented as shown in Fig. 8.

Using the SOG varactor technology, ultra-low distortion tunable capacitive devices have been fabricated, which show record-high Q values ($Q > 200$ @ 2 GHz for large capacitance values [21]), as shown in Fig. 9. As can be seen, high Q can be obtained also for the very large capacitance values due to the back-wafer contacting and copper-plating.

Multi-stacking yielded a record high linearity for a continuously tunable capacitive device [22] with an output third-order interception point $(OIP_3) > 67$ dBm, as illustrated in Fig. 10. It is noteworthy that the IM_3 level of the devices below a tone-spacing of 30 MHz basically cannot be measured since it requires an even higher dynamic range than offered by the dedicated test bench [32]. Conservatively speaking, the measured OIP_3 is larger than 67 dBm up to 10 MHz bandwidth, which is the highest value ever reported for a continuously tunable capacitive device and which is comparable to that of MEMS switched devices (see the comparison in Table III [33]–[35]).

C. Adaptive RF Circuits Using Varactor-Based Adaptive Circuits

In modern telecommunication systems there is a great need for technologies and circuits that enable adaptive RF functionality. Note that such a flexible RF functionality is desired to handle the ever increasing number of wireless services with a limited number of RF transceiver hardware line-ups. Desired functions include tunable filters, matching networks, and phase shifters. Common requirements to these networks are that they should be low loss and do not introduce any signal distortion. Consequently, the SOG technology in combination with low-distortion varactor configurations is an interesting candidate to fulfill these needs. This is endorsed by a number of varactor-

based circuit demonstrators fabricated over the last years, examples of which are given below.

In [24], an adaptive multi-band, multi-mode power amplifier is presented, that can change continuously in operating frequency, while offering load-line adjustment to enhance the efficiency of the output stage when operating in output power back-off. The tunable varactor-based matching networks used in this demonstrator as shown in Fig. 11(a) exhibit third-order interception point (IIP_3) better than +42 dBm, while able to tune the loading condition from 0.2 to 82 Ω. The amplifier demonstrator including these tunable matching networks provides 13 dB gain at 27–28 dBm output power and covers the 900, 1800, 1900, and 2100 MHz bands. In addition, the amplifier provides improved efficiency in power back-off by load line adjustment.

An example of a tunable bandpass filter based on the low-distortion varactor concepts in SOG technology is given in Fig. 11(b) [24]. The fabricated transmit-reject filter can be tuned from 2.4 to 3.5 GHz with a passband loss of 2–3 dB, a stopband rejection of 25 dB and an IIP_3 of +46 dBm.

Note that the linearity and voltage handling of all these circuits can be further improved by stacking multiple varactors in series at the expense of increased area usage [25], doing so, IIP_3 values above +60 dBm have been demonstrated. In addition to the obvious need in wireless applications for adaptive matching networks and tunable filters, the growing popularity of phase diversity systems also yields an increased interest in phase shifters. In these later systems the phase of each individual antenna element is controlled to steer the radiation pattern of the antenna without any mechanical movement. As a result, lower power is required in transmit mode, while signal degradation due to fading in receive mode can be significantly reduced. Depending on the specifications of the phase diversity systems, controllable RF true-time delays are favored over alternative solutions. To investigate the abilities of the SOG varactor concepts for these applications, true time delay phase-shifter prototype has been developed [26] as shown in Fig. 11(c). This phase shifter implementation offers a controllable delay of 110 ps at 1 GHz, with measured IIP_3 better than +45 dBm. The minimum controllable phase-shift at 1 GHz per dB loss is 150 degrees worst case, a value that is comparable to that of state-of-the-art MEMS based phase shifters [27], [36].

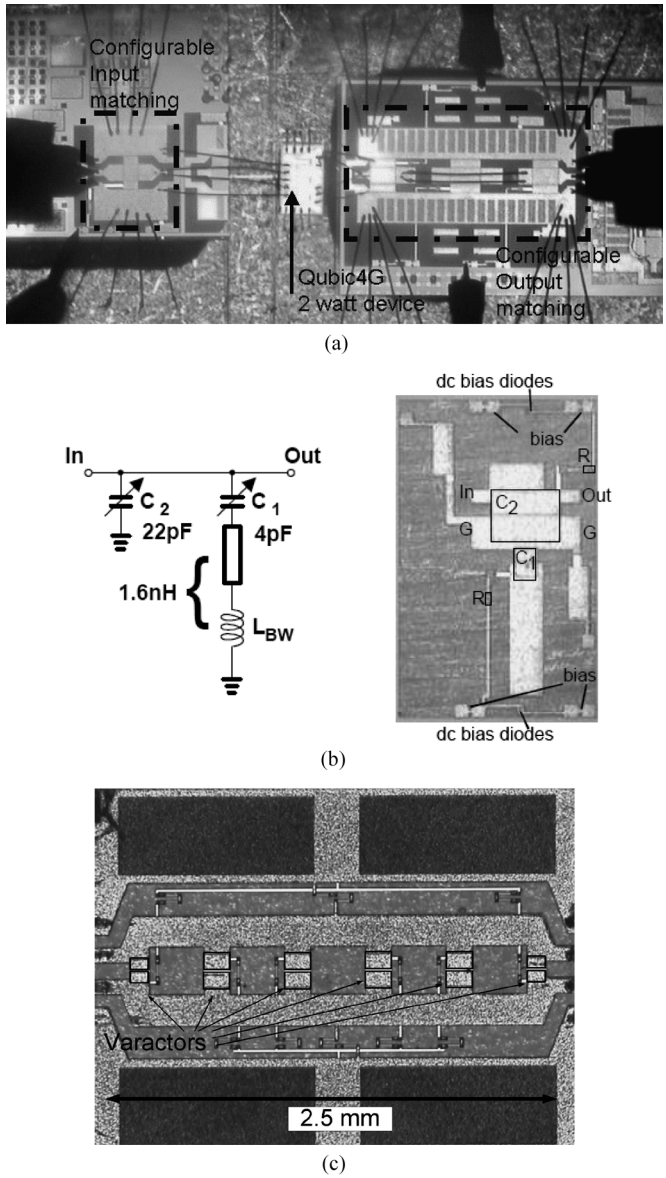

Fig. 11. Chip photographs of adaptive RF circuits making use of low-loss high-linearity varactors. (a) Multi-mode multi-band power amplifier with reconfigurable input and output matching network in SOG technology [24]. (b) Schematic and microphotograph of the bandpass tunable filter in SOG technology [25]. (c) Microphotograph of the copper-plated highly linear differential phase-shifter realized in SOG technology [27].

III. Complementary Bipolar Transistor Integration

At present there is an increasing interest in complementary high-frequency SiGe heterojunction-bipolar-transistor (HBT) BiCMOS processes and a few bulk integration schemes have recently been presented [37], [38]. As always in complementary bipolar processes, the speed of the PNP device is limited by the collector contacting via the bulk. The benefit in this respect of the two-sided contacting has been demonstrated in our low-complexity SOG complementary bipolar process.

A. Schottky Collector Contacting

In DIMES SOG bipolar process, the collector is contacted directly under the emitter and several new collector designs have been explored. Instead of the conventional contacting of a lightly-doped collector via a highly-doped region, Schottky collector contacting can be implemented [7]. This is illustrated in Fig. 12 for the case of Schottky contacting of p-type bipolar transistors. In one case, the lightly-doped p-type collector is retained and contacted by an Al to p-Si Schottky diode. In the other case, the Al metallization is placed directly on the n-type base. The characteristics of these Schottky collector devices were almost identical to the ohmic collector contact devices except for the offset voltage, which becomes very high (even above 0.3 V) for Schottky contacting directly to the base, as shown in Fig. 13. This is determined by the reverse base current, which strongly increases due to the low Schottky barrier height of the contact [39].

Besides their process simplicity, the Schottky contacts also have another advantage because the bipolar devices with im-

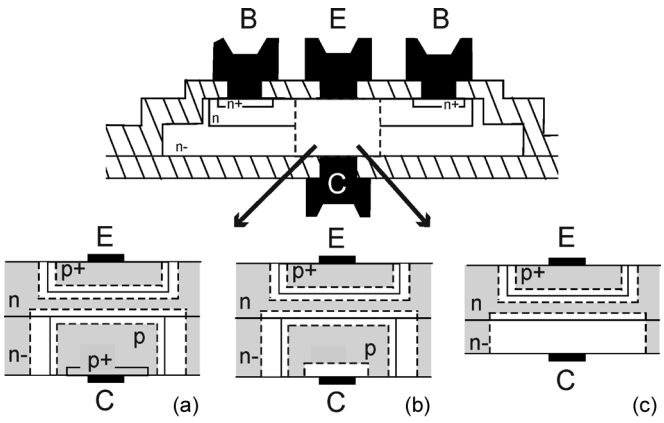

Fig. 12. Schematic of different SOG p-type BJT collector contacts: (a) implanted/laser-annealed ohmic, (b) p-Schottky, and (c) n-Schottky collector contacts.

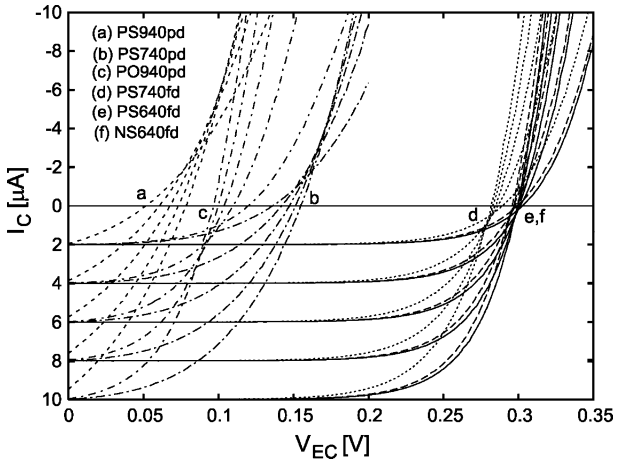

Fig. 13. Measured output characteristics around the offset voltage (at $I_C = 0$) for several p-type BJTs with different collector designs. The high offset devices (d, e, f) have a Schottky contact placed either directly on the base or very close to the base. $I_B = 2, 4, 6, 8$, and 10 μA, emitter area 40×1 μm^2 [8].

planted collector contacts suffer from the effects of the residual implantation damage [40]. Depending on the distance to the implant and the type of implant, we observed enhanced junction leakage, increased impact ionization current, and reduced breakdown voltages. These effects were not very pronounced in our devices because we have a process with relaxed dimensions, but, in a downscaled advanced process, the placing of the implanted collector close to the metallurgic collector-base junction may be destructive. This concern is completely taken away by replacing the ohmic contacts with Schottky contacts.

IV. AlN Thin-Film Heatspreaders

For many SOG devices, heatspreading and heatsinking structures become indispensable at even very low power dissipation levels [10]. For large area devices, thick Cu-plating and direct surface-mounting to a printed-circuit board can provide the necessary heatsinking [41]. In fact, replacing bulk-Si by Cu can be advantageous for reducing the thermal resistance R_{TH}. However, for circuits of small dimension devices such as high-frequency bipolar transistors, heat transport away from the

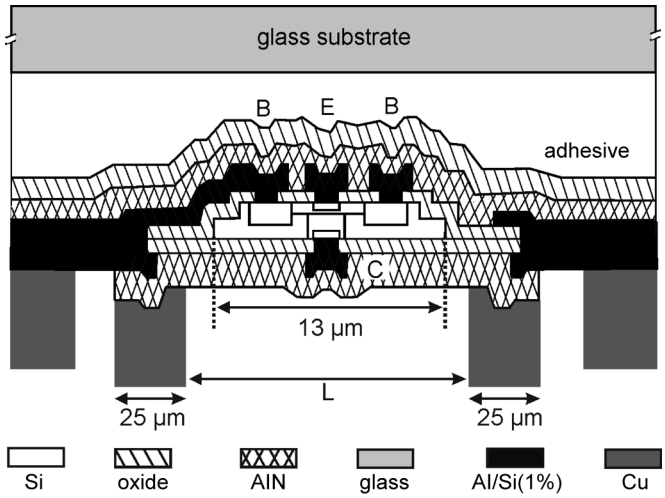

Fig. 14. Schematic of a 20×1 μm^2 emitter SOG NPN cooled by AlN and Cu. A 0.8-μm-thick AlN on both front- and back-wafer reduces the thermal resistance from 12600 K/W to 7550 K/W and additional Cu-plating brings it down to 3600 K/W.

active device area must preferably be accomplished by a thermally conductive dielectric. For this purpose, we have developed physical-vapor-deposition (PVD) of AlN to form thin-film heatspreaders directly on the SOG devices as shown in Fig. 14 [11].

A. AlN Properties

When considering the integration of dielectric heatspreaders, AlN is an obvious choice. It has a large energy bandgap that makes it suitable as an insulator in many situations and a high bulk thermal conductivity of about 270 Wm^{-1}K^{-1} at room temperature [42]. Moreover, it is compatible with standard silicon technology: it is neither contaminating nor poisonous, and can be both deposited and etched by conventional silicon processing techniques.

The integration of thick heatspreading layers in the front-wafer processing is attractive because they can be deposited just before the gluing procedure and do not require any patterning. Thus, they can in principle be chosen as thick as possible. A limitation on the layer thickness is, however, imposed by the stress since the flatness and integrity of the back-wafer surface after gluing and bulk silicon removal is very sensitive to any stress in the remaining layers. Using a low-stress deposition technique, AlN layers of up to 4 μm in thickness were successfully integrated. On the back-wafer it is possible to deposit even thicker layers, but, due to mainly unfavorable etch selectivities, the processing of windows through the AlN to the bondpads entails a trade-off between layer thickness and process complexity.

The electrical properties of the AlN layers were found to be suitable both from a DC and RF point of view. The resistivity is of the order of 10^{13} Ωcm and the dielectric constant falls in the range of 9–11.5. The behavior of AlN at microwave frequencies has been studied by fabricating Al coplanar waveguides on surface-passivated high-resistivity Si wafers. In Fig. 15 the measured losses up to 30 GHz are shown for different configurations of AlN and/or SiO_2. The results show that the presence of AlN does not introduce additional losses at high frequency, but,

TABLE IV
THERMAL RESISTANCES OF NPNS WITH DIFFERENT COMBINATIONS OF AlN AND Cu HEATSPREADERS AS APPLIED IN FIG. 14

BJT	AlN front [μm]	AlN back [μm]	L [μm]	R_{TH} [K/W]
1	0	0	no Cu	12600
2	0.8	0	no Cu	8800
3	0.8	0.8	no Cu	7550
4	0.8	0.8	0	3600
5	0.8	0.8	18	5600
6	0.8	0.8	24	6500
7	0.8	0.8	34	6530

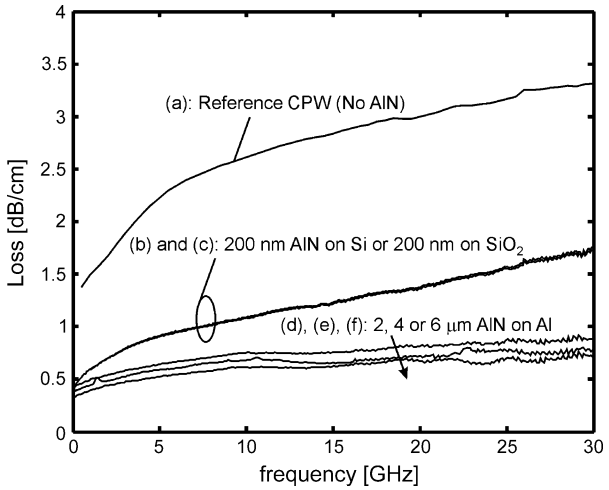

Fig. 15. Measured microwave losses for five different CPWs: (a) CPW on 330 nm SiO_2; (b) CPW on 200 nm AlN deposited directly on the silicon substrate; (c) CPW on 200 nm AlN deposited on 30 nm SiO_2; (d) 2 μm AlN, (e) 4 μm AlN, and (f) 6 μm AlN deposited on a CPW as in (a) [11].

on the contrary, depositing AlN reduces the losses. In addition to the conductive properties of the AlN, also the piezoelectric behavior has been examined; crystal morphologies of AlN are known to have strong piezoelectric properties, the presence of which would be undesirable in an RF circuit environment. For a wide range of layer thicknesses, the piezoelectric response of our AlN films was found to be negligible [11].

B. AlN Cooling of BJT Circuits

The efficiency of AlN as heatspreader can be seen from the experiment illustrated in Fig. 14, where relatively thin 0.8 μm layers are applied to an NPN and also copper-plated blocks are added at different distances from the active device area. In Table IV, the R_{TH} of the NPN is given as a function of the AlN position and of the distance between two Cu blocks. Each layer of AlN contributes to a strong reduction of R_{TH}, and, even at 17 μm from the center of the active device region, a significant measure of heatsinking by the Cu blocks is achieved.

The thermal conductivity of the AlN thin-films is much lower than the bulk value. It has been estimated here by comparing experimental results to simulations. For the latter, measurement of devices with a wide range of R_{TH} has been used as a basis to establish reliable thermal [43], [44] and electrothermal [9], [45]–[47] tools. A quite consistent agreement with the experimental results could be achieved by assuming an isotropic AlN thermal conductivity in the range of 20–50 $\mathrm{Wm^{-1}K^{-1}}$ [44]. For a higher accuracy, a more detailed description of the AlN coverage of the device surface topography as well as of the microscopic material properties is needed.

TABLE V
THERMAL RESISTANCES EXPERIMENTALLY DETERMINED FOR NPNS WITH DIFFERENT AlN LAYERS DEPOSITED ON THE FRONT-WAFER

BJT	AlN thickness [μm]	R_{TH} [K/W]
1	0	19000
2	0.8	9000
3	2	7300
4	4	5250

Both experimentally and in the simulations, the AlN induced reduction of R_{TH} is found to be very significant: a reduction of more than 70% in the value of thermal resistance is obtained by using a 4-μm-thick AlN layer on the front-wafer. A series of experimentally determined thermal resistance values are given in Table V and employed in the electrothermal simulations shown in Fig. 16(a). The thicker the AlN layer, the further the onset of thermal instability is pushed to higher dissipation powers. This strongly benefits the safe-operating-area of the transistors as shown in Fig. 16(b).

An important function of heatspreaders is to keep critical devices in a circuit at the same temperature. When several transistors in a circuit are operated in parallel, the circuit can suffer from electrothermal instabilities that lead to current hogging by the one transistor while the others switch off [47], [48]. A typical situation is shown in Fig. 17 for an NPN pair where the circuit without AlN cooling is already instable at very low current levels. The addition of a 4-μm-thick AlN layer shifts the values of R_{TH} and the thermal coupling coefficient, R_M, from 17800 and 2200 K/W to 5000 and 1000 K/W, respectively. Accordingly, the onset of thermal instability is shifted to much higher power dissipation values and the increase in operation temperature of the two transistors is much lower and stays closer together over a much wider current range. For example, for a total current of $I_{CTOT} = 5$ mA through the two transistors, the difference in operating temperature is more than 130 K without AlN and only a few K with the 4-μm-thick layer.

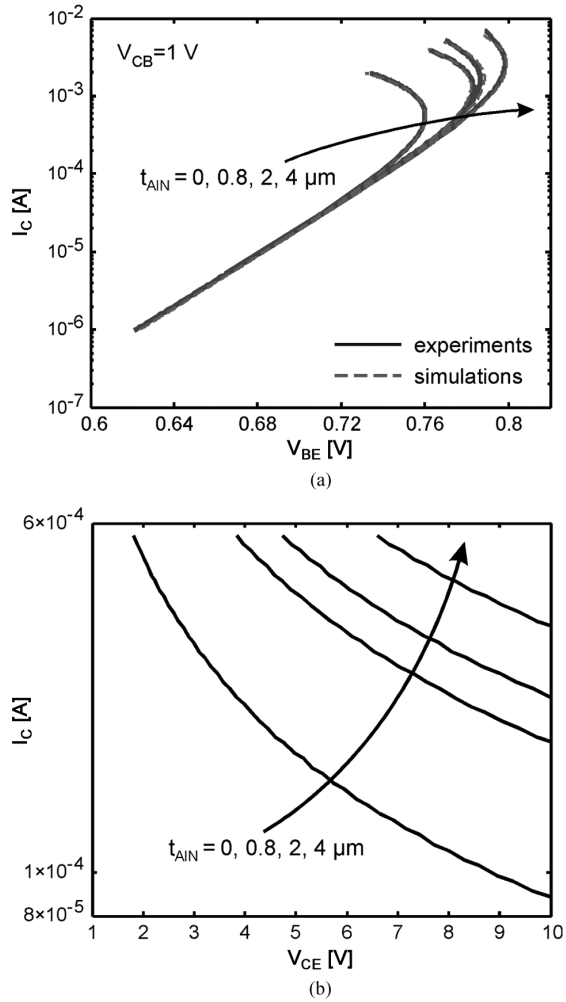

Fig. 16. (a) Experimental and simulated collector current I_C as a function of the base-emitter voltage V_{BE} for an NPN covered with AlN layers of different thickness t_{AlN}. (b) Simulated DC thermal limit of the safe-operating-area of bipolar transistors described in Table V.

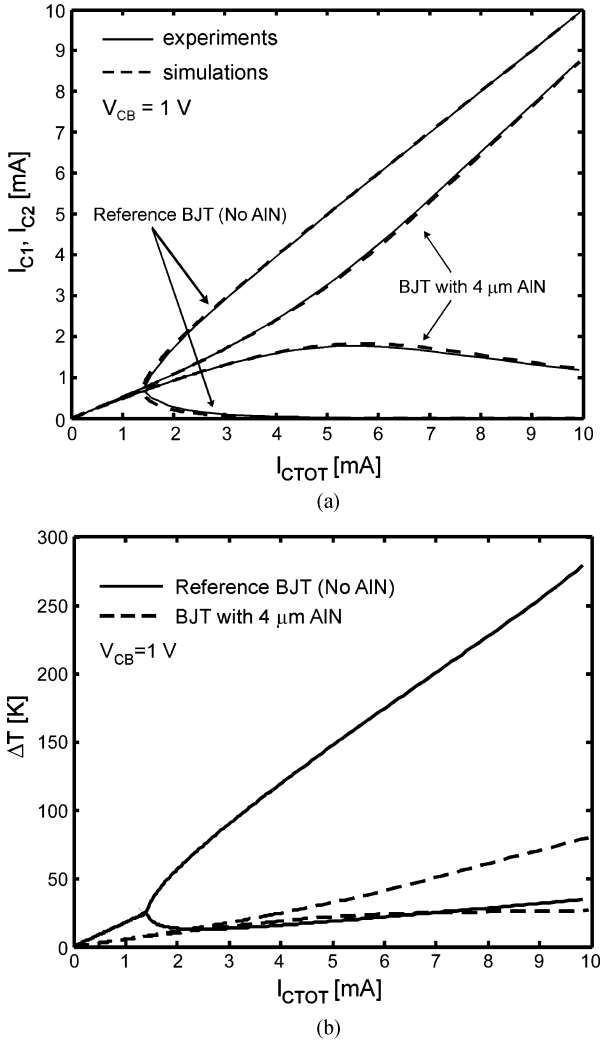

Fig. 17. (a) Measured (solid lines) and simulated (dashed lines) collector currents, and (b) simulated increase of temperature above ambient of the individual transistors of a pair operated in parallel as a function of the total collector current for devices with and without a 4-μm-thick layer of AlN. For these two identical NPN BJTs the emitters are 42.5 μm apart and separated by otherwise thermally isolating materials.

For current-controlled BJTs working in parallel, it is known that an increased thermal coupling between the two devices improves the overall electrothermal stability. A figure of merit for the electrothermal robustness of such a circuit is given by the collector current, $I_{C,crit}$, at which thermal instability appears. In a current controlled two-emitter-finger device, the onset of the current bifurcation is described by the relationship [48], [49]

$$I_{C,crit} \propto \frac{1}{V_{CE}(R_{TH} - R_M)} \tag{6}$$

where V_{CE} is the collector-emitter voltage. For the situation illustrated in Fig. 17, the difference $R_{TH} - R_M$ drops from 15600 K/W to 4000 K/W when the AlN heatspreader is added.

For circuits of elementary transistors connected in parallel, the electrothermal feedback is very susceptible to all the small differences that are in practice always present in "identical" devices. For example, the surroundings of the outer fingers are often designed differently from the inner fingers in which case the outer fingers will show the most deviating behavior, but also more subtle differences such as an asymmetry with respect to the position of the connecting metal tracks can cause significant differences in thermal resistance. In Fig. 18, a circuit of four BJTs operating in parallel is considered. The four emitters and base terminals are all connected, while the collectors are contacted individually and the collector current of each transistor is measured. The circuit without extra cooling is already instable at very low current levels. The outer transistor #4 hogs 50% of the total collector current at $I_{CTOT} = 1$ mA. For a device with a 4-μm-thick layer of AlN added, the operating temperatures of the four devices become closer and BJT #4 takes only half of the total current at $I_{CTOT} = 3.7$ mA. Thus, the reliability of the overall circuit is significantly improved.

V. Future Potentials

A. Potentials for HF SiGe HBT Fabrication

The future of Si-based high-speed bipolar transistors is strongly influenced by two other semiconductor developments. On one hand, SiGe HBTs must compete in speed with III-V HBTs, which in InP have already reached an operation

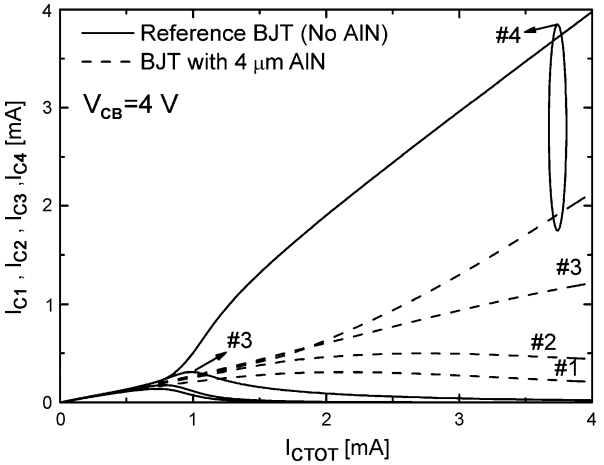

Fig. 18. Measured collector currents of the individual transistors of a set of four operated in parallel as a function of the total collector current for devices with (dashed lines) and without (solid lines) a 4-μm-thick layer of AlN. The neighboring emitters are 12.5 μm apart and separated by otherwise thermally isolating materials.

frequency of 1 THz [50]. This is three times the speed demonstrated in SiGe devices for room temperature operation [51]. On the other hand, SiGe bipolars have always had the advantage of being compatible with CMOS, but as the speed domain of pure CMOS is ever increasing, the cost and versatility with which SiGe HBTs can be integrated will continue to be important considerations when making process development choices.

The downscaling of SiGe HBT vertical doping profiles needed to reach f_T's way above 500 GHz has been theoretically predicted [52], but the concomitant downscaling of the series/contact resistances and capacitances is technologically very challenging. Obviously, the two-sided contacting can offer some relaxation of the device design compromises. With the aligning of the collector contact under the emitter, the R_C can be minimized. For a doped collector, the minimum R_C is determined by how well the doping technology can be downscaled. For low-ohmic contacting, high surface doping must be accommodated. With Schottky collector contacting, R_C can be entirely eliminated and reduction in transit time and storage time also gives a speed advantage [53], [54]. The surface recombination velocity at the metal-Si interface becomes the element that can limit the current handling capability. The metal will in first instance be chosen to have a Schottky barrier-height high enough to enable contacting as close as possible to the high-doped base while still maintaining good collector-base diode characteristics. The proximity of the metal contact to the high-doped base may have a benefit for cutting off collector-current (non-local) avalanching. For high frequency (HF) analog applications, any resulting high offset voltage is not problematic, so the optimization for high breakdown voltages will determine the collector design.

The future SiGe HBTs may have to be integrated with SOI fully-depleted CMOS [1] with Si top-layers of about 100 nm or less. In this case, the collector design is the key issue. A fully-depleted collector has been proposed in [55], which trades f_T for base-collector breakdown voltage. If SOI CMOS were to be extended to a substrate transfer implementation, the integration of SiGe HBTs with two-sided contacting becomes straightforward. Even for ultra-thin SOI below 50-nm-thick, the vertical dimensions are large enough to be able to accommodate a Schottky collector contact placed directly on the base.

B. Technologies for Two-Sided Contacting

Even though the SOG substrate transfer process is more evolutionary than revolutionary, from a production point of view it involves process modules that are not very widely used. In this respect it would be more attractive to achieve the two-sided contacting by micromachining of cavities to locally remove the substrate below the vital circuit regions. In silicon this would almost always imply the use of SOI wafers so that the BOX can be used as etch-stop. In III-V realizations, however, etch-stop layers can be grown along with the device layer stack. The main disadvantages of the micromachining version, as compared to the SOG solution, lie in the inferior accuracy of the patterning in the cavities. For large area back-wafer contacts, such as those needed for varactors, this does not become a serious limitation. Nevertheless, the size of the circuit will always be limited by membrane stability issues. This makes SOG the more flexible approach to two-sided contacting.

For the SOG IC-processing technology, the individual processing modules, including the STT and the laser annealing [56], have all been production-proven to some extent. The main concerns are connected to the stress relief experienced after gluing and silicon removal. In all our processes, the Si is thinned to around a micrometer or less and, at this thickness, Si is strong but bendable. However, topography introduced by trenching of the Si and thick metal stacks can induce high-stress points that break when the bulk-Si is removed. This does not necessarily cause direct damage of the Si devices, but will readily lead to cracks that expose the glue and front-wafer device-regions during Si-removal. This, together with bowing of the wafer, is very detrimental to the further processing of the back-wafer. In particular, the wafer-stepper alignment has need of a flat back-wafer surface [57]. Most of these stress-related problems can be minimized by using low-stress materials and well-chosen design rules for the circuit integration. Moreover, the choice of glass wafer is extremely important: a more rigid/thicker glass substrate will reduce stress-relief induced cracking. Also, choosing glass with a thermal expansion coefficient close to that of Si is beneficial. We have obtained very reliable results with 700-μm -thick glass wafers and a glue thickness in the 5–10 μm range. Nevertheless, cracking has limited the AlN thickness that we can integrate reliably in the front-wafer processing to 4 μm.

The SOI wafers used in the SOG process are more expensive and less production-proven with respect to quality than bulk Si. However, the SOG gives a very significant reduction of processing steps with respect to a comparable bulk process and this compensates for the extra wafer costs. The very low device and circuit RC parasitics also lower the costs of establishing reliable design kits: as an example, an SOG varactor-circuit design-kit can be found in [58]. Moreover, the quality of the SOI wafers has also become an industrial focus point, particularly for the thin Si SOI needed for future fully-depleted CMOS. The SOG developments are in line with the targets of industrial consortiums dedicated to SOI CMOS development. The flexibility of the SOG process with respect to the back-wafer processing

would be considerably increased if the thermal budget was limited by the front-wafer metallization scheme and not by the glue. Forming-gas alloying could then also be performed at 400 °C on the back-wafer. In the presented processes all junctions are H-passivated in the front-wafer processing, but otherwise this could become a reliability concern.

With respect to packaging, already established packaging procedures can be used if the quality of the glass wafer is chosen to be able to withstand the same treatment as a Si-wafer. This is in contrast to the situation for RF-MEMS, where fundamentally new packaging strategies are being developed when moving parts have to be protected and not impeded in their mechanical behavior by the package. For SOG, the choice of substrate quality, which can also mean replacing glass by some other sort of material, can be seen as a matter of cost.

VI. Conclusion

This work demonstrates that unique technology platforms in research environments can be an attractive incubator for new device and circuit developments. Among other things, the access to two-side contacted SOG has boosted the theoretical understanding of electrothermal bipolar circuit behavior, given the incentive to introduce deposited AlN as a new device-level heatspreading material, and provided an experimental basis for the development of new and potent varactor circuit-topologies. These are all results that can be adopted by industry also in other technology platforms.

The two-sided contacting offers a very effective means of reducing the RC parasitics, which is one of the prerequisites for efficiently exploiting silicon in RF/microwave applications and carrying it into the terahertz age. As compared to micromachined versions of two-sided contacting, the SOG technology offers much more flexibility and, in contrast to disruptive technologies such as RF MEMS, the SOG option contains no fundamentally new manufacturability challenges.

Acknowledgment

The authors would like to thank the staff of DIMES cleanrooms and measurement rooms for their continual support.

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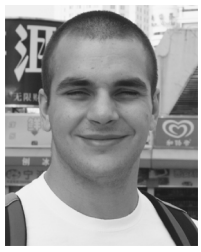

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