Nanomaterials Processing for Flexible Electronics

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***Abstract*— Inorganic nanomaterials such as nanowires (NWs) and nanotubes (NTs) are explored for future flexible electronics applications due to their attributes such as high aspect ratio, enhanced surface-to-volume ratio, prominent mobility and ability to integrate on non-conventional substrates. Device performance of semiconducting NWs are demonstrated to be superior compared to the organic counterparts. Among the synthesis methods, bottom-up vapour-liquid-solid (VLS) growth mechanism playing central role for preparing wide variety of high crystal quality semiconducting NWs. However, the high temperature synthesis process prevents fabrication of NW devices directly over flexible substrates which imply the investigation of efficient transfer techniques such as dry contact printing and electric field assisted assembly. Currently, many efforts are directed to study the integration techniques of NWs from growth substrates to non-conventional receiver substrates and parameters such as transfer-yield, alignment and density. These efforts will help to utlilize NWs as building blocks in future flexible electronic devices and circuits. This work focuses on VLS growth of semiconducting NWs and their transfer-printing over large area substrate to fabricate flexible electronics.**

Keywords—Nanowires, VLS growth mechanism, Transfer printing, Flexible electronics

I. Introduction

Large area flexible electronics holds promise for many applications in photovoltaics, photonics, optoelectronics, light emitting diode (LED) displays, sensors and robotics [1, 2]. For example, tactile feedback for future robots will help to interact with the surrounding in a much safer way [3]. Realization of such systems require high performance electronic devices and circuits to be fabricated over flexible organic materials. Organic materials dominate in flexible electronics research due to the convenient processing methodologies. Importantly, organic devices and circuits have been fabricated over large area flexible materials through low temperature printing or additive techniques [4-6]. However, organic electronics present some drawbacks such as rapid switching time, poor device stability and low device density. These problems lead researchers to look for alternative materials and devices for future flexible electronics [7, 8]. Inorganic compounds provide variety of materials for envisaged applications in flexible electronics. Bulk and thin films of semiconductors such as Si, Ge, GaAs, GaN, etc., are few examples and their devices were widely studied for many applications in the past. This includes field effect transistors (FETs), LEDs, wave guides, physical- and chemical-sensors and photovoltaic devices. The major hurdle lies in the integration of these devices over flexible materials. The problems partly rests on the high processing temperatures and fabricating larger than wafer scale systems. Compared to bulk and thin films, semiconductor nanostructures provides advantage to utilize their attractive physical and chemical properties for future flexible electronics systems. One dimensional (1D) materials such as nanowires (NWs), nanotubes (NTs) [9], etc. and two dimensional (2D) materials such as graphene, MoS_2, WS_2, etc. have shown interesting electrical, optical and quantum properties when one of its dimensions falls in the range of 10 to 100 nm regime [10]. NTs are one of the best studied 1D nanostructures tested for wide variety of applications over three decades. Additionally, semiconducting NWs such as Si, Ge, GaAs are expected to make huge impact in future flexible electronics devices and systems. Research efforts are directed in two distinct aspects in NWs to make use of them in flexible electronics: (1) synthesis techniques to produce composition controlled single crystalline NWs at specific locations, and (2) processing techniques to fabricate NW devices and circuits over flexible large area. In this regard, the focus of this paper is to provide a summary of pathways to utilize high aspect ratio nanostructures such as NWs for large area flexible electronics.

II. Synthesis Techniques

NWs synthesis method plays a key role in deciding performance of the devices. Growth process controls the crystallinity, composition, dimension and location of NWs [11]. Variety of physical and chemical techniques have been used in the past to obtain electronic device quality NWs (TABLE I). Additionally, growth mechanisms are categorized as bottom-up and top-down processes. Bottom-up techniques utilizes atoms and molecules as starting precursors to build the NWs. This technique could be executed using some of the listed thin film deposition technique in TABLE I. In contrast, top-down NWs preparation techniques start with the bulk wafer of the NW material as starting source. Availability of bulk wafer sets the limiting factor in this method. Comparing both methods, majority of the NWs based device prototypes in nano-electronics and sensors have been demonstrated using bottom-up methods [12]. Catalyst-assisted vapour-liquid-solid (VLS) growth mechanism plays a central role in semiconducting NWs synthesis. VLS mechanism has been used to produce elemental to ternary NWs with precisely controlled diameters in sub 100 nm range. Most of the thin deposition techniques have been explored to execute VLS growth mechanism. Among them, chemical vapour deposition (CVD) technique is advantageous for the following factors: (a) availability of wide variety of source precursors (b) CVD variants (LPCVD, APCVD, MOCVD etc.) provide rich experimental conditions to obtain well controlled NW growth rate (nm/s) (c) controlled *in-situ* doping is a potential advantage of CVD process. Additionally, CVD is compatible with CMOS device fabrication technology. Si NWs have been conveniently grown using VLS mechanism in the range of 3-100 nm which are a suitable candidate for flexible electronics.

TABLE I. COMPARISON OF DIFFERENT PHYSICAL AND CHEMICAL TECHNIQUES USED FOR NWS SYNTHESIS

Technique	*Source materials*	*Advantageous*	*Disadvantageous*
Physical techniques			
Evaporation (Thermal & e-beam)	Filaments, wires, etc.,	Low cost method	Not suitable for semiconductors
Sputtering	Solid targets	Low cost and composition tuned NWs	Not suitable for oxygen sensitive materials
Laser Ablation	Solid targets	Suitability for sub 20 nm wires	Not suitable for compound semiconductors (i.e.GaAs, GaN)
Molecular Beam Epitaxy(MBE)	Solid evaporation materials	Suitability for wide materials system	Expensive technique and low growth rates
Lithography-dry etch techniques	Wafers	Precisely defined array of micro-wires	Expensive tools
Chemical techniques			
CVD-LPCVD or APCVD	Vapour molecules and gases	Single crystal composition controlled NWs	Harmful gas sources
Gas phase techniques (For CNTs, ZnO)	Gaseous molecules	Large quantity synthesis	Low reproducibility
Chemical beam epitaxy	Metalorganic gas precursors	Suitable for many materials	Expensive method
Metal assisted chemical etching (MACE)	Wafers	Low cost and simple to execute	Requirement of wafers

Si NWs could potentially utilize well-established device fabrication technologies. VLS process requires a nano-sized catalyst particles prepared over the substrate as a first step. The size of the catalyst particle decides the diameter of the NWs. Si NWs have been grown using Au catalyst nanoparticles (NPs) prepared using variety of techniques. Thin film dewetting is the simplest among the methods to produce NPs of diameters from few nanometers to microns. In the controlled CVD ambient, Au NPs are exposed to the silicon sources such as SiH_4 or $SiCl_4$ at the temperature above 363˚C. The vapour flux (SiH_4 or $SiCl_4$) chemically dissociate over the catalyst surface to inject Si atoms into the Au catalyst particle. This process converts Au particle into Au-Si liquid solution upon continuous injection of Si. This process leads to Si saturation in the Au-Si solution which results Si NWs precipitation at the catalyst-substrate interface (Fig.1 (a-c)). The saturation level depends on the temperature and the driving force is quantified using the expression [13],

$$\Delta\mu_{LS} = kT\ln\left(\frac{C}{C^o}\right) \qquad (1)$$

Where, C is actual concentration of the Si in the catalyst droplet, C^0 is the equilibrium concentration of the Si at the growth temperature.

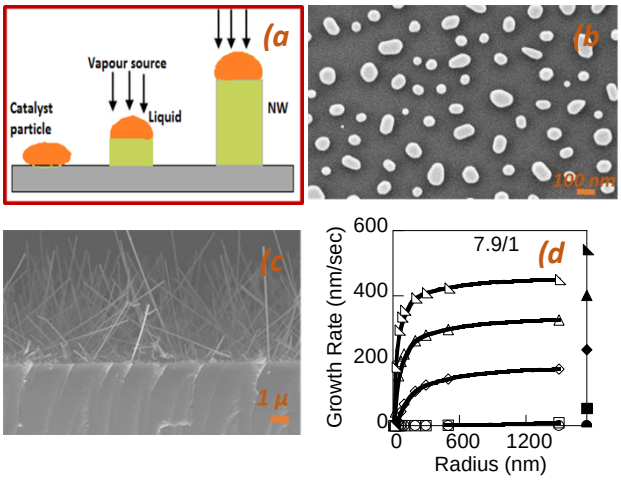

Figure 1. VLS NWs growth process steps and growth rate prediction using kinetic models. (a) Schematic diagram of the growth process. (b) SEM image of Au NPs prepared by dewetting process. (c) Cross-sectional SEM image of Si NWs by CVD assisted Si NWs. (d) Predicted NWs growth rate through models; insets are kinetic parameters.

Kinetic studies have confirmed that the (C/C^0) ratio ranges between 1.1 to 1.5. This value is used to estimate the growth rate of NWs [14]. Typically, NWs precipitate at the interface through layer-by layer (LL) growth mode. The atomistic aspects of the process are well controlled using modern gas handling systems in CVD tools. The dependencies of the growth process, such as catalyst diameter, temperature and pressure is studied using kinetic models. The growth rate of the LL mode crystallization is expressed as,

$$\left(\frac{dh}{dt}\right)_{LL-IF} = (J\pi R^2)a \qquad (2)$$

Where, J is nucleation frequency (could be deduced from classical nucleation theory) of the Si 2D crystals, R is the radius of the catalyst droplet and a is the step height of each layer [15]. These studies helped to predict NW growth rates under different CVD experimental conditions (Fig.1d). The growth rates of NWs varied between few nm/s to ~100 nm/s. The control in the growth process lead to the development of many device prototypes using VLS mechanism. VLS NWs could be grown on any required substrate at an elevated temperature typically above 400˚C. High temperature is a required parameter as its helps to attains the required crystallinity and dopant composition. VLS grown NWs are oriented vertical to the substrate surface. Hence, the mandatory requirement is to transfer print them over polymer materials for flexible electronics applications.

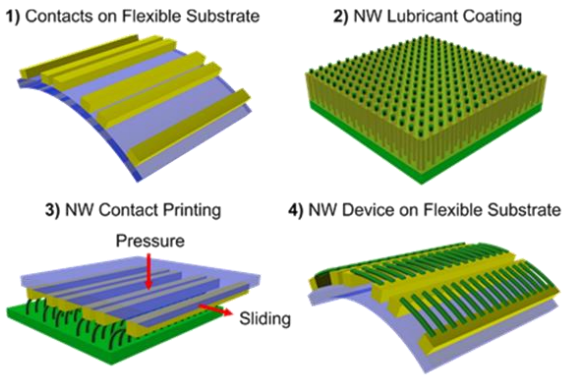

Figure 2. 3D schematic illustration of the contact printing procedure, including (1) electrode patterning on flexible substrate, (2) chemical treatment of the NW sample surface, (3) contact printing, and (4) resultant device.

III. TRANSFER PRINTING METHODS

Towards the aim of large area, high density devices and circuits based on semiconducting NWs, the transfer and alignment of as-grown NWs to a foreign substrate is another essential aspect to be investigated. The receiving substrate can be non-conventional, comprising flexible materials such as polyethylene terephthalate (PET), poly(ethylene 2,6-naphthalate) (PEN), polyvinyl chloride (PVC) and polyimide, as well as, conventional rigid substrates according to various applications requirements. To date, different methods have been developed towards this goal. The investigation direction focuses on the transfer yield, the alignment of the transferred NWs, as well as, preserving its intrinsic properties. In general, these transfer techniques can be divided into two types: (1) dry transfer method and (2) wet transfer method.

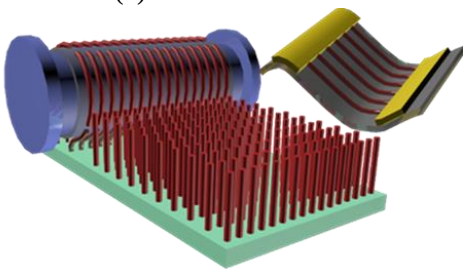

Figure 3. 3D schematic illustration of the roll-printing fabrication procedure of flexible electronics based on NWs.

A. DRY TRANSFER METHOD

In the dry transfer method, the NWs experience a segregation/anchor process due to the adhesion force between nanowires and receiver substrate and an alignment process due to the directional shear force [16]. Initial studies usually mix up the two processes and neglect the alignment hindering effect from the anchor process. However, even in this case, the alignment degree and transfer yield are rather good after minimizing the NW-to-NW interaction by introducing lubricant and increasing the adhesion force by surface functionalization [17, 18]. This initial dry transfer method is named as "contact printing" method. A schematic illustration (Fig. 2) shows four-steps based contact printing process towards a NW flexible device.

The contact printing method is subsequently extended to so called "roll printing" method [19] towards large area, roll-to-roll fabrication as shown in Fig. 3. In the study of the dry transfer technique, the separation of anchor and alignment is realized by J. Yao *et al*. Contrary to previous studies, substrate with two different areas are used. One part is surface covered with photoresist, which only has a very weak adhesion force to NWs; the other part is surface after a photoresist underdeveloped process, which has a very strong adhesion force to NWs. Thus, the transfer yield is dominated by the highly adhesive area and the alignment degree is dominated by the lowly adhesive area; they will not interfere with each other. A surprisingly high alignment degree is achieved by using this method due to the anchor and alignment isolation.

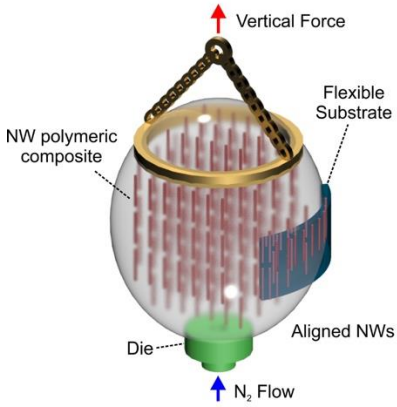

Figure 4. Schematic illustration of the BB method to align NWs.

B. WET TRANSFER METHOD

Solution based wet transfer techniques are alternative methods towards inorganic nanowires transfer. In this regard, drop-casting NWs based solution onto pre-patterned substrate is a simple approach towards NWs based flexible electronic devices. However, this method suffers from the drawbacks such as uncontrollable and low successful device yield, poor contact between metal electrode and inorganic NWs, etc. Other alternatives such as Langmuir–Blodgett (LB) technique [20, 21], bubble-blown (BB) technique and non-uniform electric field assisted alignment method are investigated by researchers to overcome these drawbacks [22]. The electric field assisted alignment, which is also called dielectrophoresis (DEP), is developed to accurately manipulate the position of NWs. Non-uniform electric fields are applied to polarize suspended NWs attracting them to pre-defined locations on the substrates. However, such method involves the complex DEP electrode fabrication and a specific electric field generation in individual locations, which are drawbacks in industrial level NWs devices and circuits fabrication. Towards a simple, wafer scale transfer and alignment of inorganic NWs, BB technique has been developed by G. Yu *et al*. [23]. As shown in Fig 4, the NWs are first embedded into a polymeric suspension then the suspension is expanded to a bubble. The effect of NWs alignment comes

from the shear force during the expansion process as shown in Fig. 4. After the bubble formation and nanowire alignment, the receiver substrate is brought into contact with the bubble surface and NWs are transferred from solution to a foreign substrate. This method can be used for ultra large scale transfer and alignment of NWs. However, the low NWs density around 0.04 NW/μm^2 is a major drawback of this method, which hinders its application towards high density NW-electronics.

IV. Conclusions

Inorganic semiconducting NWs are suitable candidates for the envisaged applications in flexible electronics applications. Nanoscale materials processing poses significant challenges compared to bulk and thin film forms. VLS growth mechanism is a promising synthesis method to prepare required semiconducting NWs with controlled dimensions in the order of few nanometers to microns of diameter. The major advantage is the ability of the method to produce composition controlled (ppm level) single crystalline NWs at a specified location. The evolution of the CVD technique is a major advantage for the VLS process to produce any required material under one roof. CVD assisted VLS technique cannot produce NWs directly over flexible substrates due to the high growth temperatures. This causes the requirement to develop room temperature transfer printing techniques. Variety of dry and wet contact printing process has been developed in the past to utilize VLS NWs. Contact printing dry transfer process holds significant edge over other techniques as it could be extended over large area. The roadmap leads towards the development of roll-to-roll contact printing of NWs over flexible materials to high performance electronics.

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