Single Supply CMOS Up Level Shifter for Dual Voltage System

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***Abstract*—A single supply CMOS up level shifter (rsc–ls), for upconverting signals from 0.45V–0.9V logic level range up to 1V power supply voltage domain (Vdd), is introduced. From simulations results, the proposed shifter provides improvements of 63% and 69% in energy consumption and speed, respectively, when compared with a similar design, in 65nm CMOS process and low threshold voltage. For a Vdd of 1.2V we obtain up to 88% improvement in delay–energy product, when the input signal high voltage level is 0.7V with a frequency of 500MHz. We report a total static current reduction of up to 110 times. For an up shift of 0.45V to 1.2V at an output loading of 800fF, our design offers a delay of 0.38ns and an energy consumption of 1.57pJ.**

I. Introduction

To reduce power dissipation, modern systems support multi–supply voltage domains. Each domain operates at a particular power supply voltage depending on its own performance requirement. It may be even desirable to significantly reduce the power consumption by operating part of the system in sub–threshold regime. A level converters are required to up and down shift the signals from/to the lower to the higher/lower power supply domains. High power efficiency is a challenge in the design of up level shifters.

A general up level converter consists of three parts; the low voltage stage (`Vddl` domain), a fast up converter interface circuitry, and a high voltage stage (`Vdd` domain), with a high drive circuitry.

One challenge in the design of up converters is the elimination or significant reduction of the undesirable static current, and therefore energy consumption. This current is the result of the high input logic (`Vddl`) not being high enough to completely turn off the following PMOS pull–up network that is connected to `Vddh`. Other challenge is the minimization of the delay in the level converters.

A subthreshold level shifter which uses a self–controlled current limiter by detecting the output error and realizes a voltage conversion from 0.1 to 1.2V with limited static power consumption is presented in [1]. At 0.2V, the circuit operates at a maximum input frequency of 254kHz. This circuit is useful to prolong operational lifetime from constrained power supplies for biological systems, and wireless sensors.

Typical techniques to reduce the short circuit current make use of diode–connected transistors and multi–threshold CMOS voltage (MTCMOS) to up convert the voltage signals. The cross coupled circuit topology proposed in [3] exploits the leakage current mirror technique to reduce the static current across a wide range of conversion voltages.

A Pseudo–Diode-Mirrored (PDM) level shifter with a small DC current is shown in [4] which enables resistive RAM (ReRAM) to achieve sub–0.5V read/write operations. This is useful for applications that require low power supply operations and non–volatile memory for power reduction.

The work in [5] proposed a hybrid structure comprising a modified Wilson current mirror and generic CMOS logic gates for upward and downward level conversion in a 65nm technology. Bidirectional level conversion improves the energy efficiency of the interface for dynamic voltage scaling (DVS). It also helps to reduce the high amount of quiescent current that occurs when the input voltage is in subthreshold region. This region of operation limits the use of the conventional current mirror level shifter. This circuit also has the desirable property of low sensitivity to transistor sizing, threshold voltage variation, and other process variations.

In order to reduce the power area cost, as well as extending the operating range, a cross–coupled half latch structure is presented in [6]. Two off–biased PMOS transistors are inserted to provide sufficient leakage current for the proper operation the converter since the NMOS transistors in the pull–down network are able to sink that leakage current. Fig. 1, presents a modified version of the circuit in [6] where two diodes (on–biased NMOS transistors), `D0` and `D1`, replace two off–biased PMOS transistors. The use of low threshold voltage NMOS transistor provides a basis for a fair comparison with our work in this paper, where the key idea is to obtain a fast and low energy level converter.

The rest of this paper is organized as follows. Section II introduces the proposed voltage up level shifter (*rsc–ls*). In Section III, simulation results are discussed and evaluated. Section IV considers post–layout simulation results of our design verifying the efficiency of the proposed circuit. Finally, this work offers a conclusion in Section VI.

II. The Single Supply up level Shifter Circuit Topology

The proposed circuit is a structure comprising three inverters and some additional transistors to reduce the static current using the logic level for node `3`, as shown in Fig. 2. When

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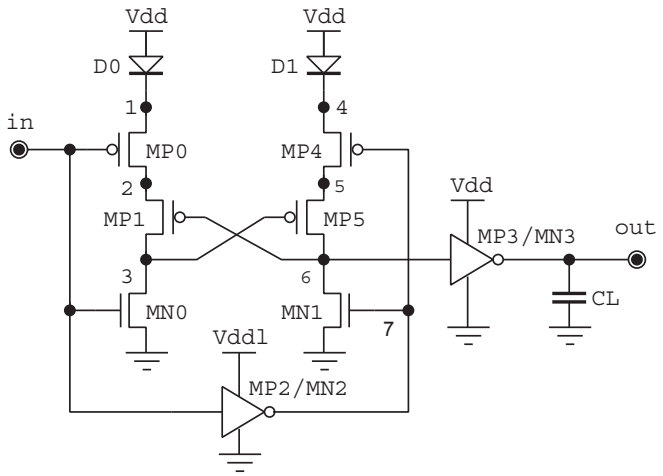

Fig. 1. The circuit diagram of *bm–ls*

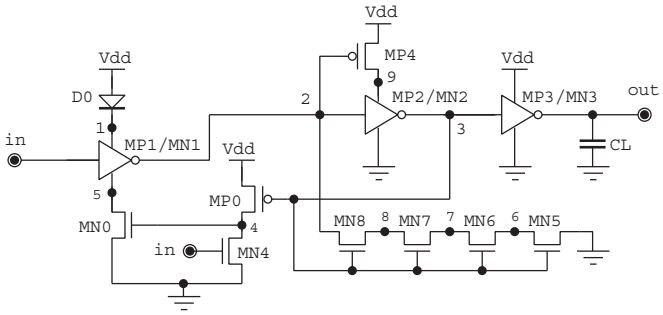

Fig. 2. Schematic for *rsc–ls* up level shifter

node in is high, inverter MP1/MN1 produces a low level at node 2, pushing node 3 to a high level. The inverting buffer (MP3/MN3), designed to assure adequate output driving strength, provides a low level on node out and capacitive load CL is discharged through MN3 transistor. The NMOS diode (D0) acts as current limiter, and is used to mitigate the current contention at the beginning of the discharge transition at nodes 2 and 5. Inverter MP2/MN2 also drives the gate of MP0 causing it to turn off, while the string of NMOS transistors (MN5–MN8) is turned on, which is used as intermediate stage to reduce the short circuit current and stand–by energy consumption in combination with MP0, MN0, and MN4 transistors. The low level on node 2 is achieved through the chain of transistors (MN5–MN8). On the other hand, transistor MN4 is turned on, pulling node 4 low, and turning MN0 off. Note that the only path for the static current is through high resistance path, consisting of the chain of MN5–MN8 transistors, to ground instead of current flowing out of node 5 through MN0. In this way, the short circuit current in the input inverter (MP1/MN1) is significantly reduced with respect to *bm–ls*, while the output switching speed is also improved.

When the input signal on node in is low, the voltage on node 2 is high (Vdd-VD0) and, consequently node 3 is switched to low. Moreover, node out pulls up and CL is quickly charged. This operation is also favored by current-limiting action of the string of transistors MN5–MN8, device MP0, and by the presence of transistors MN0, and MN4 which keep node 2 at a high level. In this way, transistors MN5–MN8, and MN4 are turned off, while transistors MN0, and MN0 are switched on. Node 5 is set to ground.

TABLE I
CHANNEL WIDTHS FOR TRANSISTORS IN FIG. 1, AND FIG. 2

Fig. 1 (Active area=310.7μm^2)		
Transistor(s)	Type	Width (μm)
MP0 and MP4	P	150 × 10.0
MP1 and MP5	P	3 × 10.0
MP2	P	80 × 10.0
MP3	P	1 × 10.0
MN0 and MN1	N	1 × 10.0
MN2	N	8 × 10.0
MN3	N	1 × 10.0
D0 and D1	N	40 × 10.0
Fig. 2 (Active area=3.94μm^2)		
Transistor(s)	Type	Width (μm)
MP0	P	1 × 0.25
MP1	P	1 × 6.0
MP2	P	1 × 2.5
MP3	P	1 × 10.0
MP4	P	1 × 0.65
MN0	N	1 × 6.0
MN1 and MN3	N	1 × 10.0
MN2	N	1 × 4.0
MN4 up to MN8	N	1 × 0.25
D0	N	1 × 10.0

Vthn= 0.28V, and Vthp=-0.2V

We used only low threshold devices to evaluate the performance of both circuit topologies. For the sake of a fair comparison, we replicated the both designs in CMOS process, while imposing a transistor length of 65nm and maintaining the same ratios of Wp/Wn (16/4) for the five input inverters in connected series that derive the node in for both *rsc–ls* and *bm–ls* circuits, and for the output inverter attached to node out. The circuits were sized as reported in Table I. The total equivalent length for the string of serially connected transistors (MN5–MN8) is 0.26μm, with all transistors in the chain having the same sizes as the rest of devices in the proposed up converter. With this sizing configuration, the string draws lower static current when is turned on. Furthermore, *rsc–ls* requires only 3.94μm^2 of active area, or 78 times less than the respective areas for *bm–ls* in 65nm CMOS technology.

Fig. 3 illustrates the output voltage waveforms for both *bm–ls* and *rsc–ls*, respectively. Simulations were performed considering a input signal frequency of 500MHz, input signal voltage of 0.7V, and 800fF of capacitive load. Note that *rsc–ls* has a significantly faster response with respect to that of *bm–ls*. Our up level converter operates correctly for Vddl as low as 0.45V. However, *bm–ls* fails to operate correctly when Vddl$<$ 0.7V. This is because the strength of the pull–down transistors is limited by Vddl.

III. PERFORMANCE ANALYSIS

Pre–layout simulations were performed for both circuits, using an input signal frequency of 500MHz, Vdd fixed to 1.2V,

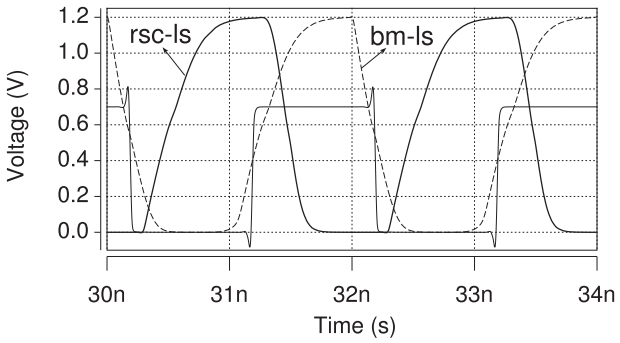

Fig. 3. Simulated pre–layout waveforms for *bm–ls*, and *rsc–ls*. A 800fF load capacitance is attached to the output

a parasitic capacitor of 25fF added to the input of each of the five inverters connected in in series that drive the node `in`, and an output buffer connected to the node `out` which is also loaded by an additional parasitic capacitor of 45fF in parallel to `CL`. Under similar conditions, *rsc–ls* has a 69% lower delay compared to *bm–ls* when loaded with a load capacitance `CL` of 800fF.

Our up level converter exhibits a significantly reduced energy, due to use of string of devices `MN5`–`MN8`, and devices `MP0`, `MN0`, and `MN4`. The efficiency of *rsc–ls*, in terms of energy consumption, is 63% higher than *bm–ls*. The energy–delay product for a load of 800fF, for *rsc–ls* is 88% lower than that for *bm–ls*.

The important feature of the proposed design is to reduce the static current. *rsc–ls* has a 110–fold lower current consumption (12.18μA/0.11μA) than *bm–ls* in the range of 80fF to 800fF `CL` load, for a 0.7V input voltage.

IV. Post–Layout Analysis for *rsc–ls* Circuit

Fig. 4 shows the layout view of the proposed up level shifter, which has been designed exploiting only metal 1 and 2 wire layers. In 65nm CMOS technology, the physical design of *rsc–ls* occupies a silicon area of only $54.9\mu\text{m}^2$ ($5.04\mu\text{m} \times 10.9\mu\text{m}$).

To further extend our analysis, we evaluated *rsc–ls* for the input range 0.45–0.9V, while keeping the same operating conditions and a 45fF capacitive load. As is shown in Fig. 5, the proposed up converter provides a good solution across a wide range of input voltages. As shown in Fig. 6, the circuit has a very small delay–energy product across a range of capacitive loads.

To investigate the robustness of the proposed up level shifter against device mismatch, we have performed a 500–points Monte Carlo (MC) simulation. The related results are shown in Fig. 7. The mean, and standard deviation for the delay–energy product are $184.2\text{e}{-24}$, and $64.3\text{e}{-24}$, respectively.

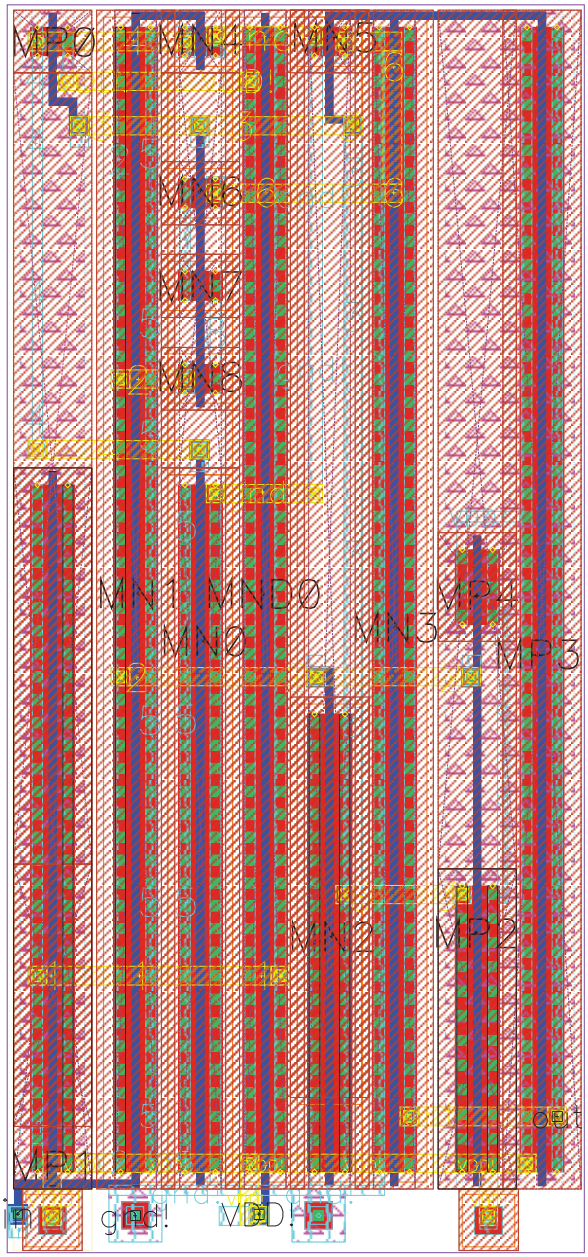

Fig. 4. Layout for *rsc–ls*

V. Comparison Results

Table II presents the results obtained for previously reported designs, and our proposed circuit. Design in [2] is implemented with high voltage CMOS transistors due to its greater output voltage. The area for *rsc–ls* is the lowest among all the designs. The delay and delay–energy product for the proposed *rsc–ls* circuit are the lowest, with the input signal ranging from 0.45 up to 1V and a load of $45fF$ and 1 buffer. Comparison of various circuits in Table II shows that [2] can operate under the highest loading condition. The slowest input voltage range is for [5].

TABLE II
COMPARISON OF THE PROPOSED DESIGN WITH OTHER UP LEVEL SHIFTERS

Desing	[1]	[2]	[3]	[4]	[5]	[6]	This work
Year	2016	2015	2014	2014	2014	2014	2016
Conversion	Up	Up	Up	Up	Up/Down	Up	Up
Technology	65nm CMOS	0.5μm HVCMOS	90nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Results	Measured	Measured	Post–layout	Measured	Measured	Measured	Post–layout
Area	31.3μm^2	1.1mm^2	Not available	Not available	16.8μm^2	7.8μm^2	3.9μm^2
Delay	13.7ns	0.5ns	2ns	Not available	Not available	66ns	0.39ns
Power	0.2μW	Not available	Not available	Not available	1–10nW	2μW	0.21mW
Frequency	1MHz	3.3MHz	1MHz	Not available	20KHz	72MHz	500MHz
EDP (J×s)	1245.33e-24	Not available	2900e-24	Not available	Not available	1848e-24	174.3e-24
Load	100fF	500pF	100fF	Not available	Not available	1 buffer	45fF + 1 buffer
Voltages (V)	0.1 to 1.2	0.5 to 100	0.15 to 1	0.1 to 2	0.1 to 1.2	0.12 to 1.2	0.45 to 1

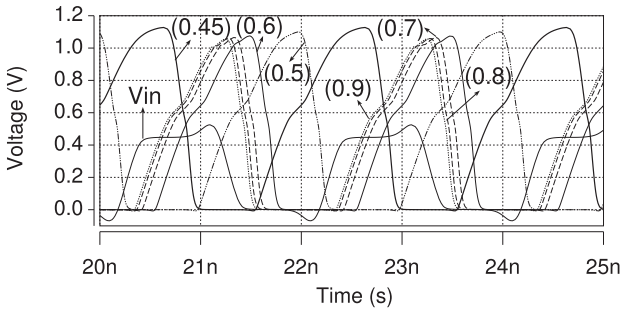

Fig. 5. Waveforms for the post–layout simulation for *rsc–ls* at 20fF

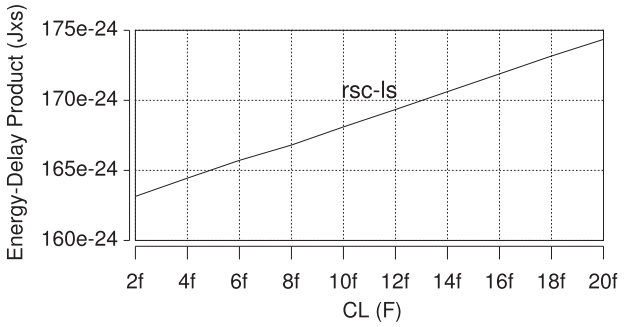

Fig. 6. Delay–energy product for the post–layout simulation for *rsc–ls*

VI. CONCLUSION

This paper compares the proposed up level shifter with a similar circuit. Both up converters are simulated using a 65nm CMOS process. Our design (*rsc–ls*) exhibits low static current consumption with lower delay (69%), lower energy (63%), and better delay–energy product (88%) than circuit used as reference (*bm–ls*). This is obtained while consuming a 110–fold lower static current, and occupying a 78–fold lower active area than *bm–ls*. From post–layout results, *rsc–ls* extends

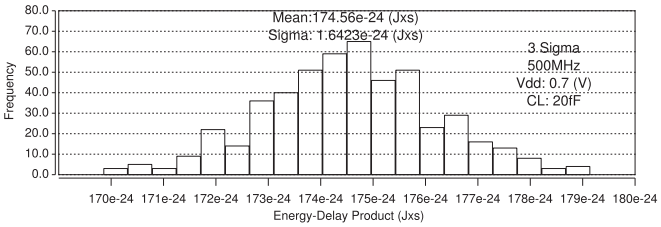

Fig. 7. Histogram for *rsc–ls*

the conversion range down to 0.45V, with a silicon area of 54.9μm^2 (5.04μm × 10.9μm). Moreover, when converting a 0.7V input to 1V output at 20fF it exhibits propagation delay of 0.39ns and energy of consumption of 0.43pJ.

ACKNOWLEDGMENT

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