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***Abstract*—PUFs (Physical Unclonable Functions) have been proposed as a cost-effective solution to provide a root of trust for electronic devices which exploit intrinsic process variability. They generate identification signatures and keys only when the devices are turned on, avoiding the storage of sensitive information in memories that could be targeted by attacks. Although PUFs have many perceived advantages, they also have disadvantages such as sensitivity to temperature. Indeed their behaviour can be affected by the fact that high temperatures can accelerate permanent and transient phenomena, such as aging and transistor switching speed. In this paper we show the effects of externally induced heat on the functioning of Ring Oscillators (ROs), which form the basis of RO-PUFs. Moreover, we discuss the feasibility of temperature attacks on PUFs.**

***Index Terms*—Physical Unclonable Function, Aging, Ring-oscillator, Hardware security**

I. Introduction

Nowadays, device security is a crucial aspect, particularly because electronic devices are used for daily tasks, sometimes sensitive, such as banking transactions and storage of personal data. Despite the progress that security (both hardware and software) has made over the years, hackers continue to come up with ways to defeat even the most secure systems.

In recent years, a new purely-hardware primitive has emerged to protect chips from cloning and duplication. This primitive, called PUF (Physical Unclonable Function) [1] [2], does not require memory blocks to store secret keys [3], but generates them on demand. PUFs exploit the natural variability resulting from fabrication [4], and therefore it is almost impossible to predict or clone the value of the generated key. One of the most studied PUFs is based on Ring-Oscillators (ROs). The frequency of ROs depends on the number of inverters, the technology of the transistors, the operating environment, aging and process variability. The operation of RO-based PUF is based on the comparison of frequencies among identically designed ROs, which are affected by process variability.

Although this solution can be effective and mostly reliable, it is not immune to attacks, particularly based on temperature variations. In the literature, temperature is often used to accelerate aging effects [5] [6], which tend to change transistor performance almost permanently. The most temperature-sensitive aging effects are Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI), and their effect can be exacerbated by extreme temperatures.

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It is important to note that among all the existing attacks, cloning is one of the most dangerous, as it allows the attacker to circumvent the PUF. Recently, the paper [7] exploited tailored bitstreams (generated by not respecting design rule checks) in order to create short circuits within an FPGA, thus deliberately raising the temperature around the ROs of a PUF and accelerate the aging process of PBTI (Positive Bias Temperature Instability). As a result of these efforts, they managed to successfully clone a RO-PUF .

Following the results shown in [7], this study focuses on the effects of temperature on PUFs, specifically ring oscillator PUFs. The study assumes that an attacker is able to locally modify the temperature of selected ring oscillators, either with short circuits (as described above) or with other techniques, such as laser injection.

This paper contributes to a better understanding of the effects of temperature on the reliability of ring oscillator PUFs and how this temperature can be used to attack these structures to instantaneously falsify their results. Since these effects directly affect transistors, they can be used to attack other types of PUFs as well, such as SRAM PUFs. Through Monte Carlo simulations on 65nm technology, our analysis highlights the significant impact of increasing temperature on ring oscillator PUF responses.

The rest of this paper is organized as follows. In Section II, we provide a comprehensive overview of PUFs, the impact of temperature and their reliability. In Section III, we discuss the temperature attack on ring oscillator PUF, and the possibility to exploit these phenomena at a local level, in Section IV we discuss the challenges posed by permanent and transient attacks on electronic chips, as well as potential methods for circumventing the security measures implemented to safeguard against such attacks. Finally, in Section V, we outline our future research directions, which will focus on fault injection in power-off circuits and we conclude our work.

II. Reliability and Temperature effects on PUF

Physical Unclonable Functions (PUFs) are intended to be used for security applications, and for this purpose, their response must remain the same throughout the entire use of the chip. This chapter shows that high temperatures greatly influence the behaviour of ring oscillators in time, which can lead to unreliability and therefore security issues.

The first part of this section provides a general overview of PUFs, including their characteristics and various metrics used

for evaluation. The second part presents simulation results on how temperature affects the reliability of a ring oscillator that composes RO PUFs.

A. *Physical Unclonable Function*

PUFs generate a unique output in response to a given input by exploiting the natural variability during semiconductor manufacturing, to provide a unique fingerprint for each physical entity [8] [9]. Indeed, during the manufacturing process used for producing most of today's electronic chips, small unintentional imperfections form on the silicon and the deposited layers [10]. This means that each fabricated device (transistor) physically differs from the others. This is the reason why we have ROs with different frequencies on a single chip

PUFs have two important properties: they use only simple circuits, and the signatures/keys are generated only when it is required, or at power-on [1] [2]. They are evaluated using various metrics [11] to measure their performance and reliability.

Uniqueness: Uniqueness refers to the capability of a PUF to distinguish a specific device from a population of devices in a unique manner. To evaluate uniqueness, each device is initially analyzed, and a reference sample is acquired. Subsequently, when a new device is introduced to the system, it is compared to every existing device by calculating the Hamming distance between their respective reference samples, as shown in equation (1).

$$Uniqueness = \frac{2}{k(k-1)} \sum_{i=1}^{k-1} \sum_{j=i+1}^{k} \frac{HD(P_i, P_j)}{n} \times 100\% \tag{1}$$

where k = the number of PUFs, n = the number of bits in each PUF response, P_i = the response of the i-th PUF, P_j = the response of the j-th PUF, $HD(P_i, P_j)$ = the Hamming Distance between these responses.

Reliability : PUF response must be reliable over time and in all usage conditions. In other words, if the experiment is repeated multiple times, the response should be always the same. In practice, reliability is difficult to ensure, as these circuits are sensitive to phenomena such as temperature, power supply voltages, and aging, which can alter the response and reduce reliability. It is therefore important to consider this notion during the manufacturing process. The reliability can be evaluated with this formula :

$$Reliability = (1 - \frac{1}{x} \sum_{y=1}^{x} \frac{HD(R_i, R_{i,y})}{n}) \times 100\% \tag{2}$$

where x = the number of samples taken from the PUF responses, R_i = the response extracted from the ith board, n = the number of response bits generated by the PUF, HD(Ri, Ri,y) = the Hamming distance between the response Ri and the yth sampling, Ri,y = is the y-th sample of Ri.

Uniformity : Uniformity assesses the distribution of responses among all instances of a PUF and is indicated by the arrangement of '0's and '1's within the response bits. A uniform distribution of responses is preferred because it guarantees that the PUF is equally resistant to attacks, regardless of the specific PUF instance being targeted. The optimal value is 50%.

$$Uniformity = \frac{1}{n} \sum_{l=1}^{n} R_{i,l} \times 100\% \tag{3}$$

with $R_{i,l}$ is the l-th binary bit of an n-bit response from a chip i.

Bit-aliasing : Bitaliasing denotes the existence of systematic biases in the distribution of binary digits (1s and 0s) within the output of a PUF. Bitaliasing serves as a metric similar to uniformity, but it is evaluated on a per-challenge basis, as illustrated in the equation (4).

$$Bit - aliasing = \frac{1}{k} \sum_{l=1}^{k} R_{l,i} \times 100\% \tag{4}$$

with k = the number of PUFs devices, l = the index of the bit in the PUF identifier, Rl,i = the value of the l-th bit in the response of the i-th PUF device.

Several types of PUFs have been proposed in literature [12] [13]. Among them, RO-based PUFs [14] can be used for key generation. The operating principle of RO-based PUFs (Fig. 1.) is as follows : a challenge is presented to the multiplexers that select a pair of ring oscillators. The counter then counts the number of oscillations, and a comparison is made at the end to provide an output (1 or 0). This structure is repeated as many times as the number of bits required in the PUF output, as depicted in Figure 1. This work focuses on the ring oscillators PUF.

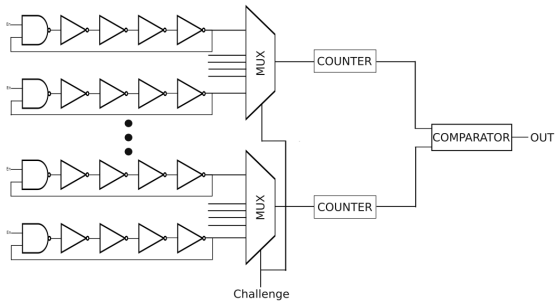


Fig. 1: Schematic of ring oscillator PUF

B. *Temperature effect on RO-based PUF reliability*

As mentioned earlier, a ring oscillator PUF is composed of multiple ring oscillators. A ring oscillator is composed of an odd number of inverters connected in a loop, where the output of the last inverter is fed back to the input of the first one.

In practice, a ring oscillator includes a NAND gate with an additional input to enable or disable the oscillation in place of the first inverter.

The frequency of an ring oscillator depends on several factors such as temperature, circuit design, transistor characteristics, their operation, and the number of inverters, as shown in Eq. 5 [15].

$$F_{osc} = \frac{1}{2N(\tau pLH + \tau pHL)} \tag{5}$$

$$\tau pLH = 0.7 \frac{2L_p}{U_p Cox W_p (V_{SGp} - |V_{tp}|)} \frac{8}{3} Cox(W_p L_p + W_n L_n) \tag{6}$$

$$\tau pHL = 0.7 \frac{2L_n}{U_n Cox W_n (V_{GSn} - V_{tn})} \frac{8}{3} Cox(W_p L_p + W_n L_n) \tag{7}$$

where N = number of stages, W_p, L_p = Width and Length of PMOS transistor, W_n, L_n = Width and Length of NMOS transistor, U_n = electrons mobility, U_p = holes mobility, C_{ox} = oxide capacitance, V_{tp} = PMOS threshold voltage, V_{tn} = NMOS threshold voltage, V_{GSn} = NMOS gate-source voltage, V_{SGp} = PMOS gate-source voltage.

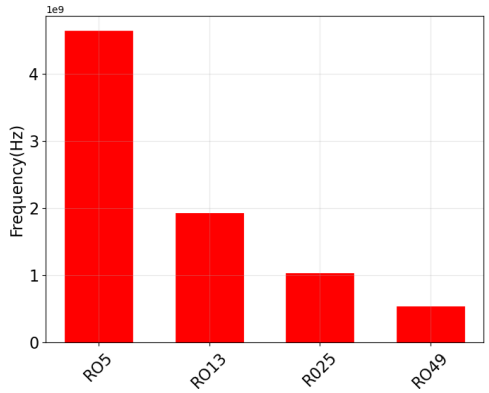


Fig. 2: Frequency of a ring oscillator according to the number of inverters used

Figure 2 shows the relationship between the frequency of a ring oscillator and its number of inverters. As the number of inverters increases, the frequency decreases significantly.

A PUF with ring oscillators whose frequencies are more separated from each other is more reliable [16]. Indeed, by increasing the temperature to certain levels, the ring oscillators become jittery, which significantly increases the likelihood of a bit flip in the PUF output.

Using simulations, we studied the frequency distributions of a ring oscillator with 5 inverters from ST Microelectronics' 65 nm technology in four different environments (27°C, 57°C, 107°C, 207°C) for 1000 different randomly generated threshold voltage values for each transistor. The results of the monte carlo simulation are visible in Figure 3.

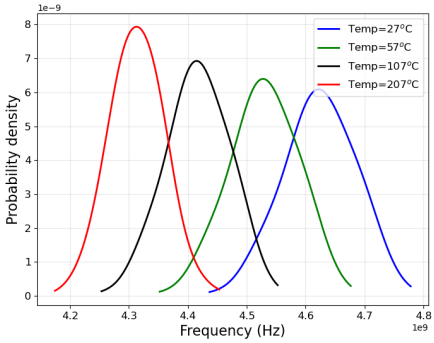


Fig. 3: Frequency distribution due to V_{TH} variability and temperature (5 inverters ring oscillator)

Figure 3 shows the effect of temperature on frequency distributions in ring oscillators. Under normal operating conditions, the frequency distribution follows a large normal distribution, meaning that the frequency values extend over a wider range of values. This reduces the probability of having ring oscillators that oscillate at the same frequency. As a consequence, this means that even with aging, these frequencies will be sufficiently far apart to avoid flippin the PUF output.
At higher temperatures (107°C and 207°C), the distributions are narrower, meaning that the frequencies are closer. This confirms that high temperatures pose a risk to ring oscillators because there is a greater chance of having ring oscillators with frequencies that are close enough together, making it easier for output flips and thus reducing reliability.

$$Frequency \simeq \mathcal{N}(\mu, \sigma^2) \tag{8}$$

With : $\mathcal{N}$ = normal distribution , μ = the mean and σ = the standard deviation.

TABLE I: Variation of the standard deviation of an ring oscillator as a function of temperature.

Temperature	Technology	Supply voltage	Mean (μ)	Standard deviation (σ)
27°C	65nm	1V	4.625 Ghz	58.39 Mhz
57°C	65nm	1V	4.530 Ghz	55.61 Mhz
107°C	65nm	1V	4.417 Ghz	51.36 Mhz
207°C	65nm	1V	4.313 Ghz	44.31 Mhz

Table I shows the evolution of the standard deviation and the mean according to temperature for a normal frequency distribution of a ring oscillator. As the temperature increases, the standard deviation decreases, indicating that the dispersion of the data around the mean is smaller. In other words, the data values are more tightly clustered around the mean and there is less variation in the data.

We repeated the same experiment on a 25-inverter ring oscillator instead of just 5 as in the first experiment. The goal is to see if the number of inverters can influence the effect of temperature on the distributions. The results are visible in Figure 4.

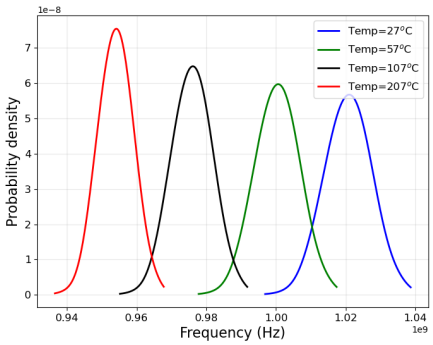


Fig. 4: Frequency distribution due to V_{TH} variability and temperature (25 inverters ring oscillator)

As with Figure 3, the frequency distributions become narrower as the temperature increases, leading to the same conclusions. This provides further confirmation on the impact of temperature on the reliability of ring oscillators, regardless of the number of inverter stages they include.

A normalized plot is shown in Figure 5 in order to understand the variation in standard deviation for different architectures, with 5, 13, 25 and 49 inverters. This allows us to observe that temperature affects the reliability of all ring oscillators in the same way.

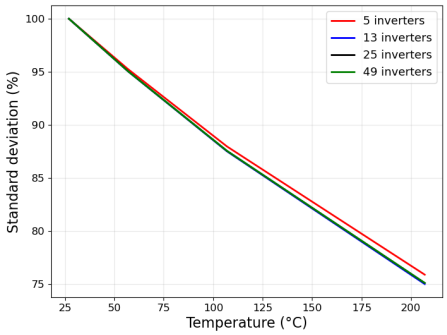


Fig. 5: Variation of the standard deviation as a function of temperature for different ring oscillators with different number of inverters

III. Temperature Attacks on RO-PUF

In the previous chapter, it was demonstrated that temperature can degrade the reliability of ring oscillators in a single chip. In this chapter, we will explore how temperature can be used to manipulate the frequencies of ring oscillators temporarily. This approach is relevant in situations where an attacker targets a single ring oscillator, leading to a change in the output of the PUF.

We studied the frequency shift of different ring oscillators with different numbers of inverter stages (5, 13, 25, 49) as a function of operating temperature varying from 27°C to 250°C. In the Table II, we summarize the decrease rate of frequency for different ring oscillators.

TABLE II: Rate of frequency decrease of ring oscillators as a function of temperature

Ring Oscillator	Technology	Supply voltage	Rate of frequency degradation(%)
5 inverters	65nm	1V	6.74
13 inverters	65nm	1V	6.831
25 inverters	65nm	1V	6.830
49 inverters	65nm	1V	6.830

Table II demonstrates that the rate of decrease is practically the same regardless of the number of inverters used, confirming that the frequency drop in temperature is independent of the number of inverters used.

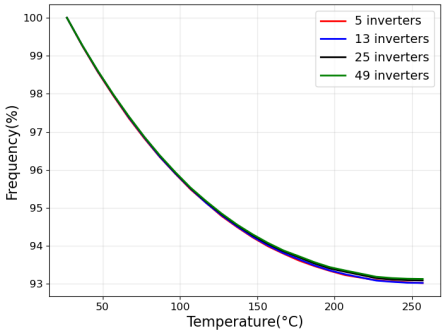


Fig. 6: Frequency variation as a function of temperature for differents RO sizes

Figure 6 displays the variation of oscillation frequency as a function of temperature. The results indicate a sharp decrease until 150°C, followed by a sort of stabilization or slight decrease in frequency until 250°C, for all configurations. This phenomenon is independent of the number of inverter used.

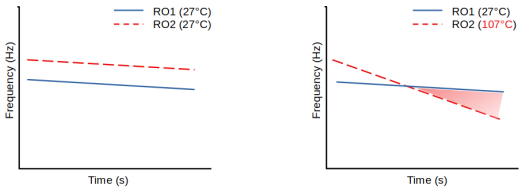


Fig. 7: Attack technique on a ring oscillator PUF

Figure 7 shows how temperature can be used to change the behavior of a ring oscillator. From an attacker's perspective, they can target a specific ring oscillator to decrease its frequency and consequently reverse the output of the PUF.

As seen in Equation 5, the frequency of a ring oscillator depends on several parameters: apart from the number of inverters, threshold voltage and mobility are the other two important parameters. Therefore, it is important to understand how temperature affects the threshold voltages of PMOS and NMOS transistors and the mobility.

Figure 8 plots the variation of threshold voltages as a function of temperature. It shows that the absolute value of the threshold voltages of the two transistors that make up

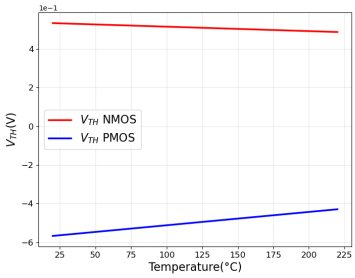


Fig. 8: Evolution of the threshold voltage for both NMOS and PMOS transistors in an CMOS inverter as a function of temperature

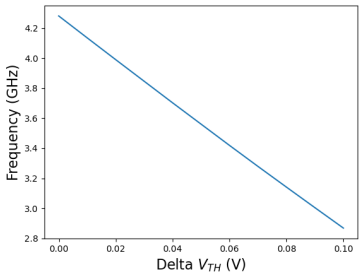


Fig. 9: Evolution of RO oscillator frequency as function of threshold voltage

an inverter (NMOS and PMOS) decreases with increasing temperature. The threshold voltages of PMOS and NMOS can be respectively modeled by equations 9 and 10 [17]. The decrease in the absolute value of the threshold voltages, can be attributed to the shift in Fermi level and band gap energy [18] [19].

$$V_{thp} = V_{thp0} - \gamma \left(\sqrt{2\phi_f + V_S - V_{sub}} - \sqrt{2\phi_f} \right) \quad (9)$$

$$V_{thn} = V_{thn0} + \gamma \left(\sqrt{2\phi_f + V_S - V_{sub}} - \sqrt{2\phi_f} \right) \quad (10)$$

With : V_{thp} = the threshold voltage of the PMOS, V_{thp0} = the intrinsic threshold voltage of the PMOS, V_{thn} = the threshold voltage of the NMOS, V_{thn0} = the intrinsic threshold voltage of the NMOS, γ = a technology-dependent parameter that describes the sensitivity of the threshold voltage to variations in transistor geometry and fabrication parameters, ϕ_f = the Fermi potential of the silicon substrate, V_S = the source voltage, V_{sub} = the absolute value of the substrate voltage.

$$\phi_f = \pm \frac{kT}{q} \ln \left(\frac{N_{sub}}{N_i} \right) \quad (11)$$

With : k = the Boltzmann constant, T = the absolute temperature in Kelvin, q = the elementary charge, N_{sub} = doping concentration of the substrate, N_i = the intrinsic carrier density of the semiconductor material.

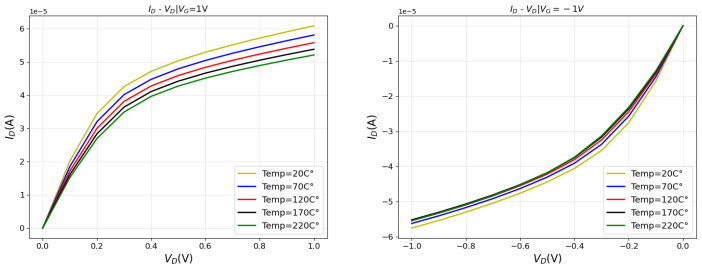
However, simulations show that the decrease in frequency cannot be attributed solely to the effect of transistor threshold voltages, as even increasing the absolute value of these voltages does not prevent the frequency from decreasing (Figure 9).

In [20], the authors explain that the variation of carrier mobility with temperature dominates the propagation, and delay variations in circuits operating at the nominal supply voltage for 65 nm CMOS technologies.

For these reasons, we studied the effects of temperature on the drain current of both NMOS and PMOS transistors in order to better understand how it is affected by temperature, and because mobility is directly related to drain current Eq. 12. These findings are presented in Figure 10, which shows a decrease in drain current as a function of temperature for both NMOS and PMOS transistors.

$$I_D = \frac{W}{L} U_0 C_{OX} (V_G - V_T - \frac{V_D}{2}) V_D \quad (12)$$

With : W = width, L = length, U_0 = carriers mobility, V_G = gate voltage, V_T = threshold voltage, V_D= drain voltage.



(a) (b)

Fig. 10: Evolution of the drain current of NMOS (a) and PMOS (b) as a function of temperature

Figure 10 shows that the drain current I_D of transistors decreases with increasing temperature. This phenomenon is due to the fact that at high temperatures, charge carriers become more energetic, increasing the probability of collisions among them, which decreases mobility and consequently the current.

IV. Controlled and Localised Aging

In the previous chapters, the impact of temperature on the reliability of RO PUFs was explored. It was found that temperature can pose a significant threat to the proper functioning of these circuits. In addition, it was demonstrated that temperature can be utilized to modify the characteristics of the transistors that make up the PUF, leading to changes in its frequency and response.

While the effects of temperature are typically transient, in some cases, it may be desirable to achieve permanent modifications to the transistor characteristics. In such scenarios, temperature can be used to accelerate the effects of aging. Aging can have an impact on all types of circuits, including PUFs [21] [22] [23]. This impact tends to develop over time

and with prolonged usage, and it can negatively affect the performance and functionality of these circuits. Typically, aging effects become noticeable after several years of usage, leading to an increase in the threshold voltage of transistors, a decrease in current, and an increase in leakage current. Additionally, aging can cause increased energy consumption and a decrease in the lifespan of the device. Temperature and power supply voltages are examples of factors that can accelerate aging [24]. Aging phenomena can be classified into two groups : effects that cause catastrophic failures of devices, such as time-dependent gate oxide breakdown (TDDB) or electromigration (EM), and effects that cause drift of device parameters, such as bias temperature instabilities (BTI) and hot-carrier injection (HCI) [25].

TABLE III: Description of 4 important aging effects

Aging effect	Target	Effect
BTI	NMOS and PMOS	Increase in threshold voltage and threshold voltage variation
HCI	NMOS	Decrease in charge carrier mobility and threshold voltage degradation
EM	Interconnexions	Curvature of conductors and opening of electrical interruptions
TDDB	Gate oxide	Increased electrical leakage and dielectric defects

However, in most current chips, there are temperature sensors that can detect high temperatures and therefore compromise this type of attack. One possible approach would be to modify the characteristics of the circuits even when they are turned off. This would allow injecting errors into the PUFs without being detected by the sensors. Our future work will be devoted to the in-depth study of this question.

V. Conclusions

Ring oscillators are essential components in many electronic circuits, including security and cryptography systems. However, it has been demonstrated that the frequencies of ring oscillators are sensitive to high temperatures, which can make these circuits vulnerable to fault injection attacks through temperature. These attacks aim to recover encryption keys by disrupting the normal operation of the circuit.

Fortunately, these attacks at high temperatures typically occur when the circuits are powered on, which means that countermeasures can be put in place to detect them. Hardware and software redundancy is one such countermeasure, which involves using additional components to monitor the circuit's operation and detect any anomalies.

However, new potential threats to the security of electronic circuits are emerging over time. In the future, we will focus on the feasibility of fault injection attacks on powered-off circuits. If this method is possible, attackers could modify the behavior of a Physically Unclonable Function (PUF) even if it is powered off, making the attack extremely difficult to detect. This perspective represents a real challenge for the security of electronic systems and will be an important area of research in the years to come.

VI. Acknowledgement

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