Noise Margin, Critical Charge and Power-Delay Tradeoffs for SRAM Design

Aravind Rajendran, Yuriy Shiyanovskii, Frank Wolff, Chris Papachristou
Case Western Reserve University
Cleveland, Ohio 44106, USA
{axr264, yxs32, fxw12, cap2}@case.edu

***Abstract*—Aggressive technology scaling has resulted in stability reduction for classic SRAM designs. This is especially problematic for large integrated circuits. The stability of SRAM cells can be affected by noise during a read operation and by radiation during the standby mode. In this paper, we present an approach to address the gradual stability reduction in SRAM designs. We present an SRAM design tradeoffs approach to improve the characteristics of SRAM by modulating the transistor sizing ratio, β. We test our approach on various SRAM designs in $32nm$ technology. We optimize the SRAM designs with β for various constraints in power consumption, performance, radiation tolerance and data stability. We discuss different design trends produced by the extensive approach analysis.**

I. Introduction

Static random access memories (SRAM) have been used as on-chip memories in high performance integrated circuits, due to its high access speed and compatibility with process and supply voltage. The demand for high performance due to aggressive CMOS technology scaling has increased the amount of on-chip memory integrated into modern semiconductor devices. The total area occupied by these memories has been rapidly increasing and reached over 70% [1]. The continued scaling of CMOS technology has also resulted in problems which were less severe in earlier generations. These include process induced variations, soft errors, transistor degradation mechanisms etc.

SRAMs dominate the memory hierarchy in performance but they are often integrated in lesser capacity due to the area limitations and the high cost per bit. Furthermore, as the technology scales deeper into nanometer levels, the stability of SRAM to noise and radiation is reduced. It is becoming increasingly challenging to maintain an acceptable static noise margin (SNM) of SRAMs while scaling the minimum feature sizes and supply voltage [1], [2]. Static noise margin (SNM) degradation, which characterizes the data integrity of SRAM during a read operation [3], has driven the development of SRAM cell design in to new direction as the supply voltage reaches near the threshold voltage. Moreover, the shrinking of the transistor dimensions has also increased the probability of radiation induced errors [4], [5].

In order to improve the overall performance of large systems, large arrays of minimum sized SRAMs are often integrated into the chip. However, this method will effect the reliable operation of the memory cells. These reliability issues have resulted in design constraint relaxation in terms of overall area. The performance characteristics of a regular SRAM cell in $32nm$ technology are presented in figure 1. The plot shows the dependence of SNM to the β-ratio (pull-down to access transistor sizing ratio) of the SRAM. Although the SRAM cell performs well in the minimum dimensions, it has disadvantages in terms of SNM and critical charge, Q_{crit}. The SRAM cells shows improved SNM and Q_{crit} at a higher β-ratio.

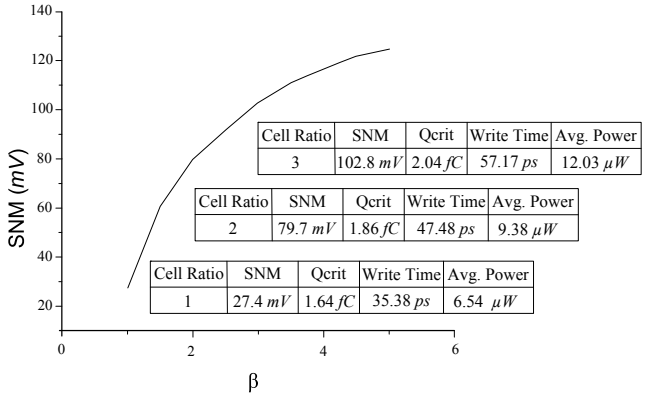

Fig. 1. Characteristics of SRAM in $32nm$ Technology

In this paper, we present an SRAM design tradeoffs to improve its performance characteristics by modulating the transistor sizing ratio, β. We apply this approach for different SRAM cells to produce good tradeoff driven by the parameters:- SNM, critical charge, write time delay and power consumption. Furthermore, we focus on optimizing the SNM while satisfying the other design constraints.

This paper has the following outline. In Section II. we present background information on SRAM stability. In section III. we describe our SRAM design tradeoffs approach to improve the characteristics of SRAM by modulating the transistor sizing ratio. In section IV, we present our simulations and discuss our results. The paper concludes in section V.

II. Background

Stability and robustness of an SRAM is characterized by its ability to retain stored data. The stability of the memory cell can be affected during read or stand by mode. The disturbance produced during the read operation, read access disturbance, influences the cell stability during read mode. During the

stand by mode, the stability of SRAM is affected by radiation induced errors.

Fig. 2 shows the classic six transistor SRAM cell (6T-SRAM) with worst case noise sources added between the storage nodes [6], [3]. The static noise margin (SNM) metric, that is used to quantify stability of SRAM during the read mode, represents the the maximum value of DC noise voltage (V_n) required to flip the stored bit [3], [7] .

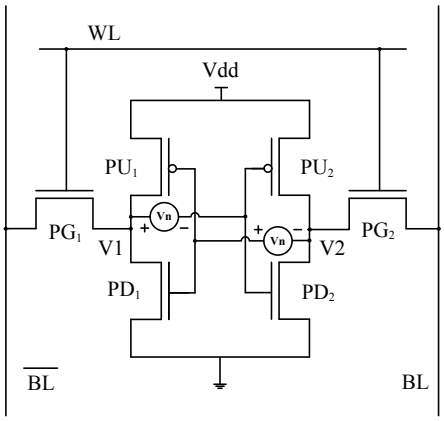

Fig. 2. 6T-SRAM with worst-case noise sources

A. Static Noise Margin

The stability of an SRAM cell is an important functional constraint in nanometer technologies as it determines the ability to retain stored information. The static noise margin (SNM), both during a read access and in standby mode, is a measure of the stability and it is defined as the maximum static noise voltage that can be tolerated by the SRAM without losing the stored information [7], [3].

The cell is most vulnerable to noise during a read access than the standby mode because the pre-charged bit-lines ($BL, \overline{BL}$), connected to the storage nodes, increases the potential at '0' storage node. The voltage divider formed between the access transistor (PG) and the pull-down transistor (PD) determines the voltage rise at the node and it depends on the strength of the transistors. Since, the strength of the transistor is determined by its dimensions the access transistor and pull-down transistor can be carefully sized to control the rise in the node voltage. This ratio is called β-ratio.

$$\beta = \frac{W_{PD}/L_{PD}}{W_{PG}/L_{PG}} \tag{1}$$

where $W_{PD}, L_{PD}, W_{PG}, L_{PG}$ are the width and length of the pull down and access transistors respectively.

The SNM of an SRAM cell can be represented graphically using the superimposed voltage transfer characteristics (VTC) of the inverters as shown in Fig. 3. The resulting two-lobed curve is generally referred to as the '*butterfly curve*'. The area inside the two lobes is a measure of the sensitivity of SRAM cell to noises and the the side of the maximum possible nested square between the curves represents the SNM of that memory cell [3]. The process variation changes in transistor attributes (length, width, oxide thickness, mobility etc.) may affect the symmetry of the VTCs. As a result, the cell shows reduced SNM levels, which is more susceptible to losing one particular data value.

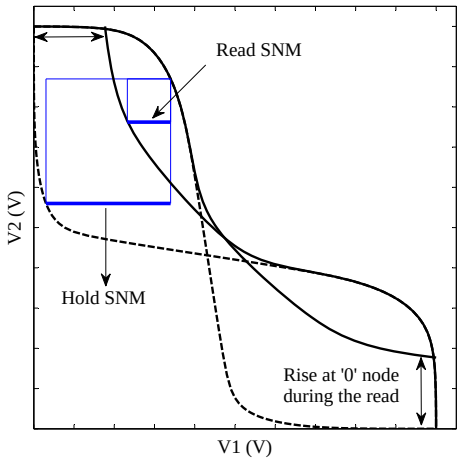

Fig. 3. VTCs of SRAM cell in the read mode and in the standby mode

The dotted lines in Fig. 3 represents the DC characteristics of the cell during standby mode while the thick lines represents the VTCs during a read access. Fig. 3 also shows the change in the VTC during a read access and the decrease in SNM from standby mode to read access. The SRAM cell has different noise immunity levels during read and hold operation. Since, the SNM is significantly degraded during the read operation, we focus on the SNM during that period. The SNM of the cell can be improved by varying the sizing ratio of transistors, threshold voltage (V_{th}), supply voltage (V_{dd}). It can be also improved by decreasing the read time or modulating the word-line voltage [2]. We consider a transistor width modulation approach to improve the SNM of the SRAM in this work.

B. Critical Charge

A Single Event Upset (SEU) in an SRAM cell occurs when a charged particle strikes a sensitive node and flips the state of the SRAM cell, causing a soft error. The high energy neutrons from cosmic radiation are the primary source for soft errors in modern ICs [5]. In a 6T-SRAM cell the reverse-biased junctions between the drain and substrate are more sensitive to SEU, caused by ionizing particles, particularly at the node storing a logic high [8]. The sensitivity of an SRAM to radiation is quantified by critical charge parameter, Q_{crit}, as the amount of charge required to change the state of the cell [5]. Q_{crit} primarily depends on operating voltage, node capacitance, and the strength of feedback transistors [4], [9].

At nanometer technologies the supply voltage cannot be used as a way to improve the critical charge due to the low power requirements. Another way to improve the critical charge of the cell is radiation hardening, where the transistor widths are increased to achieve higher node capacitance.

However, this may not improve the SNM significantly as the β-ratio is unaffected [10].

III. Stability Improvement - Approach

We present an SRAM design tradeoffs approach to improve the characteristics of SRAM by modulating the transistor sizing ratio, β. It is one of the main driving forces to improve the SNM of SRAM devices as the variation in β-ratio from 1 to 3 can significantly improve the SNM of the SRAM cell. We use this property of SRAM to improve its stability along with its other SRAM characteristics such as the Q_{crit}, the write performance and the power consumption. However, the desired SRAM design is characterized by a set of quadruple values concerning the SNM, Q_{crit}, write time (W_{time}) and power consumption. Note the Q_{crit} and the power consumption increase as the total area of the SRAM cell increases. At the same time, the SNM improves by increasing the ratios of the transistors, β, within the cell. Thus an increase in β-ratio results in an improved SNM and Q_{crit} at the expense of the write time and power consumption.

To motivate this point, consider Table I which shows a fragment of experimentally derived basic 6T-SRAM cells as the β-ratio varies from 1 to 3. It is clear from this table that the SNM improves more than 2x as the β-ratio of SRAM changes from 1 to 3. Every design version is associated by its β and characterized by the quadruple set of parameters, i.e. the SNM in mV, Q_{crit} in fC, W_{time} in ps and the power consumption in μW. In this work, the preferred parameter to optimize is the SNM. However, consideration should also be given to the other three parameters, Q_{crit}, W_{time}, and power. Our approach is to use the last parameters as design constraints to be satisfied while SNM undergoing optimization improvements. For example, if $Q_{crit} \geq 1.7fC$ then all SNM with for $\beta \geq 1.5$ would satisfy the critical charge. Moreover, if $W_{time} \leq 48ps$ and Power $\leq 10\mu W$ then the corresponding SNM with $\beta \leq 2$ will satisfy these constraints. Overall for $1.5 \leq \beta \leq 2$ all constraints would be satisfied which means values between 60.7 to 79.7 mV optimize SNM under the designer constraints.

This constraint driven tradeoff process can be generalized as follows. Suppose $\mathcal{B} = \{\beta_1, \beta_2, \beta_3, ...\}$ is the set of β-ratios for design versions 1, 2, 3, ..., respectively, derived by experimentation. Let $Q_{min}, T_{max}, P_{max}$ be the critical charge, write time and power constraint values. That is, for indices q, t, p in $\{1, 2, 3, ...\}$ let β_q, β_t, β_p be corresponding subsets in $\mathcal{B}$, then we have the following constraint relations

$$\begin{aligned} Q(\beta_q) \geq Q_{min} \geq Q(\beta_{q-1}) \\ T(\beta_t) \leq T_{max} \leq T(\beta_{t+1}) \\ P(\beta_p) \leq P_{max} \leq P(\beta_{p+1}) \end{aligned}$$

where $Q(\beta_q)$, $T(\beta_t)$ and $P(\beta_p)$ are the critical charge, time delay and power for SRAM versions q, t and p, respectively. Suppose now the solution to the above constraints are the following $beta$ subsets, respectively, $\mathcal{B}_Q = \{\beta_q, \beta_{q+1}, ...\}$, $\mathcal{B}_T = \{\beta_t, \beta_{t-1}, ...\}$ and $\mathcal{B}_P = \{\beta_p, \beta_{p-1}, ...\}$. Then the tradeoff solution satisfying all constraints can be expressed by the β subset intersections

$$\mathcal{B}_{all} = \mathcal{B}_Q \cap \mathcal{B}_T \cap \mathcal{B}_P$$

where the β elements of $\mathcal{B}_{all}$ provide the corresponding improved SNM tradeoff values (see Table I) that satisfy the above constraints. However, since all parameter values in Table I grow monotonically, we can express our tradeoff solution in terms simpler than the subset intersections using the previous constraint values for β, i.e. β_q, β_t and β_p. Thus all β_i points satisfying the following relation

$$\beta_q \leq \beta_i \leq min\{\beta_t, \beta_p\}$$

satisfy the constraints. Note these β_i points are contiguous in the table such as Table I, meaning that they lie within β_q and $min\{\beta_t, \beta_p\}$. However, if $\beta_q > min\{\beta_t, \beta_p\}$ then there is no solution satisfying the designer constraints. For the previous example, $\beta_q = 1.5$, $\beta_t = 2$, $\beta_p = 2$ and $\beta_q \leq \beta \leq min\{\beta_t, \beta_p\}$, which yields $1.5 \leq \beta \leq 2$, or $\beta = \{1.5, 2\}$.

	β-ratio				
	1	1.5	2	2.5	3
SNM (mV)	27.4	60.7	79.7	91.9	102.8
$Q_{crit}(fC)$	1.64	1.75	1.86	1.95	2.04
$W_{time}(ps)$	35.38	42.25	47.48	52.17	57.17
Power (μW)	6.54	7.96	9.38	10.72	12.04

TABLE I
Characteristics of a 6T-SRAM cell with a variation in β-ratio in $32nm$ Technology

IV. Simulation and results

In our simulations, we first determined the SNM of the 6T-SRAM cell during a read access and then we measured the Q_{crit}, write time and power consumption. We calculated the set of characteristics for the 6T-SRAM cell while varying transistor sizing ratio, β.

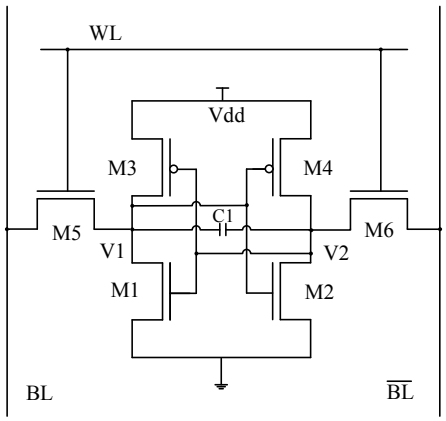

Fig. 4. Capacitor based SRAM

We explored three additional SRAM designs:- SRAM-C, SRAM-T, SRAM-NSP to find the good tradeoff points between SNM, Q_{crit}, Write time delay and power consumption. We considered these designs to show that this method is applicable to different SRAM cells and architectures. The SRAM-C design, shown in Fig. 4, uses a capacitor between the nodes to increase the overall capacitance of the cell, thus enhancing radiation immunity [11]. The SRAM-T design proposed in [12], uses modified tristate inverters connected to the storage nodes in order to protect the cell from soft errors during the standby mode, as shown in Fig. 5. The modified tristate inverters are partially disconnected from the storage cell during other modes of operation (read/write). The final design we considered for our approach is the SRAM-NSP cell proposed in [13]. In this design, as shown in Fig 6, the capacitor is connected to the storage nodes during the standby mode. However, the capacitor is disconnected during write operation to reduce the impact on write performance.

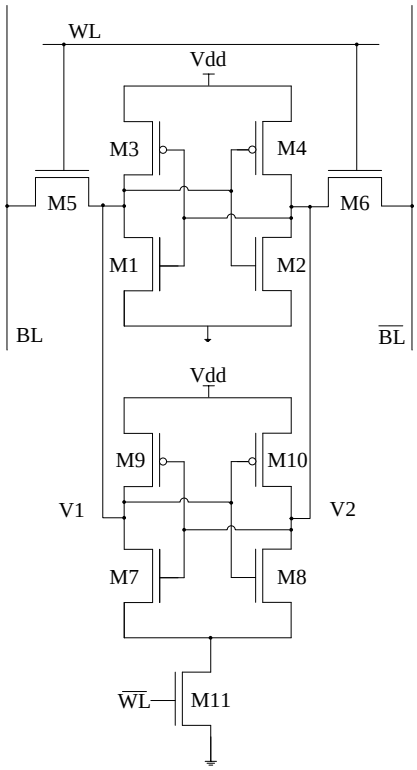

Fig. 5. Tristate SRAM cell (SRAMT) [12]

To analyze the stability of SRAM cell during a read access we generated voltage transfer characteristics (VTC) of its inverters during for that condition. SNM of the SRAM is calculated using the method described in [3]. According to this method, the area inside the two lobes is a measure of the sensitivity of SRAM cell to noise. The side of the maximum possible nested square between the curves represents the SNM of that memory cell. Figure 3 shows the superimposed inverter VTCs of the SRAM cell during a read access, that are inversed from each other. The solid line in the figure represents the butterfly curve for an SRAM cell during a read operation.

The simulations of the SRAM cells are performed for minimum device features. To achieve this we used transistors with minimum length, $L_{min} = 2\lambda$, and minimum width, $W_{min} = 4\lambda$, where λ is the minimum feature size of a particular technology node. Further more, we used the pull-down and pull up transistors sizing such that it meets the condition $W_{PD} > W_{PG} > W_{PU}$, where W_{PD}, W_{PG}, W_{PU} are the transistor widths of pull-down (PD), pass-gate (PG) and pull-up transistors (PU) respectively. The sizing of the transistor are chosen in such a way that it meets the write margin and SNM conditions. According to this, we used $W_{PD} = 6\lambda$, $W_{PG} = 6\lambda$ and $W_{PU} = 4\lambda$ for the minimum size SRAM. The SRAM6T, SRAM-C, SRAM-T, SRAM-NSP cells are designed for $32nm$ process technologies using the Berkeley Predictive Technology Model (BPTM) data for bulk CMOS [14]. The simulations are performed using HSPICE while keeping the supply voltage (V_{dd}) constant at 1.0V.

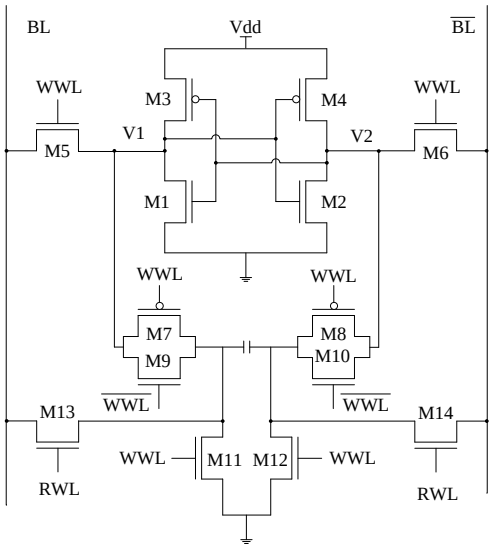

Fig. 6. SRAM-NSP cell with separate read port [13]

Keeping the process technology and supply voltage constant, we performed stability analysis of the four SRAM designs. During this analysis we varied the transistor sizing ratio, (β). We performed stability tests of the SRAM cells for the variation in transistor sizing ratios keeping the same process technology and supply voltage V_{dd}. We also measured the reliability, write performance, and power consumption of the SRAM cells for each β ratio. We quantified the critical charge of the node as the measure of the reliability due to soft errors. The critical charge of the node is determined by injecting a current pulse, I_{crit} [12], enough to flip the data, as shown in Figure 7. A commonly used analytical model for the current pulse has a double exponential form [12], [5]. The critical charge is calculated by integrating the current pulse over time. Since the charge required for 1-0 transition is lesser than the 0-1 transition, we considered the '1' storage node for

current injection. The write performance is calculated as the time required to change $10 - 90\%$ of the node voltage. For power consumption measurements, we considered the average power taken during a write operation.

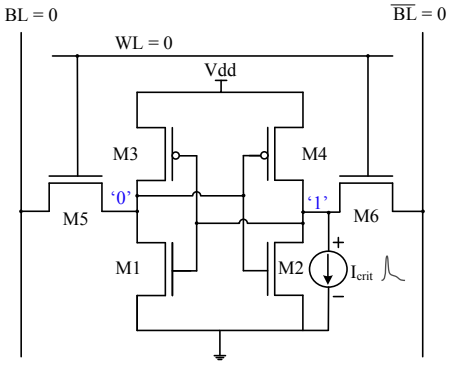

Fig. 7. Q_{crit} simulation setup

The goal of this approach is to use tradeoffs between SRAM characteristics within performance constraints to enhance the particular SRAM design. The constraints we considered are critical charge, write time delay, and power consumption. The choice of the good tradeoff points is determined by the SNM level of the required application. Normally these requirements will come from an industrial design process.

Design	β	SNM (mV)	Q_{crit} (fC)	Delay (ps)	Power (μW)
6T-SRAM	1	27.40	1.64	35.38	6.54
	1.2	45.00	1.69	37.39	7.09
	1.4	54.40	1.70	40.54	7.67
	1.6	64.60	1.73	43.44	8.27
	1.8	72.40	1.81	45.37	8.83
	2	**79.70**	**1.86**	**47.48**	**9.38**
	2.2	84.10	1.89	49.32	9.92
	2.4	91.00	1.93	51.21	10.46
	2.6	94.60	1.97	53.14	10.99
	2.8	98.30	2.01	55.18	11.51
	3	102.80	2.04	57.17	12.03

TABLE II
PERFORMANCE CHARACTERISTICS OF 6T-SRAM CELL IN $32nm$ TECHNOLOGY AT $V_{dd} = 1V$

In the case of a 6T-SRAM cell the SNM levels are significantly degraded during a read access. Table II shows the characteristics of 6T-SRAM cell in $32nm$ technology. A careful choice of β-ratio is important to achieve a better SNM levels for the cell. At the same time, the other performance characteristics of the cell will change with an increase in β-ratio. The selection of the β-ratio is determined by its impacts on write time delay and power versus area footprint of the cell. Suppose the requirements of the desired design version is restricted by the following design constraints

$$Q_{min} = 1.7fC, T_{max} = 48ps, P_{max} = 10\mu W$$

The choice of the SNM levels should satisfy all of the constraints listed above. For performance requirement, $P_{max} = 10\mu W$ all 6T-SRAM designs for β = 1 to 2 satisfy the performance requirements. For critical charge requirement of $Q_{min} = 1.7fC$ all 6T-SRAM designs for β above 1.6 satisfy the requirement. For write performance requirement of $T_{max} = 48ps$ all 6T-SRAM designs for β = 1 to 2.2 satisfy the requirement. Applying all the constraints requirements on the previously mentioned design versions, we attain a smaller set of design versions for 6T-SRAM cell with β between 1 to 2.

Design	β	SNM (mV)	Q_{crit} (fC)	Delay (ps)	Power (μW)
SRAM-C	1	27.40	5.97	247.30	47.24
	1.2	45.00	5.95	250.11	47.84
	1.4	54.40	5.91	250.05	48.44
	1.6	64.60	5.92	254.04	49.01
	1.8	72.40	5.99	254.59	49.52
	2	79.70	6.02	256.00	50.02
	2.2	**84.10**	**6.05**	**257.97**	**50.49**
	2.4	91.00	6.08	262.39	50.94
	2.6	94.60	6.10	264.47	51.37
	2.8	98.30	6.12	265.04	51.92
	3	102.80	6.15	268.25	52.44

TABLE III
PERFORMANCE CHARACTERISTICS OF SRAM-C CELL IN $32nm$ TECHNOLOGY AT $V_{dd} = 1V$

For the another scenario, we considered the SRAM-C cell. In SRAM-C design, the capacitor is connected between the nodes causes a large delay during the write operation. The rest of the SRAM-C architecture is similar to the 6T-SRAM cell. It is interesting to note that the performance characteristics of this cell increase uniformly with an incremental β, as shown in Table III. Suppose the choice of SNM is driven by the following design requirements

$$Q_{min} = 6fC, T_{max} = 260ps, P_{max} = 52\mu W$$

For performance requirements, $Q_{min} = 6fC$, $T_{max} = 260ps$, $P_{max} = 52\mu W$ all SRAM-C design versions for β = 2 to 2.2 satisfy the requirements.

The SNM of the SRAM-T cells can be optimized for the β-ratio between 1.6 and 1.8 for the performance constraints shown below.

$$Q_{min} = 3.3fC, T_{max} = 50ps, P_{max} = 15\mu W$$

Table IV shows the SRAM-T design versions for the different transistor sizing ratio, β. It also follows the trend of incremental change in the design constraints as β increases.

The trend in the performance characteristics of the SRAM-

Design	β	SNM (mV)	Q_{crit} (fC)	Delay (ps)	Power (μW)
SRAM-T	1	177.40	3.16	38.38	12.33
	1.2	185.40	3.21	39.68	13.01
	1.4	192.70	3.26	41.31	13.67
	1.6	199.90	3.31	42.76	14.31
	1.8	**206.70**	**3.35**	**43.64**	**14.97**
	2	211.10	3.40	45.17	15.59
	2.2	214.70	3.44	46.74	16.24
	2.4	219.00	3.48	48.53	16.89
	2.6	223.50	3.41	49.95	17.52
	2.8	225.60	3.56	51.28	18.15
	3	229.00	3.60	52.66	18.78

TABLE IV
PERFORMANCE CHARACTERISTICS OF SRAM-T CELL IN $32nm$ TECHNOLOGY AT $V_{dd} = 1V$

Design	β	SNM (mV)	Q_{crit} (fC)	Delay (ps)	Power (μW)
SRAM-NSP	1	112.10	7.36	51.04	10.29
	1.2	121.10	7.40	53.19	10.86
	1.4	129.60	7.45	55.11	11.32
	1.6	135.30	7.49	56.07	11.83
	1.8	140.70	7.53	58.05	12.54
	2	**143.10**	**7.56**	**60.62**	**13.08**
	2.2	147.60	7.60	63.48	13.62
	2.4	150.40	7.64	66.34	14.14
	2.6	152.30	7.68	67.76	14.30
	2.8	154.30	7.71	70.12	15.14
	3	156.50	7.75	71.86	15.71

TABLE V
PERFORMANCE CHARACTERISTICS OF SRAM-NSP CELL IN $32nm$ TECHNOLOGY AT $V_{dd} = 1V$

NSP is presented in the Table V. SRAM-NSP cells show better SNM levels for the minimum β due a different read mechanism. The design has relatively high initial Q_{crit} levels because of the extra capacitor connected between the storage nodes. The choice of β-ratio between 1 and 2 satisfy the design constraints shown below.

$$Q_{min} = 6fC, T_{max} = 60ps, P_{max} = 15\mu W$$

We can see a similar trend of increase in Q_{crit}, write time, and power consumption across all the cells as we increase the β-ratio. This monotonic nature of the performance characteristics is a direct result of additional cell area, which influences the overall characteristics of the cell. We can also observe that the 6T-SRAM cell has the lowest SNM and Q_{crit} levels, while it has better write time performance and power savings. These observations can be attributed to the small transistor dimensions compared to other tested SRAM designs. The additional components in the other SRAM cells improve its Q_{crit} levels at the expense of write time delay and power consumption.

V. CONCLUSION

In this paper, we presented an SRAM design tradeoffs approach to improve the characteristics of SRAM by modulating the transistor sizing ratio, β. We explored the monotonic nature of the SRAM characteristics to improve the SNM. We optimized the SRAM designs with β for various constraints in power consumption, performance, radiation tolerance, and data stability. We discussed different design trends produced by the analysis of the tradeoff approach. We also showed that this approach can be applied to different SRAM designs.

This paper focuses on a small selection of tradeoffs for improving the SNM. We can foresee to extend this tradeoff approach to a more general design space exploration problem which encompasses leakage power, interconnect parasitics, layout area, degradation mechanisms, process parameter variations etc.

REFERENCES

[1] H. Yamauchi, "A discussion on sram circuit design trend in deeper nanometer-scale technologies," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 18, no. 5, pp. 763 –774, May 2010.

[2] B. Alorda, G. Torrens, S. Bota, and J. Segura, "Static and dynamic stability improvement strategies for 6t cmos low-power srams," in *Design, Automation and Test in Europe Conference Exhibition (DATE)*, 2010, pp. 429 –434.

[3] E. Seevinck, F. List, and J. Lohstroh, "Static-noise margin analysis of mos sram cells," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 5, pp. 748 – 754, Oct. 1987.

[4] R. Baumann, "Soft errors in advanced computer systems," *IEEE Design Test of Computers*, vol. 22, no. 3, pp. 258 – 266, may-june 2005.

[5] F. Wang and V. Agrawal, "Single event upset: An embedded tutorial," in *VLSID 2008. 21st International Conference on VLSI Design*, Jan. 2008, pp. 429–434.

[6] C. F. Hill, "Noise margin and noise immunity in logic circuits," *Microelectronics*, vol. 1, no. 4, pp. 16 – 21, 1968.

[7] J. Lohstroh, E. Seevinck, and J. de Groot, "Worst-case static noise margin criteria for logic circuits and their mathematical equivalence," *IEEE Journal of Solid-State Circuits*, vol. 18, no. 6, pp. 803 – 807, Dec. 1983.

[8] V. Degalahal, N. Vijaykrishnan, and M. Irwin, "Analyzing soft errors in leakage optimized sram design," in *Proceedings. 16th International Conference on VLSI Design*, 2003, pp. 227 – 233.

[9] J. Cazeaux, D. Rossi, M. Omana, C. Metra, and A. Chatterjee, "On transistor level gate sizing for increased robustness to transient faults," in *IOLTS 2005. 11th IEEE International On-Line Testing Symposium*, july 2005, pp. 23 – 28.

[10] G. Torrens, B. Alorda, S. Bota, and J. Segura, "Analysis of radiation-hardening techniques for 6t srams with structured layouts," in *Reliability Physics Symposium, 2009 IEEE International*, 2009, pp. 791 –795.

[11] M. Lysinger, F. Jacquet, M. Zamanian, D. McClure, P. Roche, N. Sahoo, and J. Russell, "A radiation hardened nano-power 8mb sram in 130nm cmos," *International Symposium on Quality Electronic Design*, vol. 0, pp. 23–29, 2008.

[12] Y. Shiyanovskii, F. Wolff, and C. Papachristou, "Sram cell design using tri-state devices for seu protection," in *IOLTS 2009. 15th IEEE International On-Line Testing Symposium*, 2009, pp. 114 –119.

[13] S. Lin, Y.-B. Kim, and F. Lombardi, "A novel hardened design of a cmos memory cell at 32nm," in *DFT '09. 24th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, 2009, pp. 58 –64.

[14] Y. Cao, T. Sato, M. Orshansky, D. Sylvester, and C. Hu, "New paradigm of predictive mosfet and interconnect modeling for early circuit simulation," in *CICC. Proceedings of the IEEE 2000 Custom Integrated Circuits Conference*, 2000, pp. 201–204.