Dual-Buck Arbitrary Voltage Divider with one Output having Reduced Ripples

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***Abstract*—In this paper, a dual-buck voltage divider is further studied to provide two arbitrary, instead of balanced, voltage outputs. The two voltage outputs can be the same or different and are robust against parameter drift. The low-frequency ripples in one output are significantly reduced by actively diverting low-frequency ripple currents away from the corresponding output. Note that these are achieved by designing an advanced controller, without changing the topology. The controller consists of a PI controller to split the voltage, a repetitive controller and a resonant controller to deal with the low-frequency ripples at different frequencies. Experimental results are presented to validate the effectiveness of the proposed strategy.**

***Index Terms*—Voltage divider, dual-buck, voltage ripples, harmonic current, DC microgrids.**

I. Introduction

The development of power electronics techniques has made the regulation of DC voltages become much more simple. As a result, DC systems are becoming more and more attractive. It is often an active voltage divider that is required in DC systems to divide the DC-bus voltage into two voltage levels that can be the same or different for loads with different voltage requirements [1], as shown in Fig. 1. A neutral line is then naturally formed so that, for example, inverters with unbalanced loads can be operated. Importantly, the neutral line also helps reduce leakage currents, which can cause high electromagnetic interference (EMI) emission and risks of electric shock if not well handled.

For such dividers, a widely-used solution is the half-bridge topology [2], [3], where only two active switches, one inductor and two small capacitors are required. As a result, it features with simple structure, low cost and high efficiency. However, since the two active switches are connected in series across the DC bus, the half-bridge divider suffers from shoot-through problems, which is a major killer to converters [4]. In order to overcome this problem, a dual-buck divider was proposed in [5], which has the inherent capability to avoid several fundamental problems caused by deadtime in standard two-level converters, e.g., the shoot-through [6], [7] and also the current and voltage distortion [8]. In this case, the performance of voltage dividers is significantly improved. Conventionally, the two voltages are controlled to be balanced [3], [5]. However, it is often essential to have two different DC voltages, which are required by the loads, as illustrated in Fig. 1.

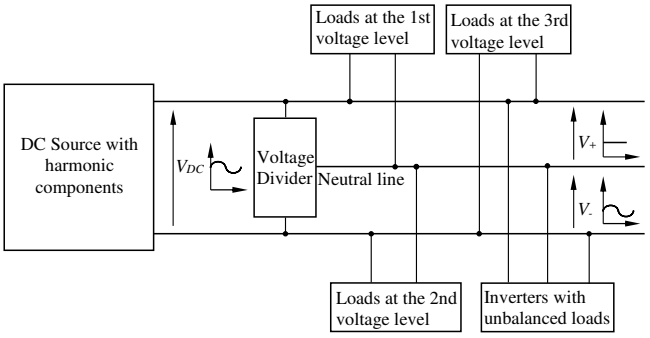


Fig. 1. A voltage divider in DC microgrids.

Apart from the unexplored DC, the AC ripples in low-frequency, for example, the well-known double-frequency ripples, of the two voltages could be a major concern, which has not been investigated as well. For instance, large low-frequency voltage ripples could considerably reduce the lifetime of PV, batteries and fuel cells [9]. In order to reduce such ripples, bulky electrolytic capacitors are often used, which, however, inevitably deteriorate system power density and reliability. In light of this, many types of active circuits without using bulky electrolytic capacitors have been proposed to divert harmonic currents away from voltages to reduce ripples; see [9] and the references therein. Such circuits can be added to voltage dividers but this will increase system complexity, cost, volume and weight.

In this paper, an advanced control strategy is proposed for the dual-buck voltage divider developed in [5] to arbitrarily

split the DC-bus voltage with one voltage having significantly-reduced low-frequency ripples so as to supply sensitive loads. After analyzing the paths of the low-frequency harmonic current, which may contain components at various frequencies [10], e.g., the 2nd, 3rd and 5th harmonics corresponding to the 50 Hz and/or 60 Hz fundamental frequencies of the power sources, it is found that the paths of the harmonic current can be diverted so that it only flows through one of the two output capacitors. The controller consists of a PI controller to split the DC-bus voltage, a repetitive controller and a resonant controller to handle harmonics at different frequencies at the same time so that the low-frequency voltage ripples can be reduced to the greatest extent. It is shown that the reduction of voltage ripples does not cause any problem to regulate DC levels of the two voltages. It is worth highlighting that no additional active switches or passive components are added to achieve the aforementioned functions. Experimental results are presented to validate the effectiveness of the proposed strategy.

II. Circuit Analysis

A. The Dual-buck Voltage Divider under Investigation

The dual-buck divider under investigation is shown in Fig. 2. It consists of two legs with their common point connected to the midpoint of the split DC capacitors C_+ and C_-. There are one active switch, one diode and one inductor for each leg: Q_1, D_1 and L_{N1} for the left leg, and Q_2, D_2 and L_{N2} for the right leg, respectively. The input of the divider is the DC-bus voltage V_{DC}, which possibly contains a certain level of ripples, and the outputs of the divider are the voltages V_+ and V_-, which are positive, with their sum equal to the input voltage V_{DC}. The voltages V_+ and V_- can be the same or different, as required by the loads connected across the output voltages V_+ and V_-. Loads with the appropriate voltage level can also be connected across the input voltage V_{DC}. Hence, there are three levels of DC voltages, i.e., V_+, V_- and V_{DC}.

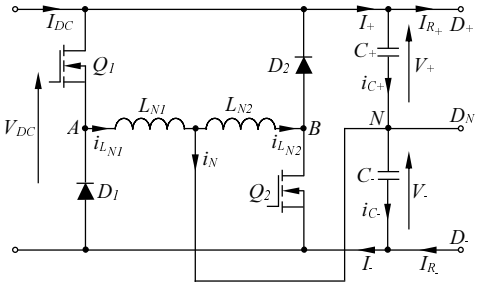


Fig. 2. The investigated dual-buck voltage divider proposed in [5].

As pointed out in [5], only one of the legs is operated to reduce losses. When the left leg is in operation, $i_N > 0$; when the right leg is driven, $i_N < 0$. When $i_N = 0$, none of the two legs is driven. The details on how to achieve this will be discussed in the Section III.

B. Average Circuit Model

According to [1], [11], the average circuit model of the divider can be built as shown in Fig. 3. A current source and a voltage source are used to replace the two switches in one leg, respectively. For example, the switch Q_1 is represented by a current source while the diode D_1 is represented by a voltage source. The currents flowing through the switch Q_1 and the diode D_1 can be given as

$$i_{Q_1} = i_{L_{N1}} d_1 \quad (1)$$
$$i_{D_1} = i_{L_{N1}}(1 - d_1) \quad (2)$$

where $i_{L_{N1}}$ is the current carried by the inductor L_{N1} and d_1 is the duty cycle of the switch Q_1. Similarly, the currents carried by the switch Q_2 and the diode D_2 can be given as

$$i_{Q_2} = i_{L_{N2}} d_2 \quad (3)$$
$$i_{D_2} = i_{L_{N2}}(1 - d_2) \quad (4)$$

where $i_{L_{N2}}$ is the current flowing through the inductor L_{N2} and d_2 is the duty cycle of the switch Q_2.

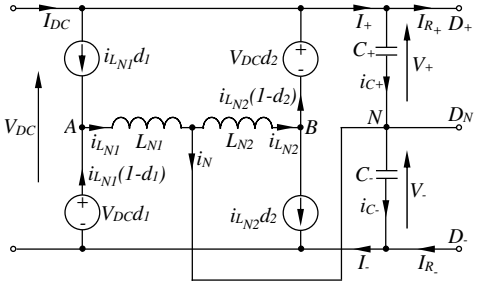


Fig. 3. Average circuit model of the dual-buck voltage divider.

When the left leg is operated, $i_N > 0$, and

$$d_1 = \frac{V_-}{V_{DC}} \quad (5)$$
$$d_2 = 0. \quad (6)$$

Substituting (5) and (6) into (1), (2), (3) and (4), there are

$$i_{Q_1} = \frac{V_-}{V_{DC}} i_{L_{N1}}$$
$$i_{D_1} = \frac{V_+}{V_{DC}} i_{L_{N1}}$$
$$i_{Q_2} = 0$$
$$i_{D_2} = 0.$$

When the right leg is operated, $i_N < 0$ and

$$d_1 = 0 \quad (7)$$
$$d_2 = \frac{V_+}{V_{DC}}. \quad (8)$$

Accordingly, there are

$$i_{Q_1} = 0$$
$$i_{D_1} = 0$$
$$i_{Q_2} = \frac{V_+}{V_{DC}} i_{L_{N2}}$$
$$i_{D_2} = \frac{V_-}{V_{DC}} i_{L_{N2}}.$$

When $i_N = 0$, both the left and right legs are not driven (i.e., $d_1 = 0$ and $d_2 = 0$) and, hence, $i_{Q_1} = i_{D_1} = i_{Q_2} = i_{D_2} = 0$.

C. The Paths of the Harmonic Current i_h

Depending on the input voltage V_{DC} and the loads, the input current I_{DC} may not be a pure DC but contains a certain level of harmonic components, which results in ripples in the output voltages V_+ and V_-. Without proper control, the harmonic current can flow through any of the switches, diodes, capacitors and/or loads of the divider, as detailed below:

- When the left leg is driven, $i_N > 0$ and the paths are shown by the red dashed lines in Fig. 4(a). The harmonic current i_h flows through the left leg, the capacitors and the loads. Because the current ripples i_h flow through the capacitors, voltage ripples appear at the outputs V_+ and V_-.
- When the right leg is driven, $i_N < 0$, and the paths of the current i_h are shown by the red dashed lines in Fig. 4(b). The harmonic current i_h now flows through the right leg, the capacitors and the loads. Again, voltage ripples appear at the outputs V_+ and V_-.
- When $i_N = 0$, no currents flow through either the left leg or the right leg. In this case, the harmonic current i_h only flows through the capacitors and the loads, which, of course, leads to voltage ripples at the outputs.

In order to reduce ripples in one of the two voltages, say V_+, all the ripple current i_h should be contained in i_N, as detailed below:

- When the left leg is driven, $i_N > 0$. The harmonic current i_h flows through the left leg, the capacitor C_- and the load R_-, as shown by the red dashed lines in Fig. 5(a). No ripple current flows through C_+ and hence there is no (low-frequency) voltage ripples in V_+.
- When the right leg is driven, $i_N < 0$. The harmonic current i_h flows through the right leg, the capacitor C_- and the load R_-, as shown by the red dashed lines in Fig. 5(b). No ripple current flows through C_+ and hence there is no (low-frequency) voltage ripples in V_+.
- When $i_N = 0$, no currents flow through either the left leg or the right leg. In this case, it also means there is no harmonic current i_h and, of course, there is no (low-frequency) voltage ripples in V_+.

Indeed, applying the Kirchhoff's current law to the average circuit model shown in Fig. 3, there are

$$\begin{aligned} i_{C_+} &= I_{DC} - i_{L_{N1}} d_1 + i_{L_{N2}}(1-d_2) - I_{R_+} && (9)\\ i_{L_{N1}} &= i_{L_{N2}} + I_{R_-} - I_{R_+} - i_{C_+} + i_{C_-} && (10)\\ i_N &= i_{L_{N1}} - i_{L_{N2}} && (11)\\ i_{C_-} &= i_{L_{N1}}(1-d_1) - i_{L_{N2}} d_2 - I_{R_-} + I_{DC}, && (12) \end{aligned}$$

where i_{C_+}, i_{C_-}, I_{R_+} and I_{R_-} are the currents flowing through the capacitors C_+ and C_-, and the loads R_+ and R_-, respectively.

When the left leg is operated, $i_{L_{N2}} = 0$ and $i_N > 0$. Then, (9), (10), (11) and (12) become

$$\begin{aligned} i_{C_+} &= I_{DC} - \frac{V_-}{V_{DC}} i_{L_{N1}} - I_{R_+} && (13)\\ i_{L_{N1}} &= I_{R_-} - I_{R_+} - i_{C_+} + i_{C_-} && (14)\\ i_N &= i_{L_{N1}} && (15)\\ i_{C_-} &= \frac{V_+}{V_{DC}} i_{L_{N1}} - I_{R_-} + I_{DC}. && (16) \end{aligned}$$

As a result, the capacitor current i_{C_+} becomes zero when

$$i_N = i_{L_{N1}} = \frac{V_{DC}}{V_-}(I_{DC} - I_{R_+}).$$

Then, (15) and (16) become

$$i_{C_-} = \frac{V_{DC}}{V_-} I_{DC} - \frac{V_+}{V_-} I_{R_+} - I_{R_-}. \quad (17)$$

In this case, the harmonic current i_h does not flow through the capacitor C_+ any more, as shown in Fig. 5(a).

When the right leg is operated, $i_N < 0$ and $i_{L_{N1}} = 0$. In this case, (9), (10), (11) and (12) can be re-written as

$$\begin{aligned} i_{C_+} &= I_{DC} + \frac{V_-}{V_{DC}} i_{L_{N2}} - I_{R_+} && (18)\\ -i_{L_{N2}} &= I_{R_-} - I_{R_+} - i_{C_+} + i_{C_-} && (19)\\ i_N &= -i_{L_{N2}} && (20)\\ i_{C_-} &= -\frac{V_+}{V_{DC}} i_{L_{N2}} - I_{R_-} + I_{DC}. && (21) \end{aligned}$$

When

$$i_{L_{N2}} = \frac{V_{DC}}{V_-}(I_{R_+} - I_{DC}),$$

$i_{C_+} = 0$ can be achieved. Then, (21) becomes

$$i_{C_-} = \frac{V_{DC}}{V_-} I_{DC} - \frac{V_+}{V_-} I_{R_+} - I_{R_-} \quad (22)$$

and the harmonic current path is shown by red dashed lines in Fig. 5(b). It does not flow through the capacitor C_+.

As a special case, $i_N = 0$ and $i_{C_+} = 0$ can only be achieved when $i_h = 0$. Otherwise, at least one of the legs is driven to achieve $i_{C_+} = 0$.

D. Arbitrary Split of the DC-bus Voltage

The regulation of the two voltage outputs can be achieved by controlling the left and right legs, i.e., to regulate the duty cycles d_1 and d_2, respectively. According to (5) and (8), $0 < d_1 < 1$ and $0 < d_2 < 1$ are always achievable because $V_+ < V_{DC}$ and $V_- < V_{DC}$. Hence, the DC-bus voltage V_{DC} can be arbitrarily split as V_+ and V_-. Note that although the ripples in the DC bus are all diverted to V_-, it does affect the voltage regulation.

III. Control Design

There are two control objectives, i.e., to split the DC-bus voltage arbitrarily into two voltage outputs and to divert the harmonic current away from the capacitor C_+ to reduce the ripples in V_+.

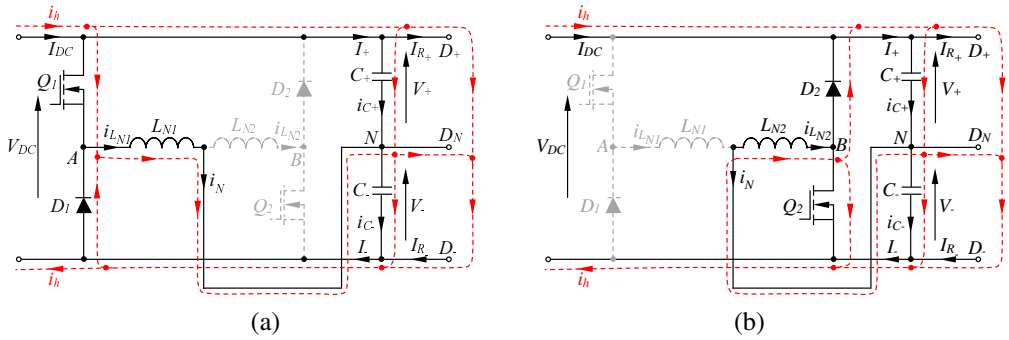


Fig. 4. The harmonic current paths of the divider as operated in [5] when (a) $i_N > 0$; (b) $i_N < 0$.

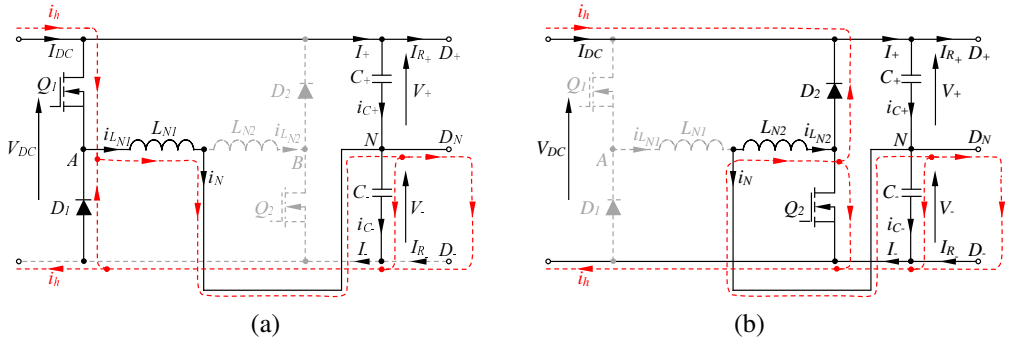


Fig. 5. The intended harmonic current paths when (a) $i_N > 0$; (b) $i_N < 0$.

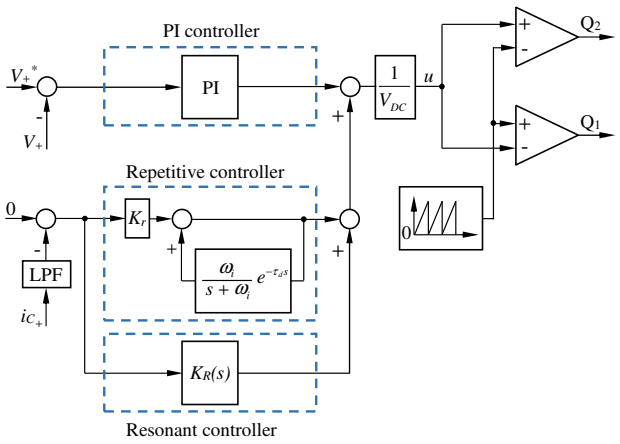


Fig. 6. The proposed controller for the divider.

A. Splitting the DC-bus Voltage

According to (8), the control signal u can be chosen as the duty cycle d_2 of Switch Q_2, i.e.,

$$u = d_2 = \frac{V_+}{V_{DC}}.$$

In other words, the output voltage V_+ can be controlled by controlling the duty cycle d_2. In order to achieve this, the voltage V_+ is measured as a feedback and a proportional-integral (PI) controller can be used to regulate V_+ around its reference V_+^*, as shown in Fig. 6. The switching pulses for Q_2 can be generated by comparing u with a positive sawtooth signal as shown in Fig. 6. When $u \le 0$, $d_2 = 0$ and $d_1 = \frac{V_-}{V_{DC}} = 1 - \frac{V_+}{V_{DC}}$. The switching pulses for Q_1 can be generated by comparing $-u$ with the same positive sawtooth signal as shown in Fig. 6. Hence, $d_1 = 0$ when $u \ge 0$ as well. This matches the operational principles discussed in Section II. Note that the outputs V_+ and V_- can be the same or different without any restrictions. Once the voltage V_+ is controlled, the voltage V_- is naturally maintained as $V_- = V_{DC} - V_+$.

B. Diverting the Harmonic Current away from C_+

Here, the capacitor current i_{C_+} is controlled in order to divert the harmonic current away from the capacitor C_+. Note that only the low-frequency components in i_{C_+} are considered. The capacitor C_+ should be large enough to filter out switching-frequency ripples. For this purpose, a low-pass filter (LPF) is adopted to extract the low-frequency components in the i_{C_+}. In practice, the LPF can be constructed by adding a resistor-capacitor circuit on the path of the measured i_{C_+}.

In order to achieve the diversion of the harmonic current, the reference current of i_{C_+} is set to zero. In this paper, a repetitive current controller is adopted to attenuate the major harmonics. The repetitive controller consists of a proportional controller K_r and an internal model given [2] by

$$C(s) = \frac{K_r}{1 - \frac{\omega_i}{s+\omega_i} e^{-\tau_d s}}.$$

For the 50 Hz fundamental frequency ω, ω_i and τ_d can be selected as $\omega_i = 2550$ rad/s and

$$\tau_d = \tau - \frac{1}{\omega_i} = 0.0196 \text{ s},$$

where $\tau = \frac{2\pi}{\omega} = 0.02$ s.With such a repetitive controller, the harmonics at multiples of the fundamental frequency ω can be significantly attenuated. However, it is not able to deal with harmonics at other frequencies, e.g. 120 Hz. In order to deal with a different frequency component, the resonant controller

$$K_R(s) = \sum_{h=\cdots} \frac{2\xi\omega_1 s}{s^2 + 2\xi h\omega_1 s + (hw_1)^2} \times K_h$$

can be added. The $K_R(s)$ is almost zero everywhere apart from the harmonic frequencies $h\omega_1$, which means harmonics at different frequencies can be considered individually. The coefficients K_h can be chosen through trial-and-error in practice with a larger value for lower harmonics but a smaller value for higher harmonics. At the same time, the h can be selected according to the knowledge of the input current I_{DC}, e.g., which frequencies should be attenuated. If such knowledge is not prior available, the spectrum of the I_{DC} has to be checked first and, based on this spectrum, the h, i.e., which frequencies should be compensated, can be decided. Note that a repetitive controller tuned at the relevant frequency can be used instead of the resonant controller.

As shown in Fig. 6, the outputs of the repetitive current controller and the resonant current controller are added together onto the output of the PI voltage controller to form the final control signal, i.e., u, before sending to the pulse-width modulation.

C. System Stability

As shown in Fig. 6, the controller has a parallel structure. The upper voltage loop mainly deals with the DC component of I_{DC} while the lower repetitive and resonant current loops deal with non-DC components in the I_{DC}. In this case, the three loops are decoupled in the frequency domain. As long as each loop is stable, which can be easily achieved, then the stability of the whole controller is naturally guaranteed [2].

IV. Experimental Results

In order to verify the proposed strategy, an experimental test system was assembled in the lab. The system is controlled by TMS320F28335 DSP and the code of the controller is built in MATLAB/SIMULINK R2013a and then downloaded to the DSP with the sampling frequency of 4 kHz and the switching frequency 15 kHz. The gains of the PI controller are 5 and 10 while the gain of the repetitive controller is selected as 15. The DC-bus voltage of the divider is supplied by a Chroma 61860 grid simulator as

$$\begin{aligned} V_{DC} &= 340 + 9\sin(120 \times 2\pi t) + 10\sin(150 \times 2\pi t) \\ &\quad +5\sin(300 \times 2\pi t), \end{aligned}$$

which includes a 340 V DC voltage and harmonic voltages at three different frequencies, i.e., 120 Hz, 150 Hz and 300 Hz.

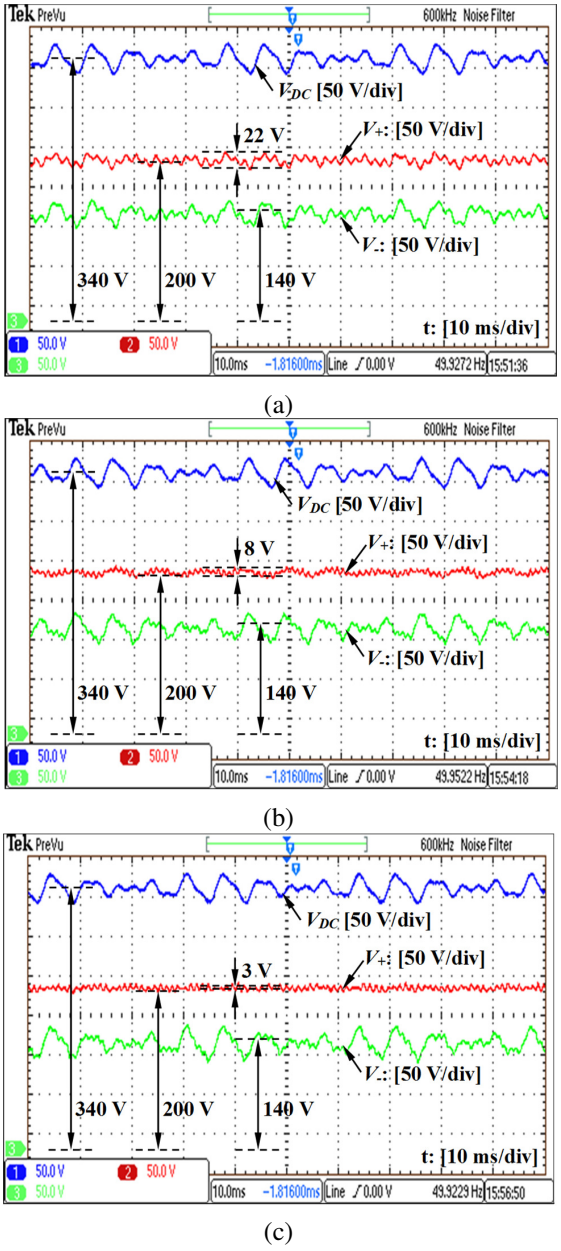
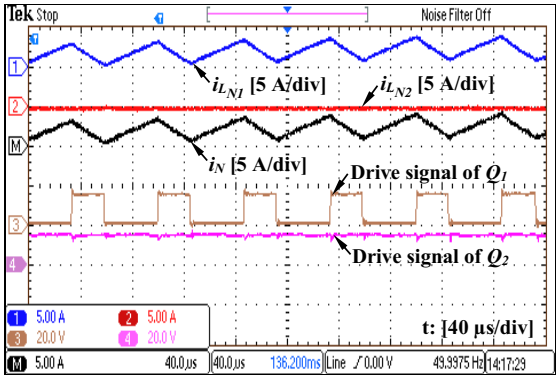
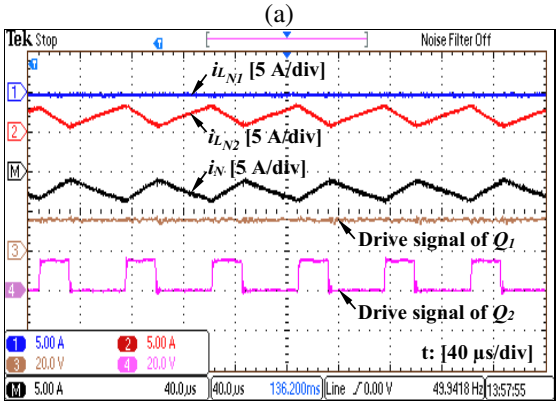


Fig. 7. System steady-state performance when $V_+^* = 200$ V, $V_-^* = 140$ V, $R_+ = 100\,\Omega$ and $R_- = 470\,\Omega$: (a) only with the PI controller; (b) only with the PI and repetitive controllers; and (c) with the PI, repetitive and resonant controllers.

The 150 Hz and 300 Hz ones are at the multiples of the fundamental frequency 50 Hz. The repetitive controller is used to attenuate both of them at the same time. The DC-bus voltage also includes a 120 Hz component, which could be due to the existence of a 60 Hz converter. It can be handled by the resonant controller. In this case, the h in the resonant controller is chosen as $\frac{120}{60} = 2$ and the corresponding gain K_h is selected as 50 with $\xi = 0.01$. The LPF for the current measurement is selected as $\frac{10000}{s+10000}$, of which the cut-off frequency is 1589 Hz. It can be implemented with a 10 kΩ resistor and a 0.01 μF capacitor.



(a)



(b)

Fig. 8. The currents i_{N1}, i_{N2} and i_N and the drive signals of the switches Q_1 and Q_2 (a) when $i_N > 0$ with $V_+^* = 200\,\text{V}$, $R_+ = 100\,\Omega$ and $R_- = 470\,\Omega$; (b) when $i_N < 0$ with $V_+^* = 140\,\text{V}$, $R_+ = 470\,\Omega$ and $R_- = 100\,\Omega$.

In order to test the system performance with unbalanced loads and capacitors, two different loads R_+ and R_- are connected across the split capacitors $C_+ = 30\,\mu\text{F}$ and $C_- = 20\,\mu\text{F}$, respectively. Two 2.2 mH inductors available in the lab are used for L_{N1} and L_{N2}, respectively, without optimizing the inductance or size.

In the experiments, the PI controller, repetitive controller and resonant controller are enabled one by one to show their performance on the reduction of voltage ripples at different frequencies. The corresponding experimental results are shown in Fig. 7(a), (b) and (c), respectively. The recorded data of the voltage V_+ in experiments were sent to MATLAB to extract the peak-peak value of its low-frequency ripple, which is 22 V for the PI controller, 8 V for the PI controller plus the repetitive controller, and 3 V for the PI controller together with the repetitive controller and the resonant controller, as shown in Fig. 7. This is consistent with the theoretical analysis.

As discussed before, only one of the two legs is in operation at a time. In order to demonstrate this, the waveforms of i_{N1}, i_{N2}, i_N and the drive signals of Q_1 and Q_2 are shown in Fig. 8(a) and (b), after changing the V_+^* and the loads to achieve the two cases with $i_N < 0$ and $i_N > 0$, respectively. Note that the switches Q_1 and Q_2 are turned off when the drive signals are high. As shown in Fig. 8(a), only the left leg is in operation when $i_N > 0$ and, as shown in Fig. 8(b), only the right leg is in operation when $i_N < 0$.

V. Conclusions

In this paper, two unexplored features of dual-buck dividers, i.e., arbitrary DC voltage levels and reduced low-frequency ripples, have been investigated. An advanced control strategy has been proposed to operate a dual-buck voltage divider to split the DC-bus voltage arbitrarily. The low-frequency ripples in one of the outputs are significantly reduced by actively diverting harmonic currents away from the corresponding output. All of these are achieved without adding any additional active or passive components. Experimental results have demonstrated the effectiveness of the proposed strategy.

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