

High Performance Automatic Gain Control Circuit for Communication Applications

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Abstract: - A high performance automatic gain control (AGC) circuit of analog type is presented in this paper. The proposed AGC incorporates a modified sample and hold peak-detector. Circuit operations of this new peak-detector are demonstrated superior to the conventional one, by both keeping and tracking the peak of the input signal at the same time. Furthermore, the design complexity of the proposed AGC is reduced in both the low pass filter and the demodulator due to the modified peak-detector. Based on post-layout simulation results, the complete AGC loop shows very satisfactory circuit operation. Therefore, it is suitable for high performance communication applications such as ASK receiver.

Key-Words: - Automatic gain control, Sample and hold, Peak detector, Variable gain amplifier, IF amplifier, Loop filter, ASK receiver

1 Introduction

Automatic gain control circuits (AGC) are usually employed in the systems where the amplitude of an incoming signal varies over a wide dynamic range [1]. The application domain of such systems is growing very rapidly from sensor interfaces to charge-coupled devices (CCD)/CMOS imagers, wire or wireless communications, disk drive read channels, medical, and multimedia systems, to name a few. Especially in the wireless communications, the signal strength level will be different due to the multi-path fading and different positions. The AGC is therefore used to adjust the received signal to a rated strength level.

The conventional AGC consists of many block circuits, as shown in Fig.1. The input signal is amplified by the variable gain amplifier (VGA). The comparator compares the signal extracted from the strength of the output by the peak-detector with a reference voltage to set a control signal in the output. The loop filter averages the control signal to generate a dc signal to vary the gain of the variable gain amplifier. Usually, this dc signal of the loop filter output is used as a received signal strength indicator (RSSI) [2]. By this feedback loop, this circuit can automatically sense the strength of the output signal and modify the gain of VGA to keep stable output signal strength.

There are two approaches to implement an AGC. One is analog type [3]. The other is mixed signal type [4, 5] which the peak-detector, comparator and

loop filter are implemented by digital circuits. The block diagram of a mixed signal AGC is shown in Fig.2.

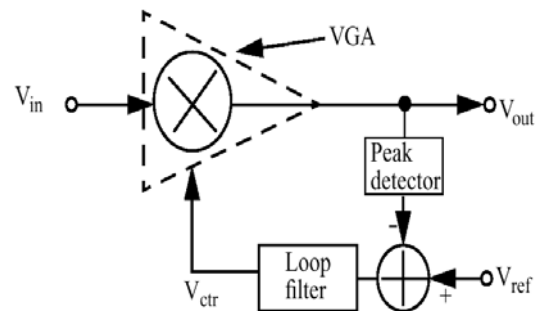


Fig.1 Conventional AGC block diagram

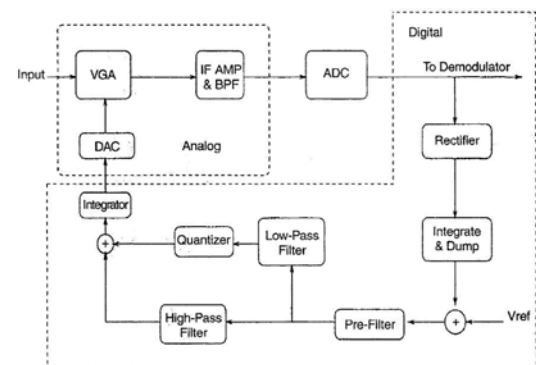


Fig.2 Mixed signal AGC block diagram

There are some advantages in the mixed signal type AGC. First, the digital circuits have better noise resistance. Second, the components of digital circuits can be realized by a DSP chip or be integrated with the digital circuits of the system to reduce the cost. In some situations the VGA and DAC are combined as a digital controlled VGA, as shown in Fig.3.

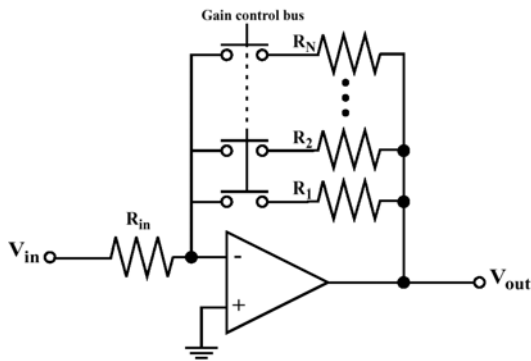


Fig.3 Digitally controlled VGA

In Fig.3, it is a VGA with a switched feedback network of resistor to tune the gain. It takes full advantage of negative feedback, so it has good linearity and both large input and output swings. However, there are still some disadvantages in this approach. Because many components are implemented by digital circuits so that an ADC (analog to digital converter) and a DAC (digital to analog converter) are needed. This reason will increase the circuit complexity, chip area and power consumption. There are also quantization errors in the process of AD/DA conversion to affect the performance. In the other hand, the digital feedback control leads to the discontinuous gain variation of VGA.

2 The Proposed AGC

The proposed AGC, especially for ASK receiver applications, as shown in Fig.4, is designed in analog type with Gilbert cell VGA [5, 6]. It uses a sample and hold peak-detector to extract the signal strength of the VGA output. The demodulator converts the signal from the peak-detector output to a digital signal. A charge pump circuit with a capacitance realizes the loop filter of the conventional analog type AGC. By this way, both ADC and DAC are not needed and it is also easy to extract the digital signal in ASK modulation by using a simple demodulator circuit. The proposed

AGC will also incorporate a modified peak-detector for high performance applications.

2.1 VGA and IF Amp Blocks

Those conventional topologies for CMOS circuits are usually achieved by controlling the degeneration or load resistance. Their characteristics of control curves are usually linear. But the best performance in an AGC circuit requires its VGA with exponential gain function. A VGA with linear gain function will lead the loop settling time constant dependent on the input signal strength.

The proposed VGA, as shown in Fig.5, is a differential pair amplifier cascaded with a modified Gilbert cell. The differential pair, M4 and M5, is the first stage amplifier. The modified Gilbert cell is the second stage amplifier. To avoid the body effect, the bulks of PMOS transistors are all connected to their source. The gain characteristics is controlled by the cascode current source, M6, M16 and M7, M17, to vary the tail currents of the differential pairs, as below.

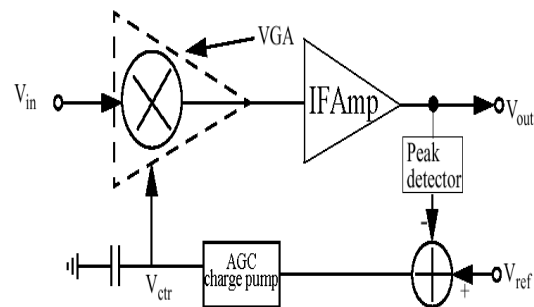


Fig.4 The proposed AGC block diagram

$$\frac{g_{m1}}{g_{m2}} = \frac{\sqrt{\mu C_{ox}} (W/L)_1 I_1}{\sqrt{\mu C_{ox}} (W/L)_2 I_2} = \sqrt{\frac{(W/L)_1 (I + \Delta I)}{(W/L)_2 (I - \Delta I)}} = K \left(\frac{1+x}{1-x} \right)^{0.5} \approx e^x$$

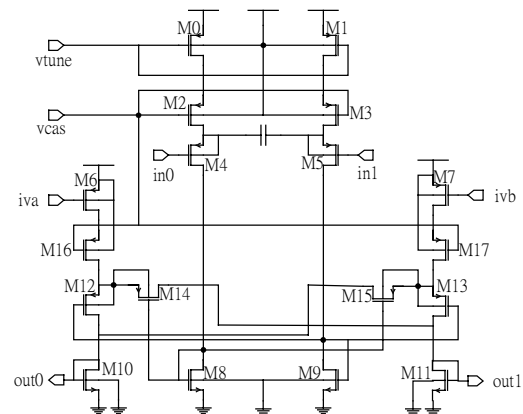


Fig.5 Proposed VGA with approximate exponential gain

Because the VGA gain is controlled by varying the tail currents in opposite directions, and the feedback control signal is a DC voltage, so that a circuit to convert the DC voltage into opposite current signals is needed. This voltage-to-current (V-I) converter circuit is depicted in Fig.6.

In Fig.6, the “vcntrl” signal is a gain control input. The current of M0 and M1 is tuned in opposite directions by using the “vcntrl” signal and they will be equal as the voltage level of “vcntrl” signal reaches VDD. Using the current mirror effect, the current flow in the VGA is controlled by the voltage of input “vcntrl”. By this design, the proposed VGA circuit can realize an approximate exponential gain function and provide large dynamic gain range about from -20dB to 12dB.

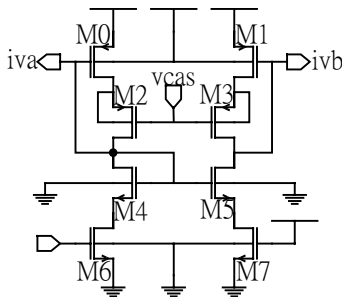


Fig.6 Proposed VI converter

Because the output signal is differential and the overall gain in IF circuit is important, a differential to single-ended IF amplifier is needed. This amplifier can be realized by modifying a wide-band amplifier [7]. The schematic of this amplifier is depicted in Fig.7.

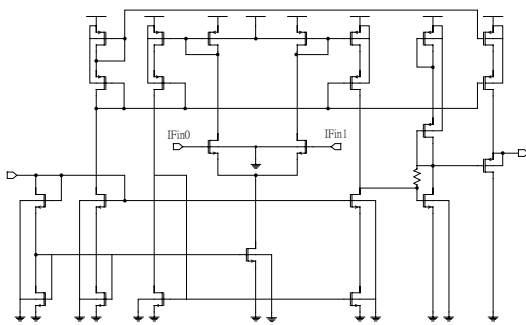


Fig.7 Proposed IF amplifier

2.2 Peak-Detector Block

The conventional peak detector and the proposed peak detector, as shown in Fig.8, is to make use of characteristics of a diode and keep the signal peak

by the capacitance. For implementation, two two-stage differential amplifiers can realize these two operational amplifiers. The diode can be realized by a diode connected NMOS transistor and the current source is simply an NMOS transistor operated in the saturation region.

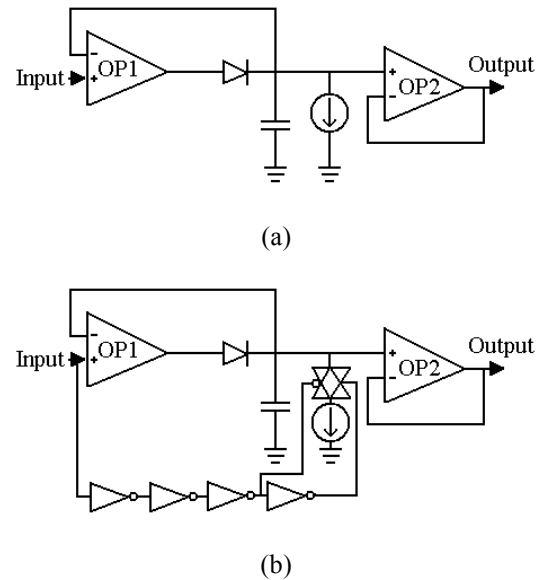


Fig.8 Block diagram of the peak-detector.
(a) the conventional (b) the proposed

Although this peak-detector is simple and easy to realize, there is a trade off in keeping and tracking the peak of the signal. A smaller discharge current leads to a smaller edge of sharp teeth of a saw and a worse capability in tracking the next peak. A larger discharge current leads to a larger edge of sharp teeth of a saw and a better capability in tracking the next peak. This trade off leads to the difficulty, that it is hard to design a low pass filter to average the edge of sharp teeth of a saw and fit well to the waveform peak in ASK signal by this peak-detector output.

The proposed sample and hold peak-detector overcomes this trade off by keeping and tracking the peak of the signal at the same time. The input signal is designed to have a dc level at VDD/2. The signal flow of this peak-detector is divided into two paths. One goes through the operational-amplifier and the diode to charge the capacitance. The other goes through the inverters to be amplified and to control the transmission gate. When the input signal is during the positive cycle (the sampling mode), the inverters amplify the input signal as a digital waveform to turn on the transmission gate and so the peak-detector tracks the peak of the input signal well. When the input signal is during the negative

cycle (the hold mode), the transmission gate turns off and the capacitance holds the peak voltage of the input signal.

3 Simulation Results

The proposed AGC loop has four modified Gilbert cell VGA cascaded as the VGA block. The simulation of a modified Gilbert cell VGA cascaded with IF amplifier is given in Fig.9. According to the results, a modified Gilbert cell VGA provides about from -20dB to 12dB variable gain range and the IF amplifier can provide about 21dB voltage gain. The whole VGA and IF amplifier can provide about 48dB control gain range and overall more than 60dB gain.

The simulations of the conventional peak detector and our proposed sample and hold peak-detector are shown in Fig.10 (a) and Fig.10 (b). The edge of sharp teeth of a saw becomes smoother and fits very well to the peak of the signal as compared to the conventional one.

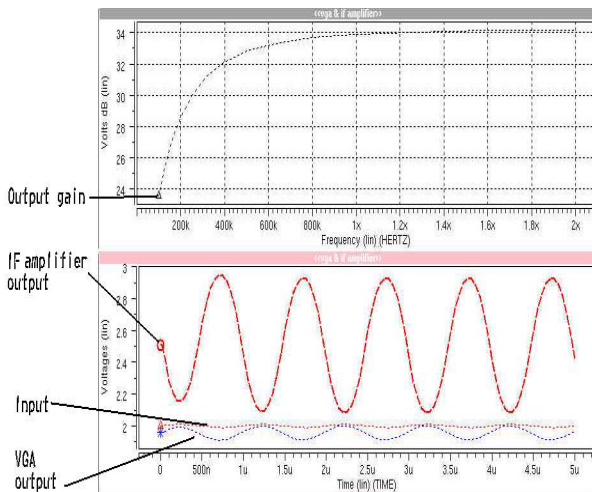
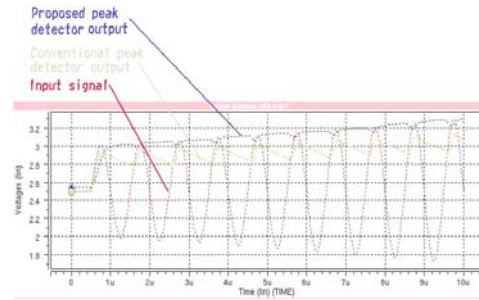
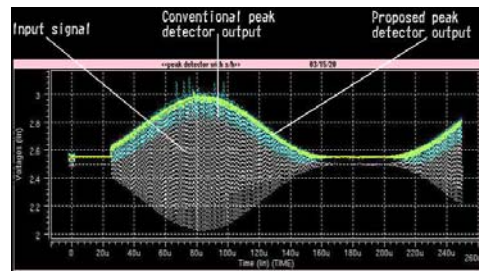


Fig.9 Transient and AC simulation for the VGA and IF amplifier

The whole chip layout is shown in Fig.11. Because the output of the peak-detector fits very well to the peak of ASK modulation signal, the digital signal can be directly extracted by using a comparator to compare the peak value with a reference voltage. In the whole chip post-layout simulation, as shown in Fig.12, the peak value, higher than the reference value is set as logic '1' and otherwise is set as logic '0'. Judging from simulation results, the complete AGC loop operation is very satisfactory.



(a)



(b)

Fig.10 Simulated transient response of (a) sine wave signal (b) ASK signal

Hspice simulations of the proposed AGC are listed in Table 1. By this design, the degree in the edge of sharp teeth of a saw is reduced so that the design complexity of the loop filter, which is used to average the edge of sharp teeth of a saw, and the demodulator decrease as well. Besides, since this AGC is implemented in CMOS process it can be easily integrated in an ASK receiver.

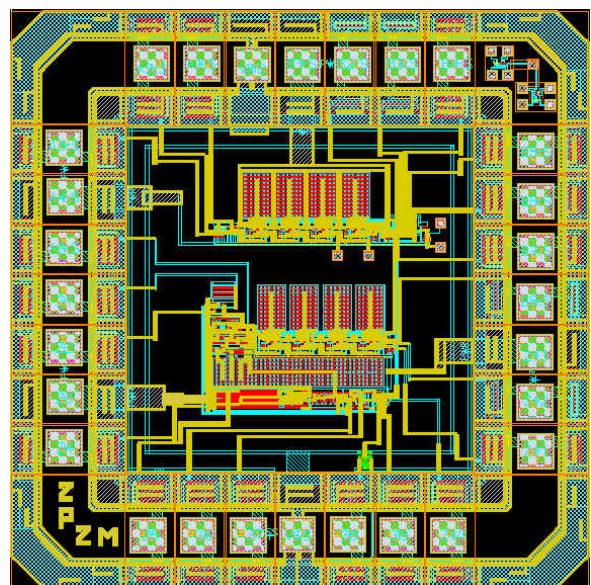


Fig.11 The proposed AGC whole chip layout

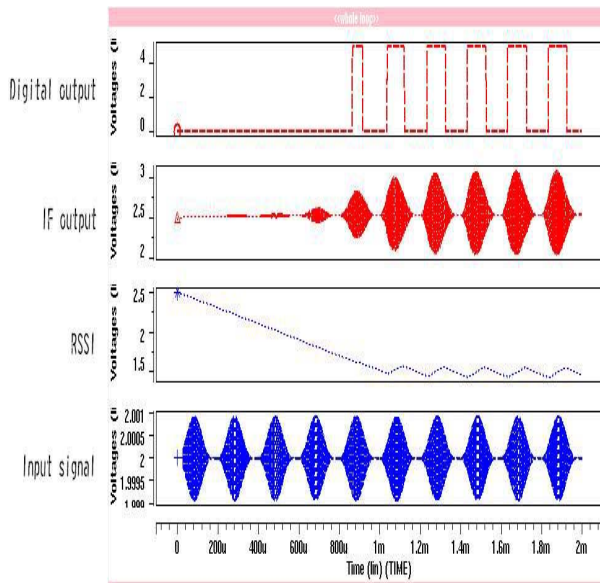


Fig.12 The post-layout simulations of proposed AGC with ASK modulation signal

Table 1 Performance summary

Input frequency	1MHz
Min. input amplitude	0.5mVp-p
Max. input amplitude	0.3Vp-p
IF output amplitude	1Vp-p
Digital output amplitude	5Vp-p
Power dissipation	16mW
AGC control range	-60dB~48dB
Chip area	1.8mm x 1.8mm
Technology	0.5um CMOS

4 Conclusion

In this paper, an analog type automatic gain control circuit has been presented. The proposed AGC incorporates a modified sample and hold peak-detector, whose circuit operation has been demonstrated superior to the conventional one. Besides, the design complexity of the proposed AGC is reduced in both the low pass filter and the demodulator due to the modified peak-detector. Based on post-layout simulation results, the complete AGC loop shows very satisfactory circuit operation. Therefore, it is suitable for high performance communication applications such as ASK receiver.

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