ACTIF: A high-level power estimation tool for Analog Continuous-Time Filters

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Abstract

A tool is presented that gives a high-level estimation of the power consumed by an analog continuous-time OTA-C filter when given only high-level input parameters such as dynamic range and signal swing. When used in combination with estimators for other building blocks (ADC's, DAC's, mixers,…) a truly high-level analog system exploration becomes feasible such as needed for architectural exploration of telecom systems. In literature only fundamental relations exist for analog filters, that predict the power with an error of orders of magnitude, which makes them hard to use in real system design. ACTIF combines existing filter synthesis methods with new behavioral models for transconductance stages in a novel way to obtain an optimized high-level yet accurate power estimation. To verify the presented approach, two recently published design examples are compared with the results from ACTIF.

1. Introduction

Architecture selection and system-level specifications of mixed-signal systems are usually defined by a very experienced designer (or group of designers) who has an overview over possible pitfalls. Even then, the new design is usually based on an old existing design in which some minimal modifications have been done.

Efforts are being done to construct CAD tools that formalize and speed up the system design while minimizing a given cost function [1]. One possible cost function is minimum power consumption. Within a given system, often many different power-consumption related trade-offs are present. These trade-offs can only be checked rapidly, without going to an actual design, if good high-level power estimators exist for the building blocks involved (analog and digital). A power estimator is a function that returns an estimated value for the power consumed by a functional block when given some relevant input specifications, without knowing the detailed implementation of the block:

$$Power_{ESTIMATED} = f(high-level\ specifications) \qquad (1)$$

For power estimators to be useful for first-order high-level system design, it is important that the following requirements hold.

- The estimators may have as input parameters only high-level block parameters. The system designer gets very fast feedback about the impact of a certain block without having to go to a transistor-level implementation or without relying on previous designs.
- The accuracy of the estimated value with respect to the exact, finally measured power consumption of an implementation of the block only has to be within a first-order range. An exact value is only needed when a chosen architecture is examined in greater detail. The trend of the estimator function has to be more accurate to allow correct architectural, high-level trade-offs.

In digital microelectronics complete tools like PowerMill from Synopsys exist, that estimate the power needed to perform a digital function. In analog microelectronics, efforts to construct power estimators are sporadic and less focused. Fundamental relations have been proposed [2,3], but they have poor results that can be far from the real value by orders of magnitude and only present a theoretical lower bound. Some more accurate estimators can be found for building blocks such as opamps [4] and high-speed ADC's [5]. This work adds to this set an estimator for analog continuous-time OTA-C filters.

High-frequency analog filters are used in many applications, including telecommunications, to filter out undesired signals. This paper presents a power estimation tool for OTA-C filters called ACTIF.

In section 2, the general approach of ACTIF is explained. In section 3 and 4 the constituting parts of the tool are described in detail. In section 5 experimental results are presented.

2. The ACTIF approach

ACTIF estimates the power consumed by an analog continuous-time OTA-C filter when given as input a limited set of high-level system parameters. Only three inputs are basically needed: the filter transfer function, the desired dynamic range (DR) and the maximal (differential) signal amplitude. The output is the power consumption needed to realize the given transfer function.

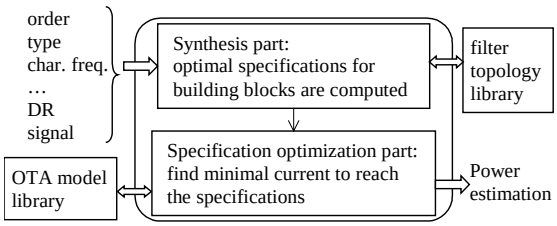

Figure 1 An overview of the ACTIF flow

The ACTIF tool is divided in two major parts: the filter synthesis part and the OTA specification optimization part (Figure 1). Linked to them are a filter topology library and a OTA model library. Details of both parts are given in the subsequent sections.

The art of finding a good analog power estimator is finding that exact level of abstraction at which one can disconnect the topology information from all what comes below that abstraction level, down to the transistor level. For the CT OTA-C filters, this point is found at the transconductor level. Finding the high-level specifications for the transconductors (gm and distortion) is done using the *filter synthesis* part. In the second step, the *OTA optimization* part, optimization techniques are used in combination with behavioral models for the OTAs to find the minimal needed current to achieve the derived OTA specifications. Other techniques are also possible, such as table lookup and in-the-loop simulation.

3. Synthesis workflow

The synthesis workflow of ACTIF as illustrated in Figure 2 is as follows. On the top left part the wanted filtering function is given to the tool (for example a 4th order elliptic bandpass filter). The filter transfer function is then split in a first-order stage, if the order is odd, and second-order stages.

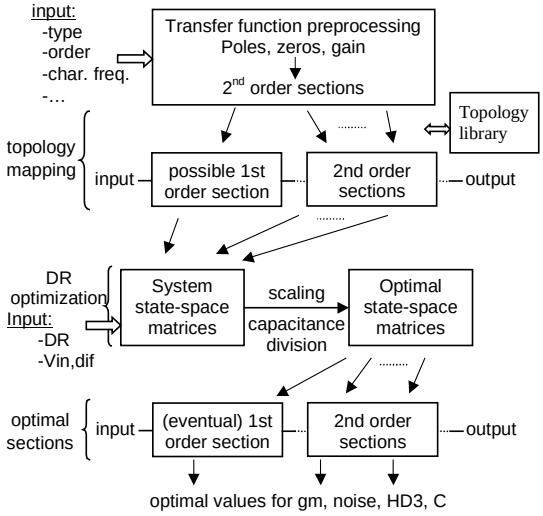

Figure 2 Synthesis workflow of ACTIF

These stages are mapped on a biquad topology and for each section the state-space matrices are constructed. Next the total system state-space matrices are calculated using the desired dynamic range and signal level from the input, the optimal system state-space matrices are then obtained after scaling and optimal capacitance distribution. The result is then broken up again into 2nd-order sections and the optimal values for the needed OTA specifications are derived. This workflow is now discussed in more detail. The construction of the filter transfer function and the pole-zero pairing, section ordering and gain assignment is extensively commented in the literature [6] and not repeated here. The next step is to map the sections on a given topology that suits best the needs of the designer. Three main topologies exist: the multiple-loop feedback realization, the ladder simulation realization and the cascade realization with biquads. In ACTIF the cascade realization is implemented. This is not a restriction for a first-order power estimation because second-order sections generally need 4 or 5 OTAs to be realized, regardless of the topology and therefore will result in a good power estimate.

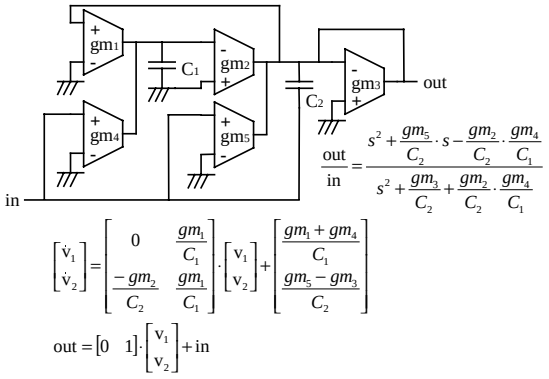

Figure 3 General biquad, its transfer function and state-space representation

In Figure 3, an example of an implemented general biquad type, its state-space matrices and its transfer function is given. ACTIF expects a differential realization to gain 6dB in DR. Once a suitable topology and its description is found, the coefficient mapping is done.

The system state-space matrices are constructed from the stages' state-space matrices in the following way:

$$\begin{aligned} Bsys_i &= B_i \cdot \prod_{j=1}^{i-1} D_j \\ Csys_i &= \prod_{j=i+1}^{n} D_j \cdot C_i \\ Dsys &= \prod_{i=1}^{n} D_i \end{aligned} \qquad \begin{cases} Asys_{ij} = B_i \cdot C_j \cdot \prod_{k=j+1}^{i-1} D_k : i < j \\ Asys_{ij} = A_i : i = j \\ Asys_{ij} = 0 : i > j \end{cases} \qquad (2)$$

In equation (2), n is the number of stages. To obtain the wanted DR, the total capacitance budget available for the filter is sweeped from a maximal desirable value until the goal is reached or until a minimum limit value is reached. For every capacitance value, scaling and optimal capacitance distribution are performed after which the DR is calculated. If the DR is fine, the sweep stops; if not then a new total capacitance value is taken and the loop is repeated. Formulas needed for scaling, capacitance distribution as well as the calculation of the DR are from [7]. The optimization does not alter the topology of the filter stages.

From the transformed and optimized system matrices the state-space matrices of the stages are reconstructed by proper division or multiplication with the scaling or transformation matrix. The gm values are obtained directly, the noise levels at the outputs of the internal integrators are calculated from the system state-space matrices, the signal swing and the DR:

$$V_{n,i}^2 = \frac{2 \cdot kT \cdot \xi_i \cdot \left(|Bsys_i| + \sum_j |Asys_{ij}| \right) \cdot \max_j Ksys_{jj}}{Cap_i \cdot CsysKsysCsys^T} \qquad (3)$$

where Cap_i is the capacitance of integrator i, *Ksys* is the system controllability Gramian matrix and ξ_i is the noise figure

of integrator i. The noise figure is assumed to be 1 or optimal. If a more accurate estimation is wanted, this value can be 1 for the first estimation, after which a better value is calculated using the information of the first results and the estimation process is repeated with the new value. The maximum distortion of each OTA can now be set equal to the noise floor.

$$HD3_i = 10\log_{10}\left(V_{in,dif}^2 \Big/ V_{n,i}^2\right) \qquad (4)$$

Another possibility is to state that the harmonic distortion or the intermodulation distortion at the output should not be higher than 1% of the signal level from which again the distortion level for each OTA is then calculated.

From here on the gm and distortion levels of each OTA are known and are given to an optimizer which minimizes the current to reach these values.

4. OTA behavioral modeling and optimization for minimal power consumption

For each OTA the bias current has to be minimized when given the above calculated constraints on gm and distortion. Only the third-order harmonic distortion HD3 is taken into account because higher-order terms are typically smaller, the second-order term is cancelled out in differential designs and the intermodulation product is obtained from the HD3 term.

This means that for gm and HD3, models have to be developed. To this end 5 different OTA stages have been simulated in a 0.35µm CMOS process with varying design parameters and with an input voltage amplitude sweep. The design parameters are characteristic for each gm topology. For example, for a source-degenerated differential pair, three parameters are used in the model: I_{DS} and $V_{GT}=(V_{GS}-V_T)$ of the input transistors and the degenerating resistance R. In total 4 parameters are sufficient for the 5 OTAs:

$$\begin{cases} gm = f(I_{DS}, V_{GT}, w, R) \\ HD3 = f(I_{DS}, V_{GT}, w, R) \end{cases} \qquad (5)$$

The w is one of the circuit design parameters.

The 5 topologies suitable for a 3.3V power supply are: a simple differential pair, a differential pair with source degeneration and 3 others that are found in [8, 9, 10]. This is an arbitrary choice that tries to span a large frequency and linearity range but any other topology can be added to ACTIF.

4.1. Modeling of the transconductances

The models used for the different OTAs, are based on existing hand formulas which have been fitted to the simulated data. For a degenerated differential pair for example, the expression for gm becomes:

$$gm = \frac{1.77 \cdot \frac{I_{DS}}{V_{GT}}}{V_{GT} + I_{DS} \cdot R} = \frac{1.77 \cdot I_{DS}}{V_{GT} + I_{DS} \cdot R} \qquad (6)$$

For the OTA structure from [10], the expression becomes:

$$gm = \frac{I_{DS} \cdot V_{GT}}{V_{GT}^2 + I_{DS} \Big/ w} \qquad (7)$$

Because a filter is a linear signal processing block the small-signal gm is modeled. All deviations from the ideal linear behavior for large signals are taken into account in the expressions for the distortion.

4.2. The distortion model

For each different OTA topology an expression for the third-order harmonic distortion has to be available. The inputs to the model are the design parameters of the OTA and the signal swing and the output then is the distortion level:

$$HD3 = f(V_{in,dif}, I_{DS}, V_{GT}, w, R) \qquad (8)$$

Theoretical expressions exist that do this for the used topologies but they are only valid for very small signals. Furthermore these formulas sometimes require too many design parameters as inputs to be practically useful in the high-level context discussed here. Finally, because an optimization is involved, as will be explained further, often the distortion has to be returned for large signals. Therefore new distortion models were built.

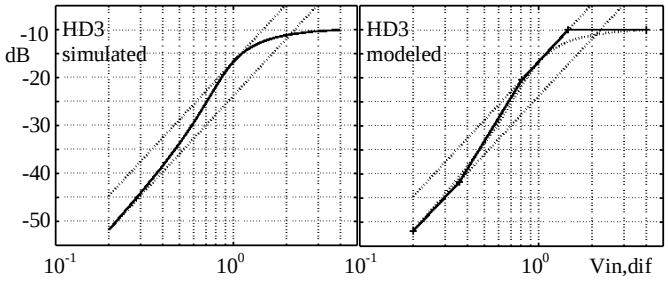

Figure 4 3th order distortion profile as a function of the input signal. left: simulated, right: modeled

A typical simulated third-order distortion behavior for the OTA of [8] is plotted in Figure 4 (left) in a solid line. For small input signals the line follows a nice slope of 40dB/decade as expected, indicated by the lower dotted line. For larger signals the distortion degrades faster than this slope predicts due to large-signal behavior and at a certain signal amplitude the distortion is clipped (in the figure at about –10dB). This behavior is modeled quite well by the solid line (right Figure 4) which is the model used in ACTIF. Sometimes the two dotted lines are virtually the same and the 4-region model changes in a two-region model. This distortion model together with the gm model is then used in an optimizer to find the minimal power consumption.

4.3. Optimization

The optimization flow is as follows (see Figure 5). For a given OTA parameter set, the boundaries of the regions in the HD3 model are calculated. If the region is known, then the expression for HD3 is known for that set of parameters. For example for the left region of the model:

$$HD3 = f(I_{DS}, V_{GT}, w, R) + 40\log_{10}(V_{in,dif}) \qquad (9)$$

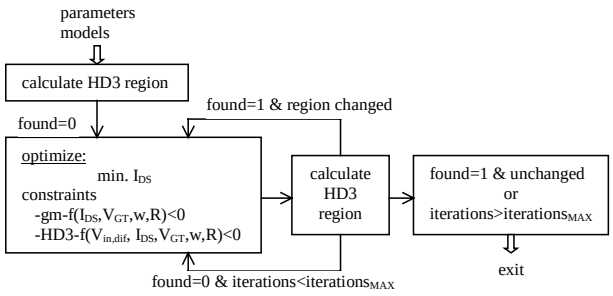

Figure 5 Optimization flow

With the expression for gm added, the constrained-based gradient search optimization as implemented in Matlab™ can start looking for that parameter set for the asked gm and HD3 values that yields minimal current I_{DS}. However, it is possible that the new set of parameters changes the model region of the HD3 model or that no solution is found. So a kind of rule-based optimization was programmed that notices when region oscillation or non-convergence occurs and handles it.

Type	Minimal current	goal gm	found gm	goal HD3	found HD3	indicator
SDP'	'1200.058'	'2.944e-07'	'0.0038001'	'55.9188'	'52.0009'	'maybe'
'SRDP'	'59.6275'	'2.944e-07'	'0.00013223'	'55.9188'	'55.9188'	'good'
'TOR'	'53.2937'	'2.944e-07'	'9.3392e-05'	'55.9188'	'55.9188'	'good'
'KRUM'	'1200.0196'	'2.944e-07'	'0.0035669'	'55.9188'	'54.6595'	'maybe'
'SIL'	'172.9208'	'2.944e-07'	'0.00034576'	'55.9188'	'55.9188'	'good'

Figure 6 Output table of ACTIF for one gm of a fictive filter example

The output of the optimization is a table for each OTA needed in the filter as shown in Figure 6. It indicates the current needed to achieve the "found" values. If these are within specifications, an indication "good" is given. If the values are not attained but are within a certain margin, the tag "maybe" is given because this is an indication that a goal could not be attained. If completely wrong values come out, a "bad" tag is given to indicate that the optimizer could not converge. It is typical that the gm values can easily be obtained and that the distortion specification is the limiting factor. This stresses the importance of including the distortion behavior of the OTAs in the power estimation of filters.

5. Experimental results

Two examples are given to illustrate the capabilities of ACTIF. Power estimation time is for each about 6 minutes using a SUN sparc-30 running Matlab™.

Example 1: A 7th order phase-equiripple 0.35µm CMOS LPF with a cut-off frequency of 70MHz was presented in [11]. It consumes 55mW, including the control circuitry, the DR is 42dB and the differential input swing is 400mV_{pp}. When given to ACTIF, the outcome for high-speed OTA topologies is 34.9mW. This is quite good considering that the control circuitry is still missing in the estimator. Including tuning strategies in the estimator is subject of further work.

Example 2: A 5th order 0.8µm CMOS LPF with a 4MHz cut-off frequency, a DR of 57.6dB, a $V_{in,dif}$ of 0.625V_{pp}, a total intermodulation distortion of 40 dB and a power consumption of 10mW was presented in [12]. The distortion level is lower than the DR and it is not a biquad implementation. It is in a different technology but with a 3V supply voltage, which is the main limiting factor for distortion. If the correct distortion level is given to ACTIF, the result is a total power consumption of about 3.5mW (again without tuning). This is close enough to the published power consumption for a first-order estimation on a truly high level, even for a different filter topology than used in the real implementation. If, as an experiment, the filter has to be redesigned by increasing the distortion specification up to the DR, then a total power of 88.8mW is expected.

6. Conclusions

A high-level tool is presented that estimates the power consumed by an analog continuous-time OTA-C filter. The inputs are typical high-level filter specifications (type, order,…), dynamic range and input signal amplitude. The output is an estimate of the power needed to realize the filtering function when an optimal implementation is used. The filter synthesis involved and the optimization and modeling of OTA stages have been implemented in the ACTIF tool. Experimental results have shown the accuracy of the power predictions.

Acknowledgements

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