AGING-BASED LEAKAGE ENERGY REDUCTION IN FPGAS

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ABSTRACT

The presence of process variation (PV) in deep submicron technologies has become a major concern for energy optimization attempts on FPGAs. We develop a negative bias temperature instability (NBTI) aging-based post-silicon leakage energy optimization scheme that stresses the components that are not used or are off the critical paths to reduce the total leakage energy consumption. Furthermore, we obtain the input vectors for aging by formulating the aging objectives into a satisfiability (SAT) problem. We synthesize the low energy design on Xilinx Spartan6 FPGA and evaluate the leakage energy savings on a set of ITC99 and Opencores benchmarks.

1. INTRODUCTION

As the rapid growth of FPGA applications in various domains, especially in portable digital applications and remote sensing, energy efficient FPGA designs have drawn a great deal of attention in the community [4][7][9].

The existing energy optimization strategies conduct pre-silicon voltage tuning in order to reduce the energy consumption [9][14] . However, these approaches cannot provide optimal solutions considering the fact that there is process variation (PV) [6] during the IC manufacturing period. As PV may vary the IC key properties, such as delay and power, from their nominal specifications, one may argue that the approaches proposed in [7] and [14] during the pre-silicion stage are no longer optimal after manufacturing due to the impact of process variation.

In order to consider and compensate for the impact of process variation on energy efficient FPGA designs, we conduct energy optimizations during the post-silicon stage after the IC is manufactured. Our key observation is that threshold voltage plays an important role in the leakage energy consumption, as shown in Equation (1) [10]:

$$E_{leakage} = 2 \cdot n \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (\frac{kT}{q})^2 \cdot D \cdot V_{dd} \cdot e^{\frac{\sigma \cdot V_{dd} - V_{th}}{n \cdot (kT/q)}} \quad (1)$$

where $E_{leakage}$ is the leakage energy, L is the effective channel length, V_{th} is the threshold voltage, W is the gate width, V_{dd} is the supply voltage, n is the subthreshold slope, μ is the mobility, C_{ox} is the oxide capacitance, D is the clock period, k is the Boltzmann constant, T is the absolute temperature, q is the magnitude of charge on an electron, and σ is the drain induced barrier lowering factor.

It is important to note from Equation (1) that the leakage energy of a transistor or a logic gate decreases exponentially with the increase of the threshold voltage. Also, threshold voltage is the main parameter affected by device aging, such as negative bias temperature instability (NBTI) [16]. Therefore, one can control the threshold voltage by conducting device aging during the post-silicon stage. Based on these observations, we develop a post-silicon device aging-based approach to reduce the total leakage energy consumption on a given FPGA design. Our approach leverages NBTI aging to intentionally stress the FPGA, so that the threshold voltages of selected transistors are increased and thus the leakage energy is decreased exponentially.

However, we face two issues that may impact the effectiveness and applicability of the proposed approach on FPGAs. First, it is well known that NBTI mainly affects the threshold voltage of the PMOS transistors while having little impact on the NMOS transistors [16]. Second, aging impacts the speed of the design and may introduce performance degradations to the target FPGA.

For the NMOS transistors, we select input vectors for the unused NMOS transistors so that their leakage energy can be minimized. Consequently, the leakage energy of the PMOS transistors dominates the total leakage consumption of the FPGA, which can be reduced by NBTI aging.

For the delay degradation problem, we selectively age only the unused components of the FPGA, or the components that are off the critical path, so that aging does not impact the critical path delay of the entire design. To achieve

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this goal, we employ a satisfiability (SAT)-based approach to determine the aging input vectors. In this way, we can avoid impacting the performance of the FPGA while still obtaining total leakage energy savings.

2. RELATED WORK

2.1. Low Power FPGA Design

Several research groups developed techniques for low energy FPGA implementation using dual supply and dual threshold voltages and analyzed their benefits [7][9]. Also, several research teams investigated the benefits of dynamic voltage scaling strategies for reducing power and/or energy in FPGA-based systems [5][15]. Our aging-based approach has an advantage over the existing pre-silicon approaches in that it exploits precise information about benefits and limitations due to slow-down of each specific gate. Related techniques can be also found in [19] and [20].

2.2. Adaptive Body Biasing

Adaptive body biasing (ABB) has been widely adopted as an efficient post-silicon approach for leakage energy reduction and performance optimization [8][13].

However, due to the impact of process variation, every gate varies from its nominal specifications in a different way and, consequently, there does not exist a single or small number of body bias values that can compensate for the PV of all gates. Also, the implementation of ABB in the target design requires additional body bias circuitry, which significantly increases the area overhead. More importantly, although the bias voltages can be adapted at runtime, the placement of body bias circuitry has to be determined at the design time, i.e., which components of the target circuit should be grouped in one cluster and applied the same bias voltage. This makes it difficult for the approach to accommodate the systematic and random impacts caused by process variation.

We leverage device aging as the primary post-silicon method to reduce the leakage energy consumption. By leveraging aging instead of ABB for leakage energy reduction, we are able to not only adjust the threshold voltage at the gate level, but also introduce no additional hardware to the target design.

3. PRELIMINARIES

3.1. Energy Model

As discussed earlier, Equation (1) is the gate-level leakage energy model [10], which indicates that the leakage energy of a transistor decreases exponentially with the increase of threshold voltage. This enables us to significantly reduce the leakage energy by stressing the target transistors and thus increasing their threshold voltage.

3.2. Aging Model

We employ the aging model proposed in [3] for our aging process. The V_{th} shift due to NBTI follows fractional power law of the stress time, as shown in Equation (2).

$$\Delta V_{th} = A \cdot e^{\beta V_G} \cdot e^{-E_\alpha / kT} \cdot t^{0.25} \tag{2}$$

where V_G is the applied gate voltage; A and β are constants; E_α is the measured activation energy of the NBTI process; T is the temperature; and t is the stress time.

As aging causes the threshold voltage and thus the delay of the IC to vary from the original values, it has been employed in hardware security applications that are based on side channels of the target ICs [11][12][18]. In this paper, we leverage the potential positive effect of aging on leakage energy reduction in FPGAs.

4. LOW ENERGY FPGA PRE-PROCESSING

We first pre-process the FPGA to identify the configurable logic blocks (CLBs) that consume ultra-high leakage energy compared to other components and mask them from the cell placement. In this way, we exclude the high leakage components from consideration prior to conducting device aging, which significantly reduces the cost of the approach. We achieve this goal by characterizing the gate-level properties, such as leakage power, which can be obtained by measuring the leakage power of the entire circuit and solving a system of linear equations. Furthermore, we employ a scenario-based method to identify the critical paths on the FPGA, which can be used to identify critical and non-critical CLBs.

4.1. Gate-level Characterization

In gate-level characterization (GLC) [17] we recover the gate-level IC properties from global side-channel measurements under the application of various input vectors. For example, when J input vectors have been applied on a target circuit with K gates, the gate-level leakage energy values can be solved using the following linear program (LP):

$$\begin{aligned} Objective: \quad & \min_{1 \le j \le J} \mathcal{F}(err_j) \\ Constraints: \quad & \Sigma_{k=1}^{K} E_{jk} = \tilde{E}_j + err_j \\ & j = 1, \ldots, J \end{aligned} \tag{3}$$

where E_{jk} is the leakage energy of gate k ($k = 1, \ldots, K$) when input vector j ($j = 1, \ldots, J$) is applied; $\tilde{E}_j$ is the measured total leakage energy when the input vector j is applied; err_j is the measurement error; $\mathcal{F}$ is a metric for

quantifying the measurement errors, such as l_1 or l_2 norm. In this LP formulation, E_{jk} can be expressed as a product of its constant nominal value $E_{nom,jk}$ and a scaling factor (due to PV) δ_k, i.e., $E_{jk} = \delta_k E_{nom,jk}$. By solving the LP with δ_k as the variables, we can obtain the value of E_{jk} for each gate k ($k = 1, \ldots, K$).

4.2. Scenario-based Critical Path Identification

Our device-aging based leakage energy reduction approach requires us to identify the unused and non-critical components on the FPGAs, so that we can avoid aging the critical components and compromising the performance. While the unused components can be obtained from synthesis and mapping of the specific application, the identification of the critical paths is non-trivial, as it is impacted by PV.

We design a scenario-based statistical analysis method in order to identify the critical path. In particular, we generate multiple IC instances following the well accepted PV models, such as the Gaussian model [2] and the quad-tree model [6], and determine the critical path on each instance. Then, we summarize the simulation results and obtain the statistics of critical path gates, e.g., how often a specific gate would appear on critical paths considering a number of PV-impacted chips. The statistics provide us with insights on how critical each gate is in terms of its performance.

5. AGING-BASED POST-SILICON LEAKAGE ENERGY REDUCTION

After pre-processing, we conduct our post-silicon leakage reduction steps, including device aging for PMOS transistors and input vector control for NMOS transistors.

5.1. Device Aging for PMOS transistors

Our goal in aging the PMOS transistors for leakage energy reduction is to stress the unused and non-critical CLBs while keeping the critical CLBs unstressed. In particular, the method we use to age a specific gate is to stress the gate, for example, setting its output to a specific signal. Therefore, the very first step in achieving aging of specific gates in the circuit is to determine the input vectors that we can apply to stress the required gates and reduce the total leakage energy consumption. In other words, the problem becomes how to determine the input vectors for an IC that set the inputs of specific gates to specific signals. We note that this problem can be formulated as an input vector selection problem similar with that in [21]:

Aging Input Vector Selection Problem. Given an IC that has N gates, where each gate i ($i = 1...N$) has a required set of signals for its inputs, the aging input vector selection problem aims to find the primary input vector of the IC that satisfies the signal requirements of the N gates.

Similar with [21], we note that the aging input vector selection problem can be translated to a SAT problem, where the signal of each gate is represented by a Boolean expression concerning the primary input signals. By evaluating all the Boolean expressions (i.e., clauses) to be true simultaneously, the SAT problem aims to search for the corresponding primary input vectors, namely aging input vectors.

5.2. Input Vector Control for Unused NMOS transistors

It is well known that NBTI only increases the threshold voltage of PMOS devices while having very limited impacts on the NMOS transistors. Therefore, the aforementioned NBTI-based aging approach only reduces the leakage energy of PMOS transistors on the FPGA. In order to address the issue for NMOS transistors, we conduct input vector control after the aging process, where the goal is to apply input vectors that set the NMOS transistors in the low leakage mode, similar with the techniques introduced in [1]. In this way, the PMOS transistors become dominating in terms of the leakage energy consumption of the FPGA, which has been reduced exponentially using our NBTI aging approach.

6. EXPERIMENTAL RESULTS

We implement the aging-based low leakage energy scheme into the FPGA design flow. In particular, we use Xilinx Spartan6-XC6SLX45 as the FPGA platform to evaluate our approach. We synthesize and map a set of ITC99 and Opencores test benchmarks on the FPGA and evaluate the leakage energy savings based on the leakage power model in Equation (1) and the cell placement results using Xilinx ISE 13.1.

Table 1 shows the resource usage of the test circuits and the leakage energy savings after applying our aging-based approach. The first five columns show the benchmarks and their resource usage on the FPGA. Here we define a "gate" as an internal FPGA gate that is used to build the target design. In the last column, we include the energy saving results (i.e., the percentage of savings compared to the original leakage energy consumption) obtained from aging the unused and non-critical gates. The results indicate that we obtain a substantial amount of leakage energy savings by intentionally aging the unused and non-critical CLBs on the FPGA while maintaining the initial performance of the FPGA.

7. CONCLUSION

We have developed an aging-based post-silicon approach for reducing the leakage energy consumption on FPGAs. The approach leveraged the fact that the leakage energy decreases exponentially with the increase of the threshold voltage, which can be achieved by aging the transistors. In order to minimize the delay degradation due to aging, we selected

Table 1. Leakage energy savings via aging on FPGA. The first five columns show the benchmarks and their resource usage on Xilinx FPGA Spartan6-XC6SLX45. The last column shows the leakage savings after applying our aging-based approach.

Benchmarks	# Gates	# FFs	Used LUTs	Used Registers	Leakage Savings
b14	10,098	245	3.8%	0.5%	35.3%
b15	8,922	449	7.9%	1.2%	34.0%
b17	32,326	1,415	23.5%	3.6%	29.0%
b17_1	39,665	1,415	23.0%	3.6%	29.1%
b18	114,621	3,320	48.9%	7.8%	20.9%
b18_1	108,482	3,320	48.5%	7.8%	21.0%
b22	29,951	735	11.5%	1.3%	32.8%
b22_1	21,772	735	12.0%	1.3%	32.7%
openrisc	44,476	2,021	46.1%	12.6%	21.7%
eth	35,961	10,544	10.9%	4.3%	33.0%
tv80s	5,604	359	6.3%	0.7%	34.5%
usb_funct	9,164	1,746	6.8%	3.1%	34.3%
ac97	8,020	2,199	3.8%	2.2%	35.3%

aging input vectors that only age the unused or non-critical components of the FPGAs by solving a SAT problem. Our evaluation results on Xilinx FPGA platform indicated substantial leakage energy reductions while maintaining the initial performance.

8. REFERENCES

[1] Y. Alkabani et al. Input vector control for post-silicon leakage current minimization in the presence of manufacturing variability. In *DAC*, pages 606–609, 2008.

[2] A. Asenov. Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 μm MOSFET's: A 3-D "atomistic" simulation study. *IEEE Transactions on Electron Devices*, 45(12):2505–2513, 1998.

[3] S. Chakravarthi et al. A comprehensive framework for predictive modeling of negative bias temperature instability. In *IRPS*, pages 273–282, 2004.

[4] D. Chen et al. LOPASS: a low-power architectural synthesis system for FPGAs with interconnect estimation and optimization. In *IEEE Transactions on VLSI Systems*, 18(4), 2010.

[5] C. Chow et al. Dynamic voltage scaling for commercial FPGAs. In *FPT*, pages 173–180, 2005.

[6] B. Cline et al. Analysis and modeling of CD variation for statistical static timing. In *ICCAD*, pages 60–66, 2006.

[7] A. Gayasen et al. A dual-Vdd low power FPGA architecture. In *FPL*, pages 145–157, 2004.

[8] J. Gregg et al. Post silicon power/performance optimization in the presence of process variations using individual well-adaptive body biasing. *IEEE Transactions on VLSI Systems*, 15(3):366–376, 2007.

[9] F. Li et al. Low-power FPGA using pre-defined dual-Vdd/dual-Vt fabrics. In *FPGA*, pages 42–50, 2004.

[10] D. Markovic et al. Ultralow-power design in near-threshold region. In *Proceedings of the IEEE*, 98(2):237–252, 2010.

[11] S. Meguerdichian et al. Using standardized quantization for multi-party PPUF matching: Foundations and applications. In *ICCAD*, pages 577–584, 2012.

[12] S. Meguerdichian et al. Matched public PUF: ultra low energy security platform. In *ISLPED*, pages 45–50, 2011.

[13] G. Nabaa et al. An adaptive FPGA architecture with process variation compensation and reduced leakage. In *DAC*, pages 624–629, 2006.

[14] P. Pant et al. Dual-threshold voltage assignment with transistor sizing for low power CMOS circuits. In *IEEE Transactions on VLSI Systems*, 9(2):390–394, 2001.

[15] A. Rahman et al. Evaluation of low-leakage design techniques for field programmable gate arrays. In *FPGA*, pages 23–30, 2004.

[16] W. Wang et al. The impact of NBTI on the performance of combinational and sequential circuits. In *DAC*, pages 364–369, 2007.

[17] S. Wei et al. Gate-level characterization: Foundations and hardware security applications. in *DAC*, pages 222–227, 2010.

[18] S. Wei et al. The undetectable and unprovable hardware Trojan horse. In *DAC*, Article No. 144, 2013.

[19] S. Wei et al. Low power FPGA design using post-silicon device aging (abstract only). In *FPGA*, page 277, 2013.

[20] S. Wei. Minimizing leakage energy in FPGAs using intentional post-silicon device aging. (Master's thesis). University of California, Los Angeles. ProQuest/UMI, 2013.

[21] S. Wei et al. Provably complete hardware Trojan detection using test point insertion. in *ICCAD*, pages 569–576, 2012.