Devices and circuits for HF applications based on 2D materials

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***Abstract*— Graphene and related 2D materials have been extensively studied in recent years. As a result, numerous components have been developed for a wide range of applications in high frequency electronics and telecommunications. These include graphene field effect transistors (GFET) which can be used to provide amplification functions, splitters and photodetectors for optical mixing. Recently, 2D materials have also demonstrated their ability to be used as analog switches to transmit very high frequency signal, based on their ultimate thickness. This paper describes some of the methods used to manufacture these devices and circuits, as well as the characterization of their performance.**

***Index Terms*— Graphene, graphene transistors, high frequency electronics, RF switches**

I. Introduction

Graphene is considered to be one of the first two-dimensional material discovered this century [1-3]. Based on its properties, graphene is a very interesting material for many applications [4]. If we consider applications in microelectronics, a large scale material is needed. Researchers are continuing to improve the growth of graphene and graphene-related materials to obtain high electrical properties [5, 6].The epitaxial graphene growth on silicon carbide substrate (SiC) is used in this work [7-10]. For this graphene, it is not necessary to carry out a transfer before manufacturing the devices. Once the graphene grown, a high quality micro-fabrication process is required to obtain high-performance components.

In this work, we describe the fabrication technology we used to fabricate top-gated graphene field effect transistors (GFET) on SiC. After fabrication, we explored the high frequency performance of GFETs. The details of the characterization procedure will be highlighted.

In the last section, a recent result relating to an RF resistive switch will be described. This device is fabricated using a monolayer of MoS_2 (molybdenum disulfide) produced by chemical vapor deposition (CVD) and transferred on our samples during the fabrication process. The performance of these state-of-the-art (SOA) switches will also be described.

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II. Process technology for GFET fabrication

A. Materials under consideration

Epitaxial graphene used in this work was grown by chemical vapor deposition on a high-resistivity 6H-SiC substrate with a thickness of 500 µm thickness. Details of graphene growth are described in ref [8-9]. Fig.1 shows atomic force microscopy (AFM) image of the surface at room temperature. Here, we show 60 µm x 60 µm scan size image of the graphene surface morphology and the presence of steps which always appears on SiC surface. The surface could show some inhomogeneity at a nanometer scale, as it can be seen in Fig.1(a) (inset), here the light color indicates 1.95 nm of the maximum height.

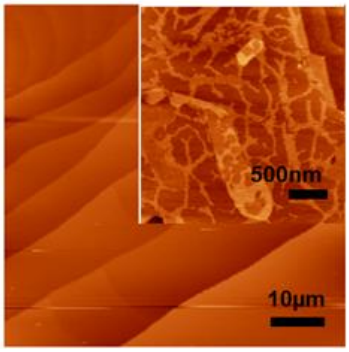

Fig. 1. AFM image of 60x60 µm^2. The inset is a zoom of the surface of graphene on SiC.

To investigate farther more the graphene quality and number of layers Raman spectroscopy was performed, at a laser wavelength of 473 nm, and 1 µm laser spot size in different position of the sample.

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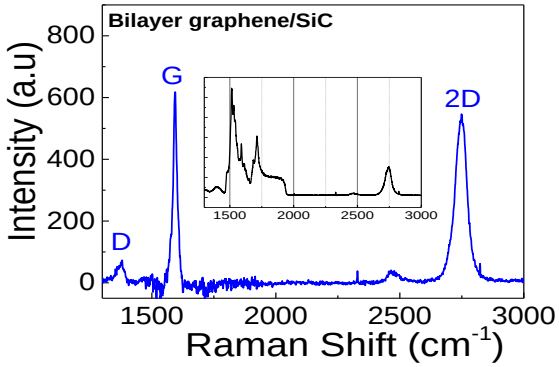

Fig. 2. The Raman spectrum of the bilayer graphene on SiC. The inset shows the Raman spectrum of SiC substrate.

Figure 2 shows an example of the Raman spectrum acquired between 1300 and 3000 cm^{-1} obtained after elimination of the SiC peak, as the substrate peak is close to the graphene peak (Fig. 2 inset). The D peak is generally linked to defect or disorder in the graphene. In our case, the D peak is small indicating local good quality of the graphene. The peaks at 1592 cm^{-1} and 2749 cm^{-1} correspond respectively to the G and the 2D band. It is possible to identify number of layer comparing the G peak intensity I(G) the 2D peak intensity I(2D) [11]. The ratio of the I(2D)/I(G) peaks is 0.83 which suggesting a bilayer graphene. The full width at half maximum (FWHM) of the G and 2D band are respectively equal to 23 and 59 cm^{-1}.

The carrier density and mobility measured on this bilayer graphene are $8.3x10^{12}$ cm^{-2} and 850 $cm^2.V^{-1}s^{-1}$ respectively.

B. Device structure and fabrication process.

The main structure of RF transistors developed in this work is illustrated on the Fig. 3. Fig. 3(a) shows a typical dual gate topology inserted in a coplanar access line for on-wafer measurements.

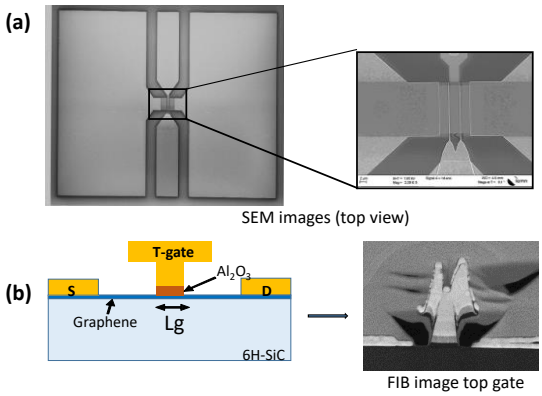

Fig. 3. (a) Top view of the transistor structure at the end of process, (b) Schematic of the side view of the top-gated transistor (left) and Focus Ion Beam (FIB) image of the side view of one gate (right).

Fig. 3(b) illustrates the cross section (left) and the focus ion beam microscope image of the top gate (right).

Figure 4 (a) shows the layout of the transistor produced. The electron-beam lithography is used for all stages of the fabrication process. (i) The first step in the manufacturing process is toelectrically isolated the device. To this end, graphene is etched all around the transistor region, leaving only the active part region and the source-drain contact regions. Holes (micrometric and nanometric sizes) are also created in the contact regions during the same electron-beam lithography process, to ensure low contact resistance by etching holes under the graphene contacts [12]. These holes also improve the adhesion of the gold to the graphene, which is used for the source and drain contacts. (ii) The thin source and drain contacts near the gate region (Ni-1.5 nm)/ Au-30 nm) by the standard lift-off process and metal evaporation. (iii) The dual T-gate of 150 nm length (L_g) were defined by using three layers of poly-meta-methacrylate (PMMA) resist followed by multi-steps electron beam lithography. Then the gate oxide is deposited using four times 2 nm of evaporated Aluminum, following by oxidation in ambient air during 24H. The final oxide thickness is about 15 nm of Al_2O_3. The Ni (50nm) / Au (300nm) gate contact is then evaporated followed by lift-off Fig. 4 (b). (iv) Finally the coplanar waveguide accesses of source, drain and gate are fabricated also using the lift-off process. The evaporated metal is Ni (50nm) / Au (300nm). Fig. 4 (c) shows the final structure of GFET.

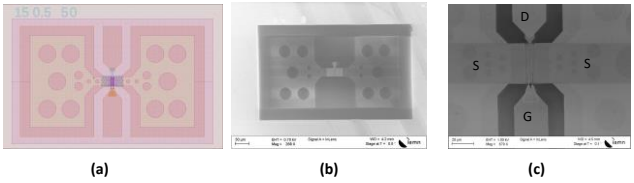

Fig. 4. (a) Layout of the GFET, (b) GFET after metallizations in the active region of GFET, (c) Final device with coplanar waveguide accesses.

III. DEVICE CHARACTERIZATION

After device fabrication, electrical measurements were performed to extract typical I-V characteristics and RF performance. The GFET under characterization shows gate length L_g=150nm and gate width of 2x15µm. The measurements were carried out using a standard probe station with Microtech's probes. The DC and the RF measurements of the transistors were performed with the Semiconductor Analyzer HP4155A and the Vector Network Analyzer Rohde & Schwarz ZVA67. A common calibration procedure of Line-Reflect-Reflect-Match (LRRM) was made before measurement.

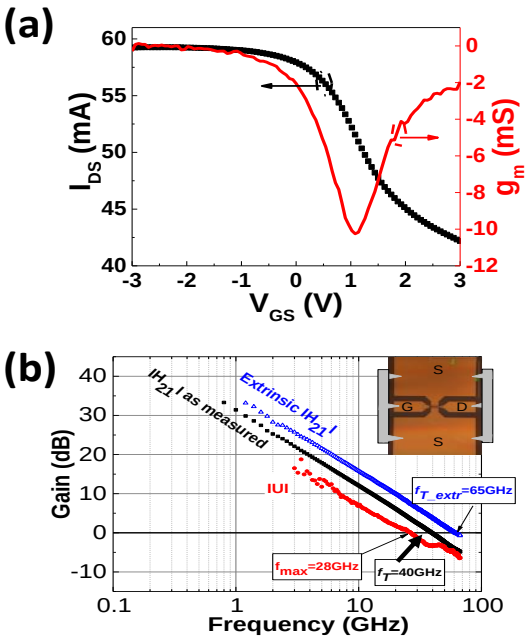

Fig. 5. Performance of GFET on SiC: (a) DC characteristics of bilayer graphene on SiC with L_g = 150 nm, W = 2x15 µm. The evolution of the drain current I_D and the transconductance g_m as a function of the gate voltage V_{GS} at V_{DS}=+1.5V, (b) RF gain performance measured on the probes plan (as measured) and the de-embedded values from which cut-off frequencies are deduced (f_t, f_{max} and extrinsic value f_{textr}.

Figure 5 shows, shows the variation of the transconductance $g_m = dI_{DS} / dV_G$) as a function of the gate voltage. The peak of g_m reaches 10 mS (600 mS/mm) in absolute value at V_{GS} = +1V and V_{DS} = +1.5 V. Fig. 5(b) shows, for a top-gated GFET on SiC substrate, the current gain and unilateral gain deduced from the as-measured S-parameters, in the probe plans. From these gains, we deduce the current gain cut-off frequency (f_T) of 40 GHz and the maximum oscillation frequency (f_{max}) of 28 GHz, in the probe planes. These "as measured" performance included the impact of the coplanar waveguide accesses.

For de-embedding procedure, specific structures such as “open” and “mute” structures are used, as illustrated in our previous work [13] to extract extrinsic performance. The extrinsic current gain cut-off frequency (f_{T_extr}) performance of 65 GHz is deduced from measurements carried out on this GFET.

IV. Illustration of Circuits Based on GFET

When considering development of RF circuits using new device technology, the analysis of reliability of the process, and the yield of resulting devices, is of primary importance. This required a statistical analysis, from material properties to RF performance. This kind of analysis reveals the correlation between performances of the circuits and local properties of substrates [14]. The reliability of the process developed for GFET is sufficiently solid for circuit manufacture to be considered.

A. *Circuit on SiC*

The circuit fabricated here is a balun or splitter circuit based on GFETs, that transform the single-ended signals (unbalanced) into the differential signals (balanced) and vice versa. Thus, the balun is a device that consists of an unbalanced single-ended input port and two balanced output ports. The active balun circuit based on the integrated differential pair architecture of GFET is considered here. The main advantage is the small area and the potential low power consumption. Fig. 6(a) shows the electrical circuit considered and Fig. 6(b) shows the final circuit fabricated.

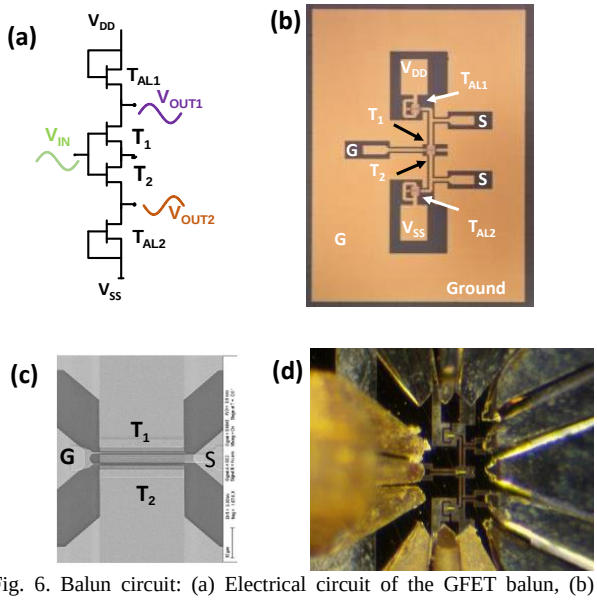

Fig. 6. Balun circuit: (a) Electrical circuit of the GFET balun, (b) Optical image of the balun circuit fabricated, (c) SEM image of T1 and T2 configuration highlighting the layout; (d) Photography of the balun circuit under measurement condition. Chip size is 0.19mm².

The GFET balun is made up of two GFET transistors T_1 and T_2 whose the common source is connected to the ground (single gate transistor) Fig. 6(c). The GFETs T_{AL1} and T_{AL2} are connected as source-drain resistors. The layout of the balun circuit based on GFETs is introduced in the same mask as the previous GFETs, and the same process steps are used. The circuit is fabricated simultaneously on the same substrate with the previous GFETs on SiC substrate. The dimension of the GFET in balun circuit is changed to improve the reliability of the circuit. Therefore, the GFET used in this circuit shows gate length L_g=240nm and gate width of 24µm. for T_1 and T_2.

First functionality test have been performed using time domain measurement using a RF source set at 100MHz and -10dBm. One single RF probes is used at the input while a differential probe is used at the output. Two other RF probes are used for convenience to apply the DC bias. +2V and -2V are respectively applied on V_{DD} and V_{SS}. Also, 2V is applied on the input thanks to a bias tee. Figure 6(d) shows photography of the balun under measurement condition.

Figure 7(a) shows the measurements that reveal the circuit is working as expected. Indeed, the circuit show 180° phase shift between the two outputs. However, and attenuation of 20 dB can be observed. This is directly correlated to the transistor performances and especially to the voltage gain of GFET which remains lower (low transconductance combined to high conductance).

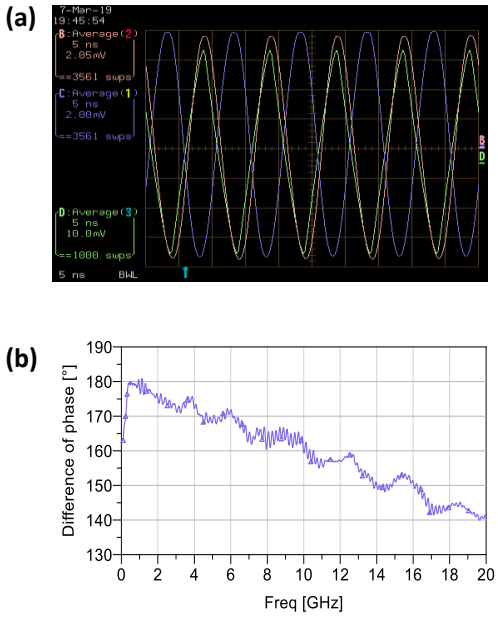

Fig. 7. Performance of balun circuit (a) Oscilloscope measurement when applying a sinusoidal input voltage with an amplitude of 32mV at the input (channel D-Green) and sensing the two outputs (channel B-Orange and C-violet); (b) Three port S parameters measurement up to 20 GHz using a PNAX: phase difference between the two outputs.

The RF characterization of this circuit was made under a differential measurements using the 4 port PNAX vector network analyzer from Keysight, to obtain calibrated datas at the probe level. For the differential measurement, the intermediate frequency is set to 100 Hz and the input power is fixed to -10 dBm. The setup is calibrated using a calibration kit dedicated to differential probes. The details on the measurements are described in the reference [15].

From S parameters measured, the other factor of merit such as a phase difference between two outputs is extracted. Fig. 7(b) shows that phase difference betwwen two outputs is less than 10° up to 6 GHz.

V. RF SWITCHES

The nonvolatile resistive switching phenonmenon in monolayers and multilayers materials [16] is promising for electronic applications. Because of the ultimate thickness of 2D layers, analogue RF switches based on 2D materials shows a favorable scaling of the cut-off frequency versus device size [17] [18], compared to other emerging technologies. We have design switches consisting of a vertical junction made of metal electrode/ 2D material/metal electrode. The 2D material for this work is molybdenum-disulfide (MoS_2) which acts as switching material. The switching is activated by applying positive or negative bias to the device. This device is embedded in a coplanar waveguide for DC and RF measurements. Figure 8(a) shows the scanning electron microscope (SEM) image of the switch and Fig. 8(b) the top view of the switch embedded in the coplanar waveguide. The fabrication process of this kind of switches is described in ref. [19].

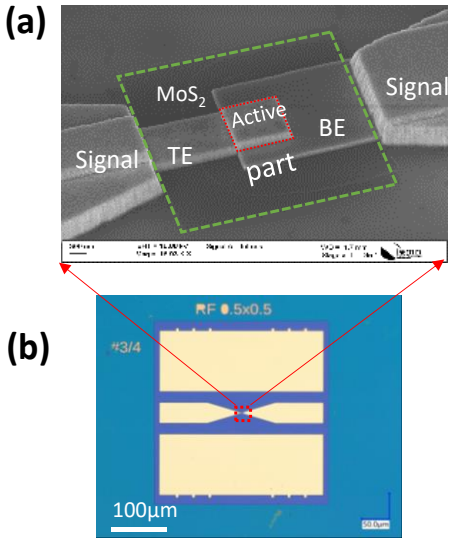

Fig. 8. (a) SEM image of the vertical resistive switch with gold as bottom electrode (BE), MoS_2 as dielectric and gold as top electrode (TE). The active size is 0,5µm x 0.5 µm; (b) Resistive switch embedded in a coplanar waveguide for RF applications.

The DC measurement Fig. 9(a) shows that the switch is in a high-resistance state (HRS) until the application of a SET voltage, which brings the device into a low-resistance state (LRS). This state persists until a negative bias is applied (RESET) to force the switch into a high-resistance state.
RF measurement is performed from [0.25 – 480] GHz using a four VNA working on four frequency bands: 0.25– 110 GHz / 140-220 GHz / 220-325 GHz / 325-480 GHz.

From measured S parameters (Fig. 9(b)), it appears that in the ON state, the power loss of the switch is around -1dB @ 300GHz, and large attenuation across the switch in the OFF state (isolation around -20dB @300GHz). The factor of merit of RF switches extracted from measurement are R_{on}=8Ω, C_{off} = 0,9fF, Fc=22 THz. These performances are sufficient to perform data communication experiments for 6G @300 GHz.

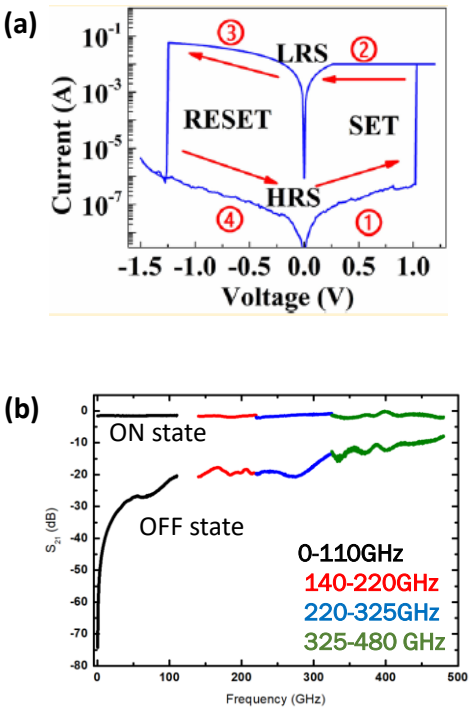

Fig. 9. (a) DC characteristics of resistive switch showing a switching voltage of 1V and reset around -1.25V; (b) Transmissission coefficient of RF switch in the ON state (lower lost), and in the OFF state. Lost over 15 dB up to 320 GHz.

VI. Conclusion

These results achieved in this work show that graphene technology, characterization and modelling techniques are mature enough, and allow today to move from RF devices to integrated RF circuit. This methodology could be transfer easily to the other new emerging 2D materials as transition metal dichalcogenides and other's. The performances achieved when RF devices and circuits are considered remains lower compared to the conventional technologies, which is not surprising given that graphene and related 2D materials remain new materials, and the improvement of their performance still ongoing. These aspects will be discussed during the oral session, as well as new device concept for HF switches (over 100 GHz).

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References

[1] A. K. Geim, K. S. Novoselov, "The rise of graphene", *Nature Materials*, vol. 6, pp. 183-191. 2007.

[2] A. K. Geim, "Graphene: Status and prospects," *Science*, vol. 324, no. 5934, pp. 1530–1534, Jun. 2009

[3] C. Berger, Z. Song, T. Li, X. Li, A. Y. Ogbazghi, R. Feng, Z. Dai, A. N. Marchenkov, E. H. Conrad, P. N. First, and W. A. de Heer," Ultrathin Epitaxial Graphite: 2D Electron Gas Properties and a Route toward Graphene-based Nanoelectronics", J. Phys. Chem. B 2004, 108, 19912-19916

[4] K. S. Novoselov, V. I. Fal′ko, L. Colombo, P. R. Gellert, M. G. Schwab, and K. Kim, "A roadmap for graphene," Nature, vol. 490, no. 7419, pp. 192–200, Oct. 2012.

[5] K.-J. Tielrooij, N. C. H. Hesp, A. Principi, M. B. Lundeberg, E. A. A. Pogna, L. Banszerus, Z. Mics, M. Massicotte, P. Schmidt, D. Davydovskaya, D. G. Purdie, I. Goykhman, G. Soavi, A. Lombardo, K. Watanabe, T. Taniguchi, M. Bonn, D. Turchinovich, C. Stampfer, A. C. Ferrari, G. Cerullo, M. Polini, and F. H. L. Koppens, "Out-of-plane heat transfer in van der waals stacks through electron–hyperbolic phonon coupling," Nature Nanotechnology, Nov. 2017

[6] L. Banszerus, M. Schmitz, S. Engels, J. Dauber, M. Oellers, F. Haupt, K. Watanabe, T. Taniguchi, B. Beschoten and C. Stampfer "Ultrahigh-mobility graphene devices from chemical vapor deposition on reusable copper", Science Advances 31 Jul 2015: Vol. 1, no. 6, e1500222, DOI: 10.1126/sciadv.1500222

[7] C. Berger, Z. Song, T. Li, X. Li, A. Y. Ogbazghi, R. Feng, Z. Dai, A. N. Marchenkov, E. H. Conrad, P. N. First, and W. A. de Heer, " Ultrathin Epitaxial Graphite: 2D Electron Gas Properties and a Route toward Graphene-based Nanoelec-tronics", J. Phys. Chem. B 2004, 108, 19912-19916

[8] W. Strupinski, K. Grodecki, A. Wysmolek, R. Stepniewski, T. Szkopek, P. E. Gaskell, A. Grüneis, D. Haberer, R. Bozek, J. Krupka, and J. M. Baranowski, "Graphene epitaxy by chemical vapor deposition on SiC," Nano Lett., vol. 11, no. 4, pp. 1786–1791, Apr. 2011.

[9] T. Ciuk and W. Strupinski, "Statistics of epitaxial graphene for hall effect sensors," Carbon, vol. 93, pp. 1042–1049, Nov. 2015.

[10] E. Pallecchi, F. Lafont, V. Cavaliere, F. Schopfer, D. Mailly, W. Poirier, and A. Ouerghi, "High electron mobility in epitaxial gra-phene on 4H-SiC(0001) via post-growth annealing under hydrogen," Scientific Reports, vol. 4, Apr. 2014.

[11] A. C. Ferrari, "Raman spectroscopy of graphene and graphite: Disorder, electron–phonon coupling, doping and nonadiabatic effects," Solid State Communications, vol. 143, no. 1-2, pp. 47–57, Jul. 2007.

[12] V. Passi, A. Gahoi, J. Ruhkopf, S. Kataria, F. Vaurette, E. Pallecchi, H. Happy, and M. C. Lemme, "Contact resistance study of " edge-contacted" metal-graphene interfaces," in *2016 46th European Solid-State Device Research Conference (ESSDERC)*. plus 0.5em minus 0.4emIEEE, Sep. 2016, pp. 236–239.

[13] L. Nougaret, H. Happy, G. Dambrine, V. Derycke, J. -P. Bourgoin, A. A. Green, and M. C. Hersam, "80 GHz field-effect transistors produced using high purity semiconducting single-walled carbon nanotubes, Appl. Phys. Lett., vol. 94, p. 243505, (2009)

[14] D. Fadil, W. Wei, M. Deng, S. Fregonese, W. Strupinski, E. Pallecchi, H. Happy, "2D-Graphene Epitaxy on SiC for RF Application: Fabrication, Electri-cal Characterization and Noise Performance", Published in IEEE MTT-S International Microwave Symposium (IMS) 2018, Philadelphia, PA, USA, pp. 228- 231. DOI:10.1109/mwsym.2018.8439655

[15] Fadil, D.; Passi, V.; Wei, W.; Ben Salk, S.; Zhou, D.; Strupinski, W.; Lemme, M.C.; Zimmer, T.; Pallecchi, E.; Happy, H.; et al. A Broadband Active Microwave Monolithically Integrated Circuit Balun in Graphene Technology. Appl. Sci. 2020, 10, 2183. https://doi.org/10.3390/app10062183

[16] R. Ge *et al.*, "A Library of Atomically Thin 2D Materials Featuring the Conductive-Point Resistive Switching Phenomenon," *Adv. Mater.*, vol. 33, no. 7, p. 2007792, Feb. 2021, doi: 10.1002/adma.202007792.

[17] R. Ge *et al.*, "Atomristor: Nonvolatile Resistance Switching in Atomic Sheets of Transition Metal Dichalcogenides," *Nano Lett.*, vol. 18, no. 1, pp. 434–441, Jan. 2018, doi: 10.1021/acs.nanolett.7b04342.

[18] M. Kim *et al.*, "Analogue switches made from boron nitride monolayers for application in 5G and terahertz communication systems," *Nat. Electron.*, vol. 3, no. 8, pp. 479–485, Aug. 2020, doi: 10.1038/s41928-020-0416-x.

[19] Kim, M., Ducournau, G., Skrzypczak, S. *et al.* Monolayer molybdenum disulfide switches for 6G communication systems. *Nat Electron* **5**, 367–373 (2022). https://doi.org/10.1038/s41928-022-00766-2