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Abstract

A Printed Circuit Board (PCB)-embedding process using pressed metal foam to connect the top-side pads of power dies is considered. The manufacturing process, simple and highly cost-effective, is described in detail; samples are manufactured and their reliability and robustness are characterised. It is shown that thermally cycled prototypes exhibit reliability close to that of Direct Bounded Copper (DBC) substrates. Samples submitted to 150 A-surges have highly scattered reliability. SiC MOSFETs submitted to destructive current limiting tests and repetitive short-circuit tests performed similarly to dies reported in TO247 packages. A discussion on the development of reliability-assessment-methods, especially suited for PCB-embedding processes, is proposed.

1   Introduction

Although wire-bonding processes are mature and fully mastered, they have limited performances. For instance, wire bonds can account for more than half of the conduction loss of a packaged low-voltage transistor while adding an inductance in the order of ten nanohenries. Furthermore, wire-bonded dies can only be cooled from their bottom-sides. Last, wire bonds have limited reliability and robustness [1].

These limitations call for a new way to connect the top-sides of dies. Many academic and industrial researchers [2, 3, 4] tackle this issue, using copper [5] or aluminium [6] ribbons or a flexible Printed Circuit Board (PCB) [7] instead of aluminium wires, using pressed contacts made with spring-like metal wool [8] or made of plain metal [9, 10].

Embedding the dies within the PCB-substrate itself is another approach to wire-bond-free components and modules [11, 12, 13, 14, 15, 16]. As a matter of fact, in such device, the top-side pads of the dies are often connected by a layer of copper electrodeposited on the top of the dies. This process, however, is rather complex and costly since it involves sputtering seed layers on the top-side metallisation layers of the dies, which is seldom compatible with today's PCB factories. Some publications tackled the reliability of these assemblies. In [17], it is reported that all samples passed 1000 thermal cycles between -55 °C and +125 °C without showing any delamination but no

electrical measurement was made. In [12], a reduced temperature swing was used ($\Delta T_j < 90$ K) and none of the aged sampled reached the failure criteria, defined as a 10 % increase in IGBT saturation voltage, after 400 k cycles.
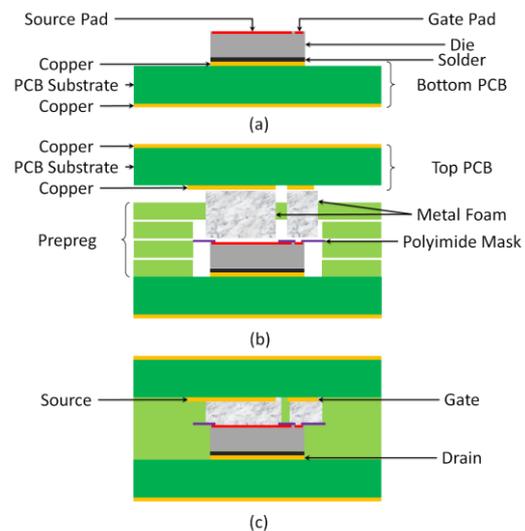

Fig. 1. Embedding of a MOSFET using pressed metal foam. (a): the die is soldered on the bottom PCB; (b): prepreg layers, a polyimide mask & pieces of metal foam (one for each top-side pad) are positioned; (c): the stack is laminated, the epoxy resin polymerizes and floods the foam.
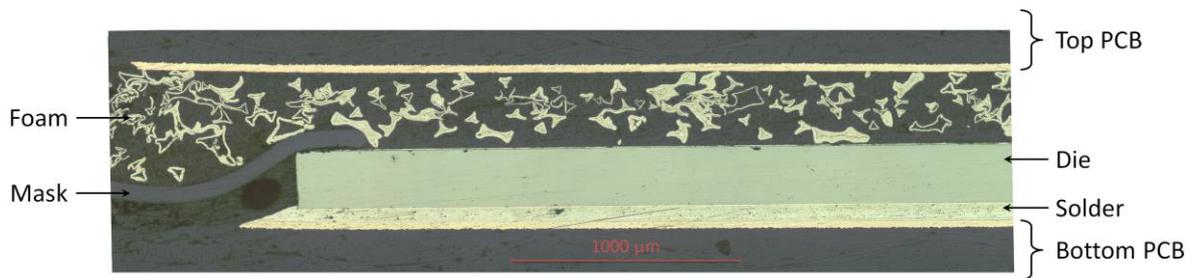
Fig. 2. Partial cross-sectional view of an embedded diode. The die is 250 μm-thick and 6.5 mm-wide.

In [18], we proposed a new technique to connect the top-side of a die, using a pressed contact made of metal foam. This paper deals with the reliability and the robustness of this process. Various sources of stress were experimentally investigated: samples were thermally cycled, submitted to current surges and submitted to short-circuit tests. These tests were intended, depending upon the nature of the stress applied, either to assess the reliability and robustness of the connection itself, or to ensure that the proposed packaging process does not degrade the reliability and robustness of the die. Few samples were submitted to each test, hence the limited statistical significance.

Additionally, a discussion on the relevance of defining new reliability indicators, suited to PCB-embedded power electronics, is proposed.

2 Packaging process

The manufacturing process is quite straightforward; it consists of only three steps. First, the bottom side of the die is soldered on a "bottom PCB" (Fig. 1.a). Then, the bottom PCB (and the die), layers of prepreg, a polyimide mask (with one hole placed above each top-side pad of the die), a piece of metal foam for each top-side pad, and the top PCB are stacked (Fig. 1.b). This is then laminated, as specified by the prepreg manufacturer (Fig. 1.c).

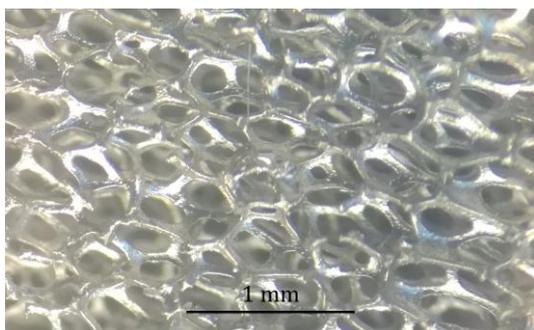The mask allows using pieces of foam wider than the pads and roughly positioning them above it. As a

matter of fact, provided that the polyimide mask is precisely positioned above the die (i.e. that the holes in the mask are aligned with the pads), it will prevent the foam, slightly distorted during the lamination process, from short-circuiting adjacent pads (cf. Fig. 1.c).

The foam is neither soldered, nor sintered, nor glued to neither the copper nor the die; it is solely pressed between the top-PCB and the die and kept in place by the epoxy resin.

Nickel foam Ni-5763 was used [19]. It is mainly composed of nickel (99.5 %), alloyed with iron (0.2 %), copper and zinc (0.1 % each). The foam thickness and porosity before lamination were, respectively, 1.4 mm and 96 % whereas they drop to about 300 μm and 70 %, respectively, afterward.

In spite of its rather high porosity (see Fig. 2) and thanks to its three-dimensional structure (Fig. 3), the foam is able to carry current between the die and the top PCB and thereby electrically connect them.

3 Aging with high-intensity current pulses

3.1 Motivation

Fig. 2 and Fig. 4 show that the contact between the foam and the die top-side metallisation are highly localised. This will induce local high current densities that, in conjunction with the contact resistance, might induce hot-spots at these points. These might be highly stressful to both the die and the package.
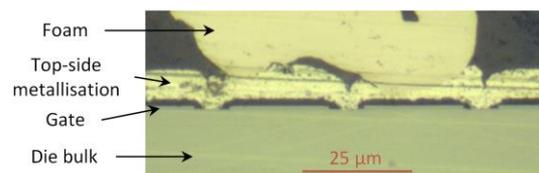

Fig. 3. Photography of the foam before lamination.

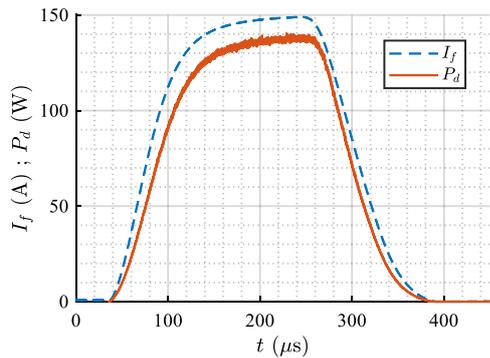Fig. 4. Cross-sectional view of a contact between the foam and the die.

Fig. 5. Current and dissipated power during a current surge.

3.2 Method

To investigate this potential failure mechanism, current pulses with amplitude 150 A and duration 200 μs (Fig. 5) were forced through diodes embedded using the process under study. The diodes were 60 V–18 A -rated and the die size was 4.2 mm × 6.5 mm × 250 μm. The pulse amplitude and duration were chosen low enough so that the mean die temperature would remain close to the ambient temperature whereas the energy of each pulse would be high enough to induce metallurgical changes at the interface between the foam and the die.

The peak mean current density in the die was close to 700 A/cm². The pulses frequency was 12.5 Hz and each pulse delivered 30 mJ to the device; the mean dissipated power was thus 0.38 W. The die mean temperature was therefore about 4 K above room temperature. Most of the energy was dissipated within the diode junction. Assuming that, throughout the pulse, the heating of the die was homogenous and adiabatic, it can be estimated that the temperature of the active region of the die increased by only a few kelvins during a pulse.

In each sample, so as to further intensify the stress on the interface between the foam and the die without increasing the stress on the die itself, a piece of foam much smaller than the die was used: its surface (2 mm × 4 mm, in Fig. 6: $w_f = 2$ mm) was only 30 % that of the die (4.2 mm × 6.5 mm, in Fig. 6: $w_d = 4.2$ mm).

After every 1000 to 10,000 pulses, the static characteristic of the Device Under Test was measured between 0 and 150 A using a Tektronix 371A High Power Programmable Curve Tracer (Fig. 6). Each characteristic was modelled by a resistance series-connected with a voltage-source. This resistance, defined as the derivative of the (V_f, I_f) characteristic at a given current I_f^0, included not only the connection
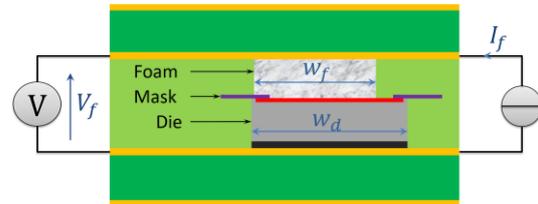

Fig. 6. Kelvin-connection of an embedded diode to the curve tracer: current source and voltage sensing, connected on the right- and left- hand side in the schematic, respectively.

using pressed metal foam, but also the die and the solder.

3.3 Results

One of our samples failed as a short circuit after only 7 k pulses, one failed as an open circuit after 1 M pulses, one has not shown any sign of aging after 13 M pulses. At this point, a wire-bonded die (used as reference) sustained 10 M pulses without showing any degradation.

The evolutions of the elements of the model of a sample are given in Fig. 7. The shape of the resistance curve compares with that observed during a bond wire lift-off [1].

Optical observations of metallurgical cuts of failed devices did not reveal any sign of degradation. In particular, no fracture in the resin surrounding the foam could be spotted.

3.4 Conclusions on the aging with current pulses

The foam being a highly non-homogenous medium might explain the dispersion of the results; this would
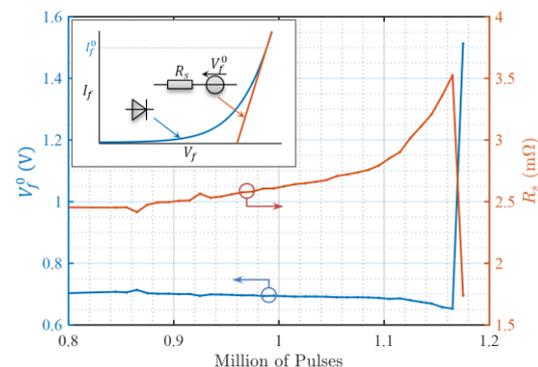

Fig. 7. Inset: measured characteristic (blue) and model (red) of a diode, for a given current I_f^0. Main plot: evolution of the resistance R_s and voltage source V_f^0 modeling a diode packaged using our process until failure – aging by current surges. $I_f^0 = 20$ A.

therefore be a significant limitation to the proposed connecting technic. On the other hand, the dispersion might be due to the process lack of maturity.

Optically studying failed sampled proved to be insufficient to determine the causes of failures. These might be linked to hot-spots on the die or in the foam, or to a degradation of the interfaces between the foam and either the copper of the top-PCB or the aluminium of the die.

4   Passive thermal cycling

4.1   Motivation

As in any compact assembly involving materials with different Coefficients of Thermal Expansion (CTE), thermal cycling can be highly stressful for laminated assemblies. In particular, the high CTE mismatch between standard epoxy-based PCB substrate (usually CTE≈60 ppm/K [20]) and the die (CTE=2.6 ppm/K for silicon, 23 ppm/K for aluminium) can induce cracks or delamination [20, 21].

Furthermore, since the contact between the die top-side metallisation and the foam is only pressed, small relative movements are possible at the interface. This might result in a local matting or abrasion of the top of the die. On the other hand, this could increase the reliability of the assembly by removing the strain otherwise appearing at the feet of bond wires and responsible for plastic deformations [21].

The reliability of eight dies embedded using our process was therefore assessed through passive thermal cycling.

4.2   Method

Eight diodes with die size 4.2 mm × 6.5 mm were embedded using the proposed process. They were then placed in a climatic chamber and thermally cycled between $-40\ ^\circ\text{C}$ and $150\ ^\circ\text{C}$. Each cycle lasted 70 min, including 15 min-long dwell times. The temperature slope was less than 8 K/min.

4.3   Results

Before and after 220 cycles, the resistances of the samples were measured (at $I_f^0 = 10$ A) and compared (cf. Fig. 8). The resistance of all the diodes increased, by 5 % to 108 %; the mean increase was 54 %.

The blocking capabilities of the components, on the other hand, were not affected by the test. This likely indicates that the dies were not damaged and
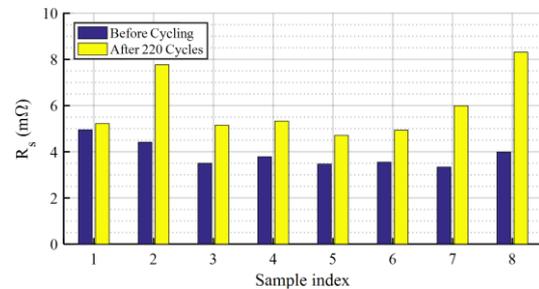

Fig. 8. Resistance of diodes packaged using our process before and after thermal cycling; $I_f^0 = 10$ A

that the pressed contacts themselves evolved during the aging.

Metallurgical cuts were made on aged assemblies and studied using an optical microscope but no sign of degradation, such as delamination (like those reported in [20]), or resin fracture, could be found in any sample.

Most power modules use Direct Bounded Copper (DBC) as substrate, the reliability of which has been widely studied. In [22], delaminations in the solder between the DBC and the base plate appeared after only 25 cycles between -40 °C and 120 °C. In [23], catastrophic failures due to cracks in the ceramic were observed after 200 to 300 -40 °C/150 °C cycles. Similar results were reported in [24, 25].

4.4   Conclusion on thermal cycling

This shows that DBCs submitted to the same harsh test conditions as our prototypes would have likely catastrophically failed whereas the physical integrity of our samples was not impaired. Nevertheless, the very high resistance increase denotes a severe degradation of the assembly, possibly within the foam or at the interface between the foam and either the die or the top-PCB. Such resistance increase is a strong limiting factor for reliability aspects.

Metallurgical cuts were not sufficient to determine failure mechanisms; a more thorough failure analysis will be required to draw definite conclusions.

5   Robustness in Current Limitation Mode

5.1   Motivation

Dies packaged using bond wire have their top-side pads connected in only as many points as the number of bond wires used – usually 2 or 3 in a discrete package such as TO247. On the other hand, in the proposed packaging process, the contact between the foam and the die is disseminated over the entire die
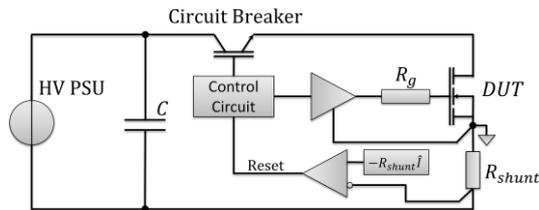
Fig. 9. Schematic of the set-up used in current-limiting tests.

surface. This is an improvement that should result in smaller surface current, and therefore reduced resistive voltage drop, in the top-side metallisation. As a result of it, the potential of the source pad may be expected to be more homogenous and the current more evenly distributed over the cells, thus limiting the risk of hot-spot.

This could result in an improved robustness, in particular to short-circuit tests.

5.2   Method

Transistors were tested in current limiting mode using the set-up shown in Fig. 9: a high-voltage power supply was applied across the Device Under Test (DUT), which was then turn on until failure. A circuit breaker was used to disconnect the power supply after failure, when the current reaches a threshold value $\hat{I}$ and prevent the DUT from exploding.

The current through the DUT was measured using a coaxial shunt (400 MHz, $R_{shunt} = 10$ mΩ, from T&M), the voltage across it was measured using a PHV1000-RO passive voltage probe (400 MHz, 1:100, from PMK), the gate current was measured with a CT2 current probe (200 MHz, 1mV/mA, from Tektronix) and all was monitored using a HDO8108 oscilloscope (12 bits, 1 GHz, 2.5 GS/s, from Teledyne-LeCroy).

Bare dies SiC MOSFETs with reference CPM2-1200-0025b (rating: 1200 V – 98 A – 25 mΩ, with die size 6.44 mm $\times$ 4.04 mm), from Cree were used.

So as to be able to easily perform an optical study of the dies after failure, a custom set-up able to mimic the properties of our process without requiring lamination was designed. Fig. 10 shows a cross-sectional view of the set-up. A stack composed of:
- a bottom PCB – on which the die was soldered;
- a polyimide mask;
- pieces of foam, positioned by a single layer of prepreg (which shall not be cured);
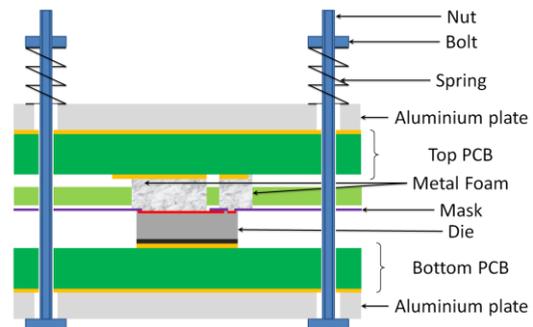- a top PCB;

Fig. 10. Schematic of the press-pack-like mechanical set-up used for the tests.

was placed between two plates of aluminium (required due to the high flexibility of PCB) that were maintained by four bolts and springs. The set-up acted as a press-pack package: the springs applied a pressure of about 3 MPa (close to that otherwise applied during the curing of the prepreg) on the foam and maintained it in contact with the die.

Three prototypes were tested using this set-up whereas a fourth had been fully embedded, laminated.

5.3   Results

5.3.1   Measured waveforms
The gate currents and voltages measured on our samples during a current-limiting short-circuit are given in Fig. 11. Gate leakage current appeared a few µs after the beginning of the test resulting, in conjunction with the 51 Ω-gate resistance, in a decrease in the gate voltage. This current migh denote a gate oxide failure [26]. The shape of the drain current in a representative sample (Fig. 11) was as expected. At first, the rate of the current increase is limited by the test voltage and the loop inductance; subsequent evolutions of the saturation current can be explained by the temperature dependences of the threshold voltage and majority carrier mobility in the channel [27]. From about 3.5 µs after the start of the test, the saturation current starts decreasing due to the drop in majority carrier mobility, later accentuated by the drop in gate voltage due to the gate leakage current.

The peak saturation current was 430 A (i.e. 1.6 kA/cm²), that is 4.4 times the nominal value. This ratio is comparable to those reported in the literature for similar devices [26, 28, 29, 30, 31].
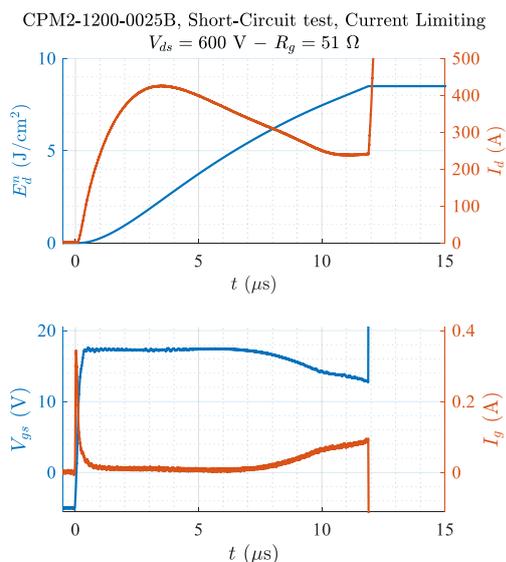
Fig. 11. Waveforms acquired during the tests on a sample: drain current and cumulative dissipated energy (top); gate to source voltage and gate current (bottom).

The drain current, gate voltage, drain-source voltage and gate current are highly similar for all devices, the difference being the time to failure, which varies from 9.3 µs to 12 µs.

5.3.2   *Dissipated energy leading to failure*

The dissipated energy until failure is defined as the amount of energy dissipated in a component until its failure as a short-circuit. The value of this parameter,
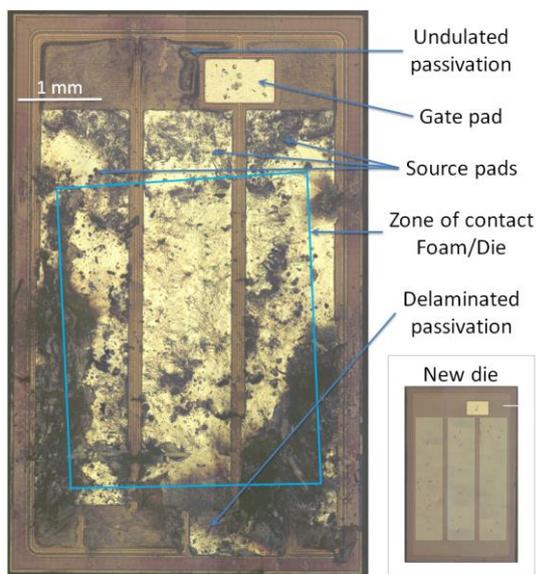

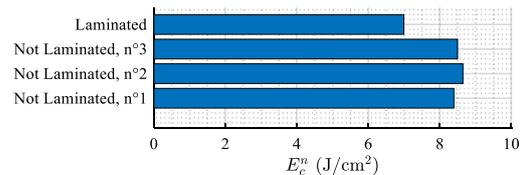Fig. 13. Photography of a die before and after test.

Fig. 12. Energy density leading to failure of CPM2-1200-0025b dies.

normalised by the die area, was calculated for four prototypes and is given in Fig. 12. In spite of the low representativeness of statistics calculated over such a low number of samples, this shows that the results are quite repeatable in so far as the measured values are within ±1.6 % of the mean critical energy for non-laminated samples (i.e. using the press-pack like set-up). Furthermore, Fig. 12 shows that using the press-pack-like package shown in Fig. 10 gives comparable results as laminated devices whilst allowing a more thorough study of failed devices (cf. next section).

Test on dies from the same generation (2nd) of the same manufacturer (Cree), in a TO247 packaged have been reported in the literature. For instance, [26, 28, 29, 30, 31] investigated the dissipated energy leading to failure of a C2M0080120 (80 mΩ – 1200 V) transistor. [28] found it to be 6.9 J/cm² (at $V_{ds} = 600$ V, $R_g = 47$ Ω, $V_{driver} = 18$ V), [26] reported a value only 5 % greater (at $V_{ds} = 600$ V, $R_g = 47$ Ω, $V_{driver} = 21$ V) and analogous results were reported in other papers.

These values are close to those found in the case of dies embedded using the proposed process, suggesting that using a contact made of pressed metal foam or bond wires contributes similarly to a die current limiting robustness.

5.3.3   *Study of failed transistors*

After failure, all sampled had their drains, sources and gates short-circuited. An optical inspection of the dies showed that they were all burned (cf. Fig. 13) and fractured. The passivation of the dies was greatly distorted, showing undulations with characteristic length in the order of a hundred of µm – comparable observations were made in [32]. In some spots, the passivation had even been ejected away from the die (Fig. 13).

Simulations [29, 33, 34, 35] have shown that during a short-circuit test, the temperature of the surface of the die can rise well above the melting point of aluminium (660 °C). The optical study of our samples showed that the top-side metallisation layers of all dies had melted (Fig. 14). The cells clearly stand
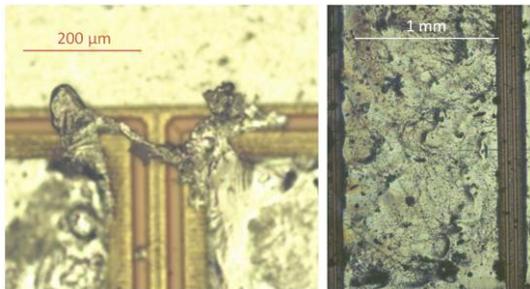
Fig. 14. Melted aluminium above the passivation protecting a gate finger (the dendrite of aluminium is roughly 25 µm-high; left image) and below the piece of foam (right image).

out from the surface of a new die but cannot be distinguished in a failed one. Small waves, demonstration of a flow of liquid aluminium could be spotted, mostly in the regions of the metallisation that were not in contact with the foam. This flow of liquid metal could result, not only from the pressure applied on the die, but also from the Lorentz force due to the interaction between the magnetic field created by the high current density and the electrical charges themselves.

From the moment the component failed and during the time it took the circuit breaker to open the circuit, the current rises rapidly, at a rate mainly limited by the loop inductance. In our set-up, the peak current reached about 4.2 kA and lasted 3.5 µs. There is therefore no way of telling to what extent the damages observed correlates to the device failure or were a consequence of this current spike.

5.4 Conclusion on curent limitation mode tests

These tests show that dies packaged using the proposed process or conventional techniques have similar current limitation mode robustness, which may be explained by the fact that the weakest element of the assembly is, in this test, not the connection but rather the die itself. Still, this shows that the proposed connection technique does not degrade this aspect of the robustness of the die, nor does it seem to increase its dispersion.

Secondly, these tests suggest that our press-pack like set-up (Fig. 10) mimics quite accurately the performances of the complete process.
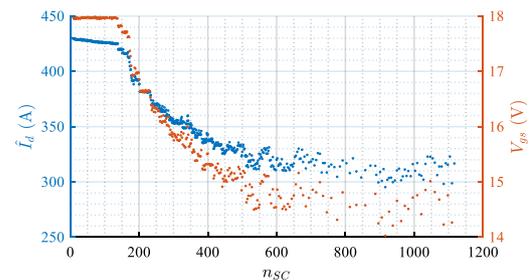

Fig. 15. Peak saturation current (blue) and on-state gate to source voltage (red) vs. number of short-circuits

6 Short-circuit Aging

6.1 Method

The same test bench as in the previous section was used to submit prototypes to repetitive, non-destructive, Short-Circuit (SC) tests. The bus voltage was set to 600 V, the gate voltage was -5/+18 V and the gate resistor was 51 Ω. Two devices were tested in the press-pack-like mechanical set-up shown in Fig. 10 and aged. One was submitted to SCs long enough for a gate leakage current to appear whereas the other was submitted to shorter SCs. Every few short-circuits, the on-state resistance of the DUT, including the die, foam, contacts and solder resistances, was measured. The short-circuit repetition period was 3 s.

6.2 Results – 4.5 µs-long SCs

A prototype was submitted to 4.5 µs-long repetitive short-circuits. The dissipated energy was about 890 mJ (that is 3.4 J/cm²), per SC, i.e. 40 % of the energy leading to failure.

Fig. 15 shows that during the first 140 SC, the saturation current remained quite constant (the decrease was only 1 %); so did the gate voltage, proof that the leakage current was negligible (≪ 1 mA). During subsequent SC, however, a DC gate leakage current appeared, reaching and stabilizing itself around 80 mA after 400 SC. Similar results were found on C2M0080120, which are TO247-packaged MOSFETs from the same generation of the same manufacturer [36] as ours. The conjunction of the gate voltage reduction, a shift of the threshold voltage, and an increase in the on-state resistance of the component (due to the restructuration of the top-side metallisation layer) might explain the drop in saturation current [37]. An optical study of the device after the experiment showed that the top-side metallisation had undergone severe reconstruction, the surface having lost its shine and having become rough. However, the

on-state resistance of the DUT remained constant throughout the entire experiment; evidence that using a contact disseminated over the entire surface of the die is beneficial in term in metallisation layer aging.

6.3   Results –3 µs-long SCs

A sample was submitted to 3 µm-long SC, i.e. short enough so that no gate leakage current appeared. The dissipated energy was about 530 mJ per SC, i.e. 2 J/cm² or 25 % of the energy leading to failure.

After 10 kSC, the decrease of saturation current was negligible (-2 %). Furthermore all changes in on-state resistance could be correlated with ambient temperature variations or explained by the lack of repeatability of the connection of the device to the test-bench.

A TO247-packaged component from the same generation of the same manufacturer as ours was aged in [28, 36, 38]. The test conditions were alike: same bus voltage, same SC duration, comparable ratio between the dissipated energy and the energy leading to failure. It was reported that the resistance increased quite faster: +3.7 % after 3.000 SC.

6.4   Conclusion on short-circuit aging

Notwithstanding their low statistical significance, these tests show that the reliability of SiC-MOSFETs packaged using the proposed process is comparable to that of wire-bonded chips. It thus appears that the proposed connection method does not degrade the performances of the die.

7   Discussion

7.1   Repeatability

We showed in [39] that the process appeared to be quite repeatable since 54 of our 59 embedded diodes had resistances between 3 and 5 mΩ, with a standard deviation of 470 µΩ. Yet, this study shows a great variability among the reliability of the samples.

This apparent paradox might be due to the fact that the resistance due to the packaging is negligible vs. the resistance of the die itself whereas the reliability of the component is – at least for the high-current pulse and thermal cycling tests –primarily defined by the packaging.

Furthermore, the tests were performed on few prototypes and should be conducted on larger sets of samples in order to gain statistical significance.

Hypotheses could explain the high dispersion of the test results. Although most of the steps of the process are simple and mastered, to this point, samples have been manufactured using unautomated laboratory equipment; the repeatability of the process might therefore not be optimal. Additionally, foam is a random medium, which leads to a random distribution of contacts over the die metallization, different from one prototype to another. One could expect pores to be small enough compared to the die area for the contact to be homogenized, but this is yet to be verified.

A more extended study is yet to be conducted so as to improve and assess the process reproducibility. It will then become possible to more thoroughly evaluate the process reliability.

7.2   Reliability indicators for PCB-embedding processes

The structure of assemblies with PCB-embedded dies is fundamentally different from that of standard power modules: no bond-wire is used, not only laminated but also electrodeposited copper layers are used, DBC are typically replaced by organic substrate (potentially anisotropic), the assemblies are more symmetrical: dies can be flipped and the top-side connections are similar to the bottom-side ones. The failure mechanisms of such assemblies might therefore differ from those of standard modules. Without diminishing the relevance of common, standardised, aging test, these structural changes might call for the development of new reliability-assessing-methods.

For instance, aging by current overloads, as in section 3 of this paper, might be a relevant performance indicator.

On the opposite, a 5 % increase of the resistance is a common failure criterion for wire bonded power modules. It is based on the fact that this increase induces a 5 % conduction loss increase and that it is an evidence that most bonding wires are already lifted-off (or on the verge to be so) and that the module is close to a catastrophic failure. Then, this criterion may have limited relevance in the case of PCB-embedded electronics, which is characterised by different failure mechanisms.

8   Conclusion

A PCB-embedding process using pressed metal foam to connect the top-side of PCB-embedded power dies has been considered. Results of an experimental

study of the reliability and robustness of this process have been presented: embedded dies were submitted to passive thermal cycling, current surges, destructive short-circuit tests, or repetitive short-circuit tests. Although the reliability and robustness has been shown to vary greatly from one sample to the other, some performed as well as state-of-the-art DBCs and wire-bonded packages. Finally, the development of new reliability-assessment-methods, suited to PCB-embedding processes, has been discussed.

Acknowledgements

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