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FPGA Implementation of STBC Based Cooperative Relaying System

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SUMMARY Multihop network is an approach utilizing distributed wireless stations for relaying. In this system, area size, coverage and total transmit power efficiency can be improved. It is shown by computer simulations that the cooperative relaying scheme provides transmit diversity effect, and can offer much better performance compared with that of non-cooperation case. To confirm this superior performance in actual environments, field trials using real time communication equipments are now being planned. This paper reports the design and the performance of wireless equipments for field trials.
key words: *multi-hop wireless networks, cooperative relaying, laboratory experiments, FPGA implementation*

1. Introduction

Multi-hop wireless networks can reduce transmit power, improve the area spectral efficiency, and enhance the system capacity [1], [2]. In this network, packets sent from the source station are relayed by the relay stations to get to the destination station. However, simple relaying causes considerable degradation of the end-to-end performance due to error propagation through the relay route.

Cooperative relaying networks having multiple relay stations at each hop can be a solution to this problem [3]–[5]. Cooperative relay stations work together using transmit diversity, and thus reduce errors owing to the diversity effect. In these networks, an error at a relay station can be recovered unless all relay stations at the hop fail to receive correctly, and the end-to-end performance can be improved compared to normal (one relay station at each hop) relaying networks. Moreover, the end-to-end packet error rate (PER) can remain nearly the same value regardless of the number of hops [3].

Cooperation by space-time block coded (STBC) [6] transmission is typical, and gives transmit diversity gain. Computer simulations show a significant improvement in PER in flat fading channels. This benefit becomes greater as the number of hops and the number of cooperative stations in each hop increase [7]. However, in computer simulations, all communication channels of multi-hop networks are supposed to be ideal Rayleigh fading channel in most cases.

The goal of this research is to evaluate the error rate performance of this cooperative relaying multi-hop wireless network in actual fading environments [8], [9]. As far as the authors' knowledge, experimental studies of cooperative relaying are channel capacity calculations [10] using measured data, or throughput measurements using wireless LAN equipments. In this paper, the design and the error rate performance of a cooperative relaying system are reported.

2. STBC Based Cooperative Relaying System

2.1 Network Configuration

Figure 1 shows the system model considered in this paper. The cooperative relay network consists of the source station, pairs of cooperative relay stations and the destination station. Each relay station forwards the received packet if it is correctly decoded. These relay stations cooperate each other to perform STBC transmission in order to obtain diversity gain. The routing algorithm is out of scope of this paper.

3. Transceiver Performance

3.1 EVM Performance

A transceiver is used as an up-converter from IF to RF. Since the transceiver chosen in this research is designed only for narrowband analog modulation, some modifications are made to expand its bandwidth. Figure 2 shows the error vector magnitude (EVM) performance versus the symbol rate. In this measurement, a vector signal generator and a wireless communication analyzer are connected through the transceiver (in transmitter mode). The generated $\pi/4$ shift

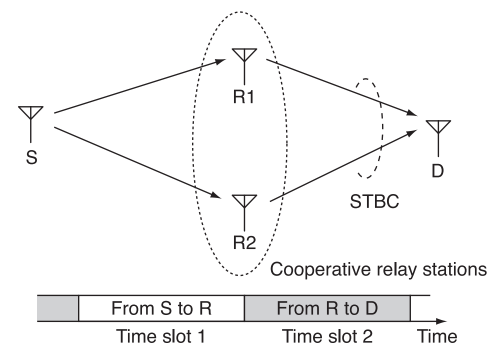

Fig. 1 Two-hop transmission system with cooperative relaying.

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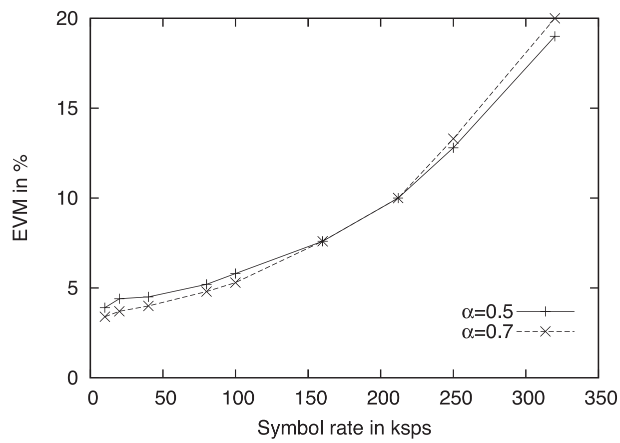

Fig. 2 EVM performance of transmitter versus symbol rate.

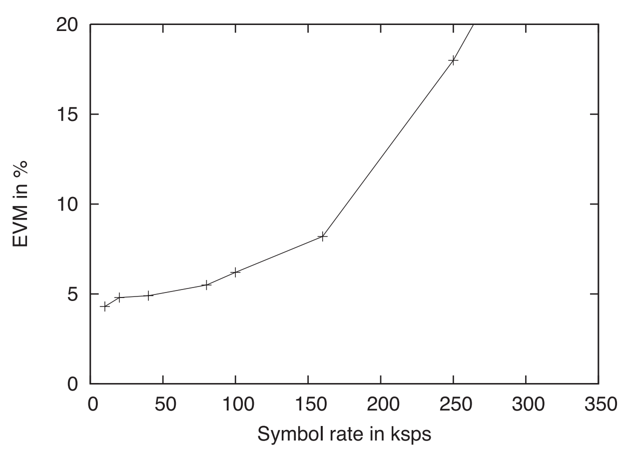

Fig. 3 EVM performance when the signal passes through both transmitter and receiver.

QPSK signal at carrier frequency of 10.85 MHz is fed into the transceiver. The RF output of the transceiver is analyzed in terms of EVM.

In Fig. 2, two cases of the roll off factor are compared. When the symbol rate is lower than around 150 k symbol/sec, the roll off factor of 0.7 gives better EVM performance than that of 0.5. It can be seen that the EVM value less than 4% can be achieved. Note that the EVM performance of the vector signal generator is around 1.5%.

As a next step, the EVM performance of the system consisting of two transceivers is evaluated. The transmitter up-converts the IF signal generated by the vector signal generator to the RF signal, and the receiver down-converts this RF signal to the IF signal before this signal is demodulated by the wireless communication analyzer. The EVM performance of this system is shown in Fig. 3. When the symbol rate is lower than around 50 k symbol/sec, the EVM value is less than 5%. In order to reduce the complexity of the receiver signal processing, we expect flat fading channels for the experiment so the data rate is set to satisfy the flat fading condition. This also lowers the EVM value. From these reason, the symbol rate of this system is chosen to be a similar

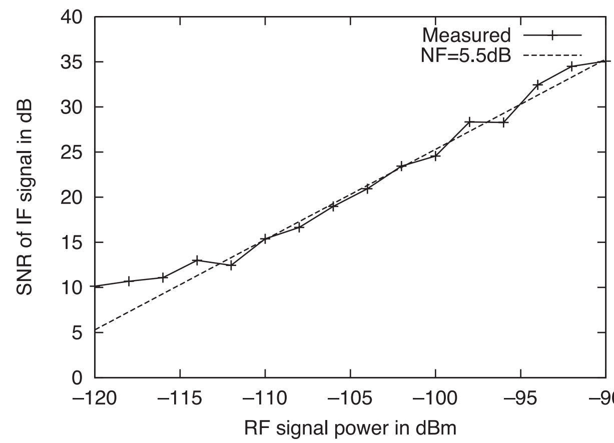

Fig. 4 SNR of IF signal versus RF signal power.

value of the PDC system.

3.2 Noise Figure

Noise figure of the receiver is measured by using a spectrum analyzer. Figure 4 shows the SNR of the IF signal along with a theoretical SNR in the case where the noise figure is 5.5 dB. From this figure, the estimated noise figure of this transceiver is 5.5 dB except the low signal power region below −114 dBm. This unexpected high SNR may be due to leak signals directly from the transmitter.

4. FPGA Implementation

The signaling format is shown in Fig. 5. A frame consists of 32 packets, in which the 8 pattern (fixed same data) packets are used for automatic gain control (AGC) setting, and the other 24 packets are valid data packets. By using the received training sequence, channel state information (CSI) and the received timing are estimated with a simple correlation technique. Major specifications of this implementation are given in Table 1.

4.1 Source Station

The logic circuits that generate the IF signal are implemented in a FPGA board as shown in Fig. 6. This includes a PN generator, a CRC encoder, a $\pi/4$-shift QPSK modulator, FIR filters, and a D/A converter. The FIR low pass filters have a square root roll off impulse response with 128 taps in length and a 8 times over sampling rate. The EVM value of the FPGA generated signal passing through the transmitter is about 5%. Compare with the case of a vector signal generator, the EVM degradation is less than 1%.

4.2 Relay Station

Figure 7 shows the block diagram of the relay station. In the relay stations, the relay transmission timing is determined

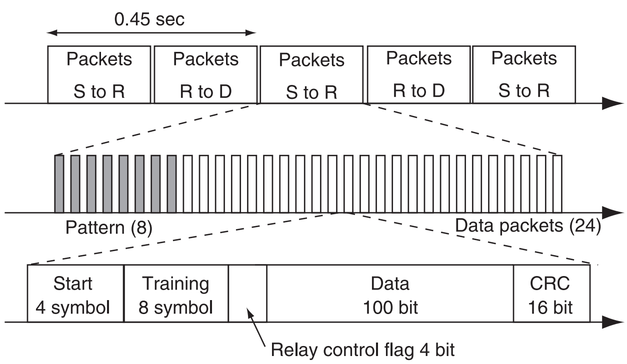

Fig. 5 Frame and packet structure.

Table 1 Major specifications.

Parameters	Values
Modulation scheme	$\pi/4$ shift QPSK
Symbol rate	21.1914 kHz
Radio frequency	1.299 GHz
Intermediate frequecy	10.85 MHz
Maximum RF output power	30 dBm
FIR filter	Root roll-off Nyquist ($\alpha = 0.7$)
FIR filter span	8 symbols
FPGA	Stratix EP1S25F780C5
Error detection	CRC-16
STBC	Alamouti scheme

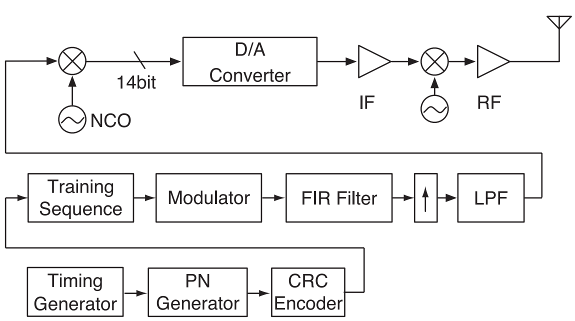

Fig. 6 Block diagram of source station.

based on the received timing of packets from the source station. All of the decoded packets are buffered, and then the correctly decoded packets are transmitted by using an STBC technique in the next time slot. The STBC code and the training sequence are uniquely assigned.

4.3 Destination Station

The block diagram of the destination station is given in Fig. 8. The major difference between the receiver part of the relay station and the destination station is the STBC decoder. In the channel estimation block, the two CSI from R1 and from R2 are estimated.

5. In-Lab Experiments of Cooperative Relaying

The block diagram of the experimental setup is shown in Fig. 9. Two fading emulators are employed as channels between S and R1, R2, and also between R1, R2 and D. The signal powers are adjusted by applying four RF attenuators (ATT) to the RF signal paths. Two RF switches are drove by the TTL signals from the FPGA. Figure 10 shows the experimental setup.

A timing synchronization algorithm and an automatic frequency control algorithm are implemented in R1, R2, and D [11]. Figure 11 shows the deviations of estimated timings

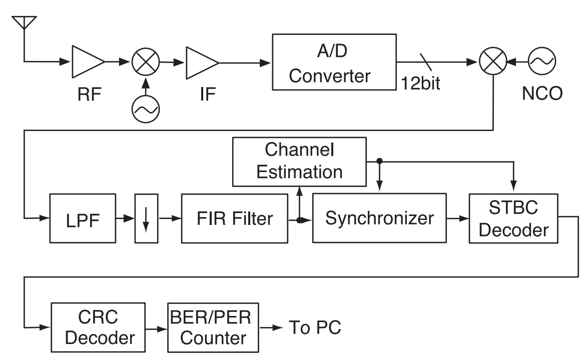

Fig. 8 Block diagram of destination station.

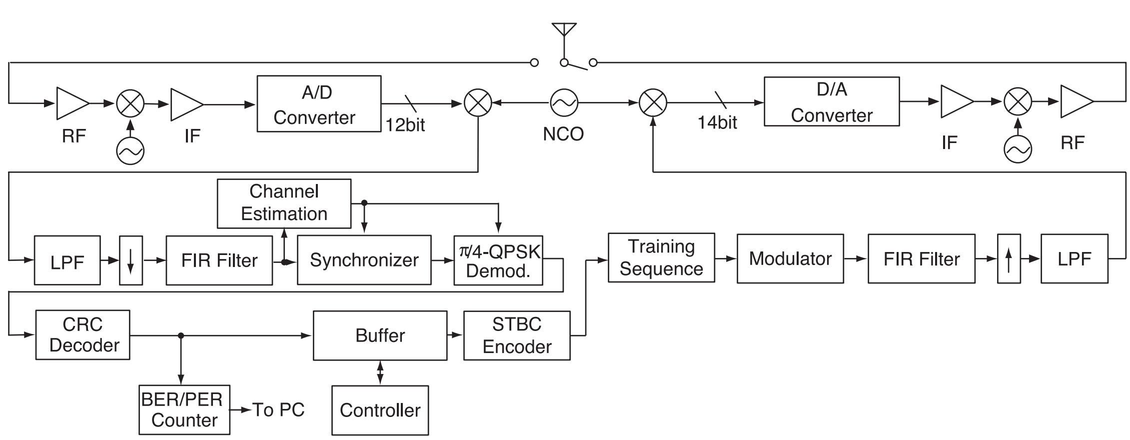

Fig. 7 Block diagram of relay station.

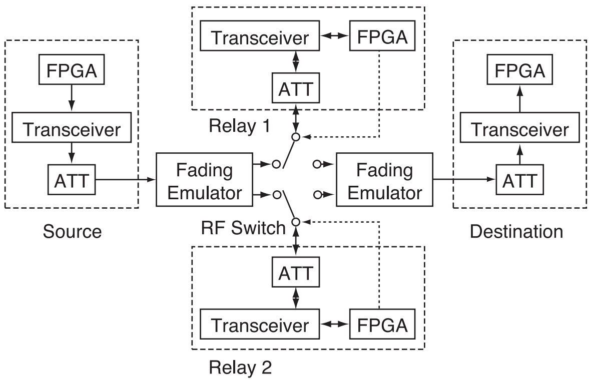

Fig. 9 Block diagram of experimental setup.

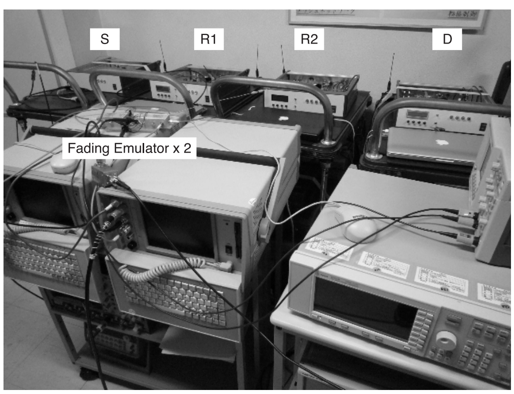

Fig. 10 Experimental setup.

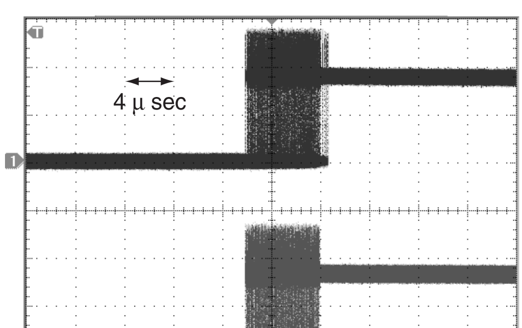

Fig. 11 Estimated timing deviations of relay stations R1 and R2.

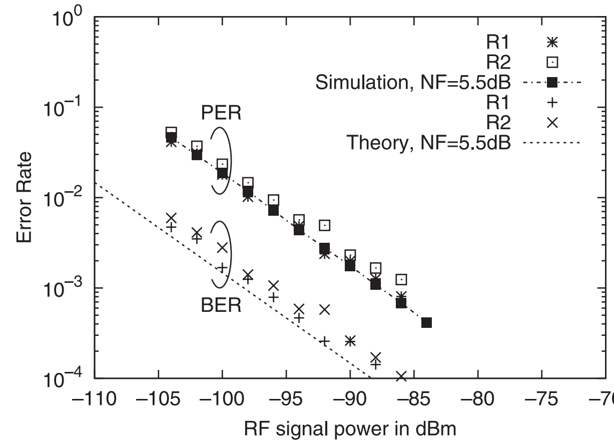

Fig. 12 Probability of error at relay stations versus received signal power on a frequency flat Rayleigh fading channel (maximum Doppler frequency = 1Hz). Computer simulation results are also plotted, with CSI, timings and frequencies known perfectly.

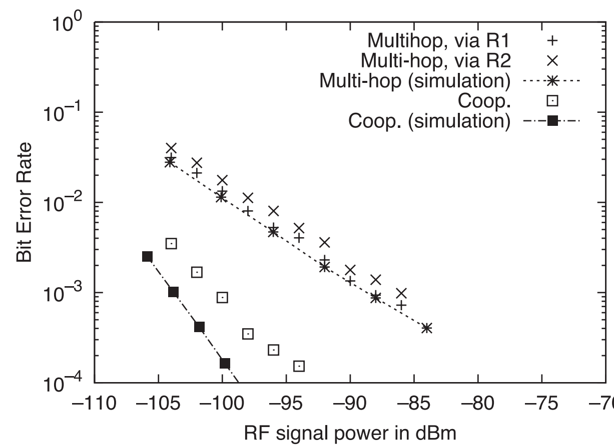

Fig. 13 Probability of bit error at destination station versus received signal power on a frequency flat Rayleigh fading channel (maximum Doppler frequency = 1Hz). Computer simulation results are also plotted, with CSI, timings and frequencies known perfectly.

at each relay station. The digital oscilloscope is triggered by the transmission timing of the source station. As can be seen, the timing deviations are within about 6 μ sec.

5.1 Error Performance of First Hop

For the sake of confirmation, the bit error rate (BER) and packet error rate (PER) performance of the relay stations is shown for an independent and identically distributed (i.i.d.) flat Rayleigh fading channel in Fig. 12. The theoretical BER performance of $\pi/4$-shift QPSK is also presented. For the computer simulation results and the theoretical BER performance, the noise figure of 5.5 dB is taken into considerations. As can be seen from this figure, the performance degradation due to CSI estimation error, timing synchronization error, and frequency tuning error is not severe.

5.2 Error Performance of Two-Hop Transmission

Figure 13 presents the results for BER as a function of the received signal power, again for an i.i.d. Rayleigh fading channel. For the computer simulation results, the noise figure of 5.5 dB is taken into considerations. One can see that the BER of cooperative relaying decreases rapidly compared with that of a multi-hop system. The results confirm the theory in the sense that cooperative relaying provides a higher diversity gain than non-cooperative relaying (multi-hop). However, the performance degradation of cooperative relaying compared with the computer simulation results is not negligible. This suggests that timing and frequency synchronization algorithms need to be further improved.

6. Conclusions

The design and the error rate performance of an STBC based cooperative relaying system has been presented. The developed system is fully hardware controlled, and personal computers are employed only for logging purposes. It is demonstrated that the cooperative relaying system can exhibit significant gains compared with a non-cooperative multi-hop system. Field trial results of the developed system will be reported in near future.

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