The CMS ECAL Very Front End Electronics: production and tests

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Abstract

The CMS electromagnetic calorimeter consists of about 76000 lead tungstate crystals. A brief description of the readout electronics chain of the calorimeter is given. About 15000 Very Front End (VFE) cards amplify, shape and digitize the signals of the photo-detectors attached to the crystals. The production and the test program for these VFE cards are presented. The test program includes the power on test, the burn in and the calibration of the read out channels. Preliminary results of the tests performed on 420 pre-series VFE cards are presented.

1 Introduction

The CMS [1] Electromagnetic Calorimeter (ECAL) is divided into a barrel (EB) and an end-cap (EE) part complemented by a silicon pre-shower detector in the end-cap region.
The EB is made of 61200 lead tungstate crystals arranged in 36 super modules (SM) each consisting of 1700 crystals each [2]. The two end-caps consist of 14648 crystals arranged in 4 Dee's each with 3662 crystals. The crystals are organized in matrices of 5x2 and 5x5, in the barrel and end-caps respectively. The electronics are arranged to read groups of 5x5 crystals in $\eta \times \varphi$. This corresponds to a trigger tower in the barrel and to a 'Super-crystal' in the end-caps. The scintillation light of the crystals is converted into an electrical signal by two Avalanche Photo-Diodes (APDs) in the EB and a vacuum photo-triode (VPT) in the EE. The photo-detectors are glued on the end face of the crystals. Kapton cables connect the photo-detectors to a motherboard. One motherboard serves one trigger tower. It houses 5 Very Front End (VFE) cards and a low voltage regulator card and distributes the regulated voltages [3]. The trigger tower electronics is completed by the Font End (FE) card which processes the digitized data from the 25 read out channels.
The scintillation light yield of the crystals varies by $-2\%/\mathrm{degC}$ and the gain of the APDs by $-2.3\%/\mathrm{degC}$. The calorimeter therefore requires a stable absolute temperature to within $0.1\mathrm{degC}$ over the expected LHC calibration period of $\sim 3\,\mathrm{months}$. Thermistors are attached to every 10^{th} crystal to follow any temperature variation.
The motherboard distributes and filters the reversed bias voltage to the APDs, adding $136\mathrm{k}\Omega$ series resistance. At a nominal APD gain of 50, the gain at $380\,\mathrm{V}$ varies with $3.3\%/\mathrm{V}$. However the leakage current of $\sim 10\,\mathrm{nA}$ of un-irradiated APDs increases to about $\sim 150\,\mathrm{nA}$ for those irradiated to a dose corresponding to 10 years of LHC running. This causes non-negligible voltage drops across the series resistance which require an adjustment of the bias voltage in order to keep the APD gain constant. Therefore the leakage currents of all APDs are measured, allowing a correction of the bias voltage setting in groups of 50 crystals, corresponding to 100 APDs.
The FE board [4] stores and processes the digitized data during the level 1 trigger latency of $\sim 3\mu\mathrm{sec}$. It utilizes 7 radiation tolerant FENIX Application Specific Integrated Circuits (ASICs) performing the following tasks: five FENIX chips buffer the data from the five VFE cards for the level one trigger, each doing a raw sum of the energy of one VFE card (strip sum in φ). Another FENIX generates the trigger tower energy by summing the five strips sums, identifies the associated bunch crossing and sends the information to the trigger

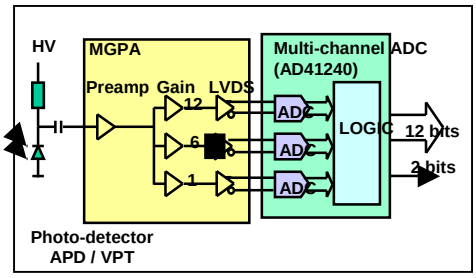

Figure 1: Read out chain for ECAL electronics

system using an optical link system with a Gigabit optical link (GOL) chip. The last FENIX is used as an event builder reading the data from the buffers and sending the data via a second optical link to the data acquisition system, provided a level 1 accept signal is present. The clock and control unit (CCU) chips developed for the CMS tracker project perform clock distribution and system control.

2 The Very Front End card

The VFE cards contain five identical read out channels. Each channel consists of a Multi Gain Pre-Amplifier (MGPA), an Analog to Digital Converter (AD41240) and two LVDS-Rx buffers designed in radiation tolerant $0.25\,\mu$m CMOS technology. The MGPA [5] consists of a low noise pre-amplifier stage, followed by three gain amplifiers with nominal gains 1, 6 and 12. The overall gain is fixed by an external resistor of $12\,\text{k}\Omega$ (in the EB) with 0.1% precision and 25 ppm/degC. The full-scale signal are 60 pC corresponding to ~1.67 TeV and 16 pC corresponding to 3.5TeV for barrel for end-caps respectively. The noise in the Ecal Barrel is ~8000 electrons for gains 6 and 12 and ~28000 electrons for gain 1. The linearity is close to ±0.1% of the full-scale. The three output signals of the MGPA are connected to the multi-channel ADC [6] by low voltage differential signals of $\pm 0.45\,\text{V}$ with common mode voltage of $1.25\,\text{V}$. The custom designed 12 bit 4-channel 40 MHz AD41240 automatically selects the optimal gain range by integrated digital selection logic. It outputs 12 LVDS signals for the ADC value plus 2 LVDS signals indicating the selected gain range. The LVDS-Rx adapts the output signals of the AD41240 to the single ended inputs of the FE board.
The MGPA allows the individual setting of the pedestals for the three different gains using integrated digital to analogue converters programmed via an I^2C interface. The I^2C bus is also used to program the test pulse unit of the MGPA. It allows to inject a test charge

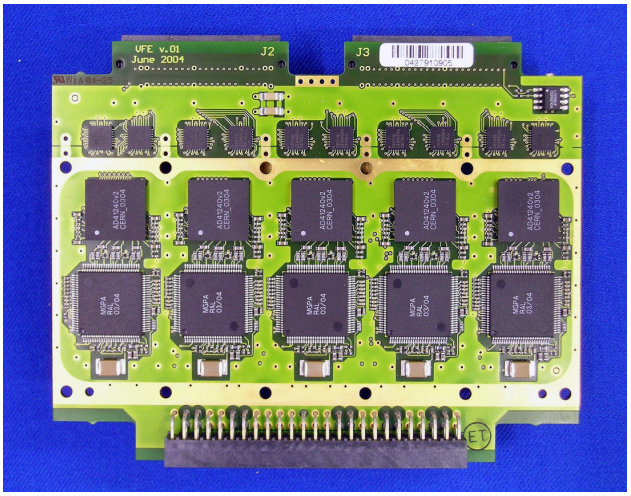

Figure 2: Very Front End card

into the input of the amplifier in the following way: the output of a DAC is charging a precise capacitor to a known voltage, which in turn is discharged by an external trigger. Each VFE card [7] uses a DCU (Detector Control Unit) for the measurement of the APD leakage currents and the crystal temperature.
The power consumption measured for 420 pre-series VFE cards is ~2.3 A (see figure 3) at 2.5 V corresponding to 1.15 W/channel. 1.2 A are used by the MGPA and the analog part of the AD41240, 0.97 A by the digital part of the AD41240 and 0.12 A by the LVDS-Rx buffers and the DCU.

3 The VFE production and test program

The production of 12800 VFE cards for the barrel calorimeter is planned with batches of 2000 cards/month. An option of 3000 cards for the ECAL end-caps is included in the contract.
After the tendering procedure the production of the VFE cards started in summer 2004 with 10 prototype PCBs, followed by a pre-series of 420 pieces.
The test program of the PCBs consists of an optical inspection, a “power on” test and a burn in which is followed by a complete calibration of each channel.
Thorough testing of the PCBs at the manufacturer is required in order to achieve the required production yield of 99 %.
All the VFEs are identified with a barcode (figure 2). This allows its unique identification and registration into a data base. All relevant test results are stored in this data base. During the construction of the calorimeter the geographical identification of each card

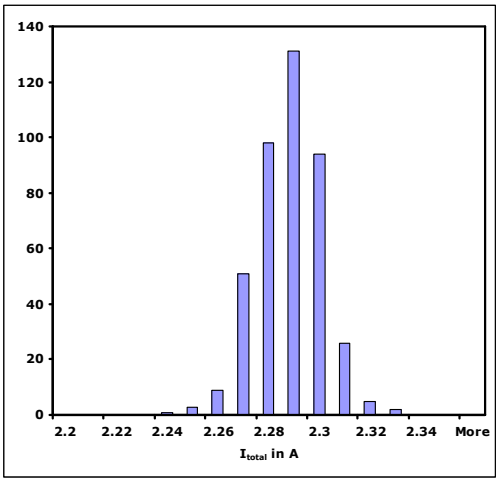

Figure 3: histogram of VFE power consumption

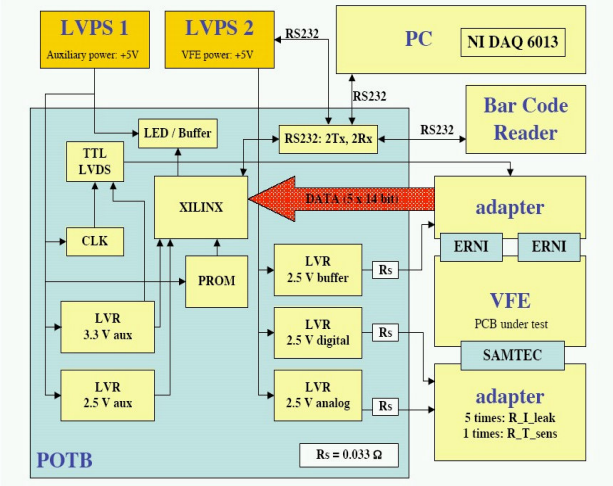

Figure 4: power on test block diagram

is registered associating the VFE calibration data with a given read out channel/crystal/APD. The production test program is the following:

- Automatic Optical Inspection (AOI) of the card by the manufacturer.
- Power-On test, including a limited functional test by the manufacturer. The required test set-up is provided by the ECAL collaboration (ETH).
- Burn-in test for three days at IN2P3, Lyon.
- Calibration and characterization of all cards. The calibration is done by three different institutes using identical test systems.

Out of the 420 PCB's requested for the pre-series, 416 were delivered. 120 of them failed the Optical Inspection and had to be repaired. The cards were then checked with the calibration test set-up at CERN, Lyon and Turin: 398 passed the test. The first ECAL Super module has been equipped with 340 tested boards and will be tested in the H4 beam at CERN the beginning of October.

3.1 Automatic Optical Inspection

The Automatic Optical Inspection (A.O.I.) test consists of pattern recognition of the cards. It checks the presence of all components, active and passive and verifies the soldering quality. The A.O.I. test is developed by the manufacturer, using a specialized machine.

3.2 Power On test

The power on test is the first electrical test of the VFE cards. All VFE cards are tested by the manufacturer.
The test system powers the VFE card and measures 4 voltages and currents:

- Output voltage and current of the power supply.
- Voltage and current of the MGPA and of the analog part of the ADC.
- Voltage and current of the digital part of the ADC.
- Voltage and current of the LVDS to single ended CMOS buffers.
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A functional test will be implemented into the Power On test using a Xilinx FPGA to read simulated APD leakage currents and crystal temperatures from the DCU, to select the ADC gain modes, and to record and analyze the data generated by the MGPA test pulse system.

3.3 Burn in

The burn-in [8] test of fully assembled VFE boards is carried out to find infant mortality failures and freak failures. A burn in period of 3 days at an elevated ambient temperature of 60^{o}C is proposed. Up to 300 cards at one time can be tested. All cards will be tested at their nominal voltage of $2.5\,V$. The $40\,MHz$ clock will be distributed through a special mother board. A PC workstation will monitor the clock and the total current of the VFE.

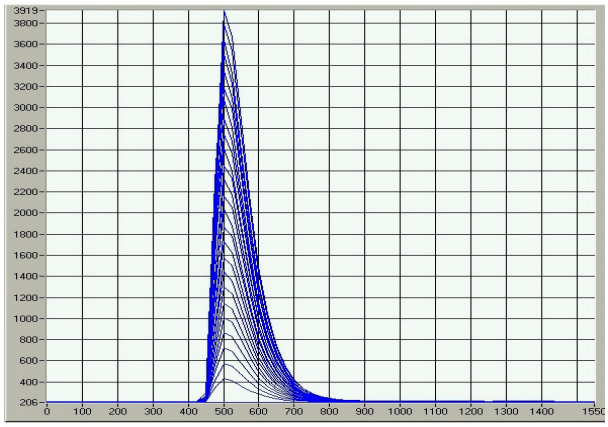

Figure 5: charge pulses in ADC counts vs. time for gain 1

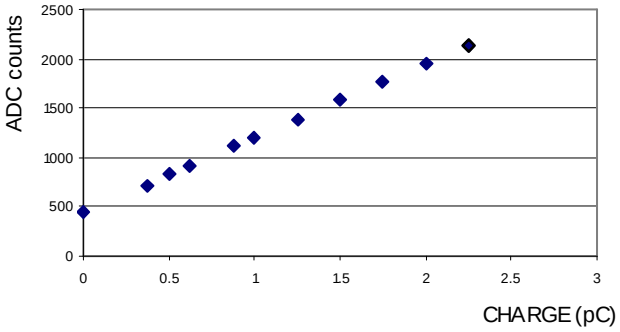

Figure 6: linearity in the highest gain

Burn-in will start with 50 cards from the pre-series in order to gain experience and confirm if the burn-in period is appropriate.

3.4 Calibration

The calibration test is intended to check the operational parameters of the VFE card. The steps of the test are:

- Measure the pedestal and noise at three different gains.
- Vary the size of a charge pulse injection over the full dynamic range and verify the linearity.
- Simulate the leakage current of the APDs.
- Testing the temperature read out channel from the crystal.

In order to measure the pedestal, the noise and to check the linearity a CAMAC charge generator is used. It injects different values of charge into the VFE and a test board measures the output of the ADC. The response in ADC counts is recorded over the full dynamic range ($0 - 60$pC) for all three gains of the five channels of each VFE card.
The stability of the leakage current and consequently the precision of the APD gain is tested using a current source which simulates a variation of the leakage current ($0 - 200$nA) to the input of the VFE. The data are collected by the DCU chip on the VFE and are sent to the data acquisition system via the I^2C bus. For the temperature read out channel of the crystal, the test board uses a digital potentiometer that changes its value to simulate a temperature variation of the crystals.

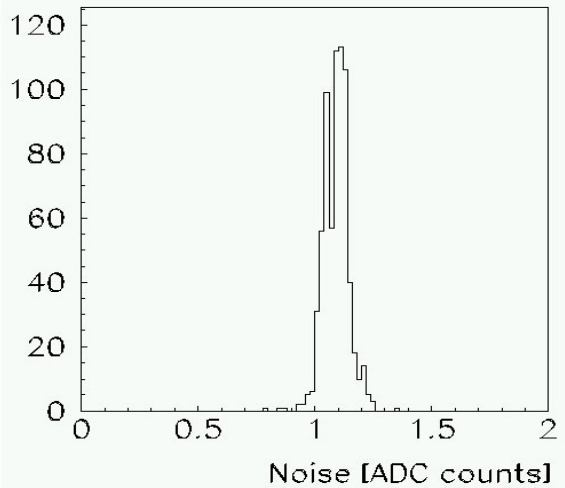

Figure 7: the average noise over 675 channels in gain 12

The DCU reads and sends the data to the data acquisition system. All data are first sent to an ALTERA FGPA placed on the test board and then via a RS 232 bus to the PC where they are stored in a Data Base.
The linearity of the response of the VFE on the whole scale is shown for gain 12 in figure 6.
The sigma of the noise for the three gains was measured for 675 channels and the results in ADC counts (see figure 7) are around 0.6 for gain 1, 0.7 for gain 6 and 1.2 for gain 12.
The pedestal was measured for 2 days on a trigger tower (25 channels) and the variation was less than one ADC count (see figure 8).

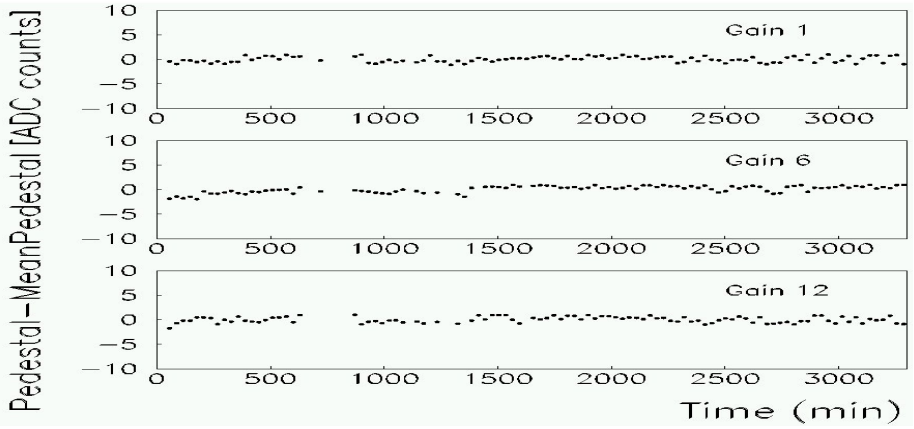

Figure 8: pedestal stability in the three gains

4 Conclusions

The production of the VFE cards has started with the fabrication of 420 pre-series cards. Different test set ups have been developed and built. In particular the power on test set up was systematically applied by the manufacturer. It identified several simple failures. The integration of the functional test will identify the majority of the failures at an early stage during the series production.
The Burn in will start with a pre-series of 50 VFE cards in first half of October.
The calibration test has to be finalized although it has been significantly improved in the past two months.
During the pre-production test the calibration system was not fully operational and only a functional test of the 420 VFE cards was possible.
A full Trigger Tower (25 channels) with 5 VFE, 1 FE board and 1 LVR board was tested with beam at PSI with 10^9 p/cm^2/s for 2 hours and:

- No Data errors were discovered
- Power consumption didn't change, as expected for this technology.
- The baseline moved from 200 to 600 ADC counts after 2h irradiation, corresponding to 10 years of LHC running in the ECAL barrel. However this can be monitored and corrected using the I^2C.

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