Introduction to Instruction-Set Customization

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Over the last years, we have witnessed the increased use of customizable processors. These processors can be tuned and/or extended to meet specific requirements and to achieve a balance between performance, power, hardware resources and time-to-market. The problems involved are numerous and they tend to have high computational complexity. One of the main approaches is the identification of the most suitable instructions to include in the instruction-set. The customization of a given instruction-set with specialized application-specific instructions has become a common technique used to speed up the execution of applications. As a result, in this session we first present two papers focusing on methods to design custom instructions and then, a paper which gives an overview on contemporary architectures that offer dynamic instruction-set support.

Kevin Martin et al. present a constrain-driven method for fast identification of computational patterns which form a base for application-specific instruction selection and processor extension generation.

Kingshuk Karuri et al. present a generic and easily adaptable flow for application oriented instruction-set extension design that supports both of the prevalent ASIP design paradigms - complete ISA design from scratch through an extensive design-space exploration, or limited ISA adaptation for a pre-designed and pre-verified base-processor core.

Huynh Phung Huynh and Tulika Mitra provide a detailed survey of the contemporary architectures that offer dynamic instruction-set support and discuss compiler and/or runtime techniques to exploit such architectures.

K. Bertels et al. (Eds.): SAMOS 2009, LNCS 5657, p. 193, 2009.